AMIS-49587

Product Preview

Power Line Carrier Modem

ON Semiconductor's AMIS-49587 is an IEC 61334-5-1 compliant power line carrier modem using spread-FSK (S-FSK) modulation for robust low data rate communication over power lines. AMIS-49587 is built around an ARM 7TDMI processor core, and includes the MAC layer. With this robust modulation technique, signals on the power lines can pass long distances. The half-duplex operation is automatically synchronized to the mains, and can be up to 2400 bits/sec.

The product configuration is done via its serial interface, which allows the user to concentrate on the development of the application.

The AMIS-49587 is implemented in ON Semiconductor mixed signal technology, combining both analog circuitry and digital functionality on the same IC.

Features

- Power Line Carrier Modem for 50 and 60 Hz Mains
- Fully compliant to IEC 61334-5-1 and CENELEC EN 50065-1
- Complete Handling of Protocol Layers Physical to MAC
- Programmable Carrier Frequencies from 9 to 95 kHz in 10 Hz Steps
- Half Duplex
- Data Rate Selectable: 300 – 600 – 1200 – 2400 baud (@ 50 Hz)
  360 – 720 – 1440 – 2880 baud (@ 60 Hz)
- Synchronization on Mains
- Repetition Algorithm Boost the Robustness of Communication
- SCI Port to Application Microcontroller
- SCI Baudrate Selectable: 4.8 – 9.6 – 19.2 – 34.4 kb
- Power Supply 3.3 V
- Ambient Temperature Range: -40°C to +80°C
- These Devices are Pb-Free and are RoHS Compliant*

Typical Applications

- ARM: Automated Remote Meter Reading (Télérelevé)
- Remote Security Control
- Streetlight Control
- Transmission of Alerts (Fire, Gas Leak, Water Leak)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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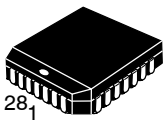
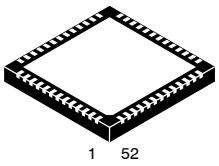
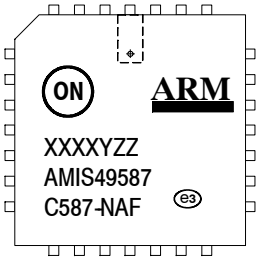


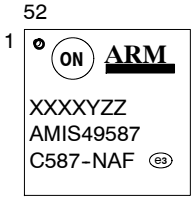
PLCC 28 Lead
CASE 776AA



QFN52 8x8, 0.5P
CASE 485M

MARKING DIAGRAMS





XXXX = Date Code
Y = Plant Identifier
ZZ = Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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1 APPLICATION

1.1 APPLICATION EXAMPLE

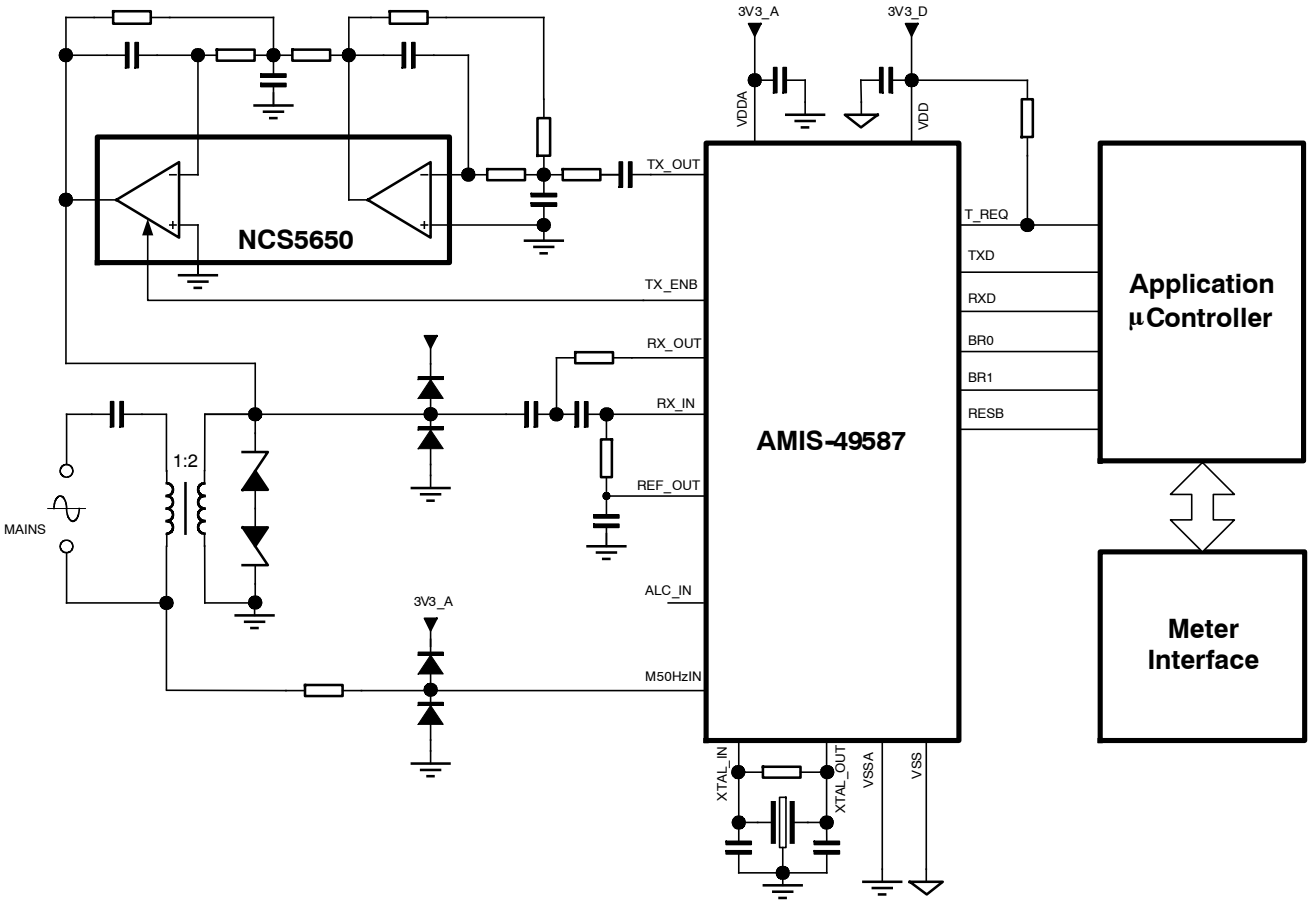

Figure 1. Typical Application for the AMIS−49587 S−FSK Modem

Table 1. ORDERING INFORMATION

Part No.	Temperature Range	Package	Shipping†
AMIS49587C5871G	−40°C − +80°C	PLCC−28 (Pb−Free)	Tube
AMIS49587C5871RG	−40°C − +80°C	PLCC−28 (Pb−Free)	Tape & Reel
AMIS49587C5872G	−40°C − +80°C	QFN−52 (Pb−Free)	Tube
AMIS49587C5872RG	−40°C − +80°C	QFN−52 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in this clause may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2.1.1 Power Supply Pins VDD, VDDA, VSS, VSSA

Table 2. ABSOLUTE MAXIMUM RATINGS SUPPLY

Rating	Symbol	Min	Max	Unit
Absolute maximum digital power supply	V_{DD_ABSM}	V_{SS}−0.3	3.9	V
Absolute maximum analog power supply	V_{DDA_ABSM}	V_{SSA}−0.3	3.9	V
Absolute maximum difference between digital and analog power supply	V_{DD}−V_{DDA_ABSM}	−0.3	0.3	V
Absolute maximum difference between digital and analog ground	V_{SS}−V_{SSA_ABSM}	−0.3	0.3	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2.1.2 Non 5V Safe Pins: TX_OUT, ALC_IN, RX_IN, RX_OUT, REF_OUT, M50HZ_IN, XIN, XOUT, TDO, TDI, TCK, TMS, TRSTB, TEST

Table 3. ABSOLUTE MAXIMUM RATINGS NON 5V SAFE PINS

Rating	Symbol	Min	Max	Unit
Absolute maximum input for normal digital inputs and analog inputs	V_{IN_ABSM}	V_{SS*}−0.3	V_{DD*}+0.3	V
Absolute maximum voltage at any output pin	V_{OUT_ABSM}	V_{SS*}−0.3	V_{DD*}+0.3	V

2.1.3 5V Safe Pins: TX_ENB, TXD, RXD, BR0, BR1, RESB, RX_DATA, TREQ, CRC, TX_DATA/PRE_SLOT

Table 4. ABSOLUTE MAXIMUM RATINGS 5V SAFE PINS

Rating	Symbol	Min	Max	Unit
Absolute maximum input for digital 5 V safe inputs	V_{5VS_ABSM}	V_{SS}−0.3	6.0	V
Absolute maximum voltage at 5 V safe output pin	V_{OUT5V_ABSM}	V_{SS}−0.3	3.9	V

2.2 Normal Operating Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in the Receiver Block Diagram Section and for the reliability specifications as listed in the Local Transfer and Configuration Commands (LTC) Section. Functionality outside these limits is not implied.

Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1% of the useful life as defined in the Local Transfer and Configuration Commands (LTC) Section.

Table 5. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Power Supply Voltage Range	V_{DD}	3.0	3.6	V
Ambient Temperature	T_A	−25	70	°C

3 PIN DESCRIPTION

3.1 PLCC Packaging

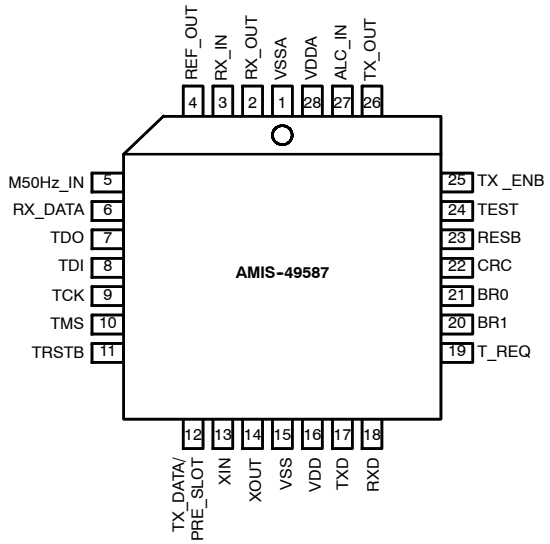


Figure 2. Pinout

Table 6. AMIS−49587 PLCC PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
1	VSSA		P	Analog ground
2	RX_OUT	Out	A	Output of receiver low noise operational amplifier
3	RX_IN	In	A	Positive input of receiver low noise operational amplifier
4	REF_OUT	Out	A	Reference output for stabilization
5	M50HZ_IN	In	A	50/60 Hz input for mains zero cross detection
6	RX_DATA	Out	D, 5V Safe	Data reception indication (open drain output)
7	TDO	Out	D	Test data output
8	TDI	In	D	Test data input (internal pulldown)
9	TCK	In	D	Test clock (internal pulldown)
10	TMS	In	D	Test mode select (internal pulldown)
11	TRSTB	In	D	Test reset bar (internal pulldown, active low)
12	TX_DATA/ PRE_SLOT	Out	D, 5V Safe	Data output corresponding to transmitted data or PRE_SLOT signal (open drain output)
13	XIN	In	A	Xtal input (can be driven by an internal clock)
14	XOUT	Out	A	Xtal output (output floating when XIN driven by external clock)
15	VSS		P	Digital ground
16	VDD		P	3.3 V digital supply
17	TXD	Out	D, 5V Safe	SCI transmit output (open drain)
18	RXD	In	D, 5V Safe	SCI receive input (Schmitt trigger input)
19	T_REQ	In	D, 5V Safe	Transmit request input
20	BR1	In	D, 5V Safe	SCI baud rate selection
21	BR0	In	D, 5V Safe	SCI baud rate selection
22	CRC	Out	D, 5V Safe	Correct frame CRC indication (open drain output)
23	RESB	In	D, 5V Safe	Master reset bar (Schmitt trigger input, active low)
24	TEST	In	D	Test enable (internal pulldown)
25	TX_ENB	Out	D, 5V Safe	TX enable bar (open drain)
26	TX_OUT	Out	A	Transmitter output
27	ALC_IN	In	A	Automatic level control input
28	VDDA		P	3.3 V analog supply

P: Power pin
A: Analog pin
D: Digital pin

5V Safe: IO that support the presence of 5V on bus line
Out: Output signal
In: Input signal
In/Out: Bi−directional pin

3.2 QFN Packaging

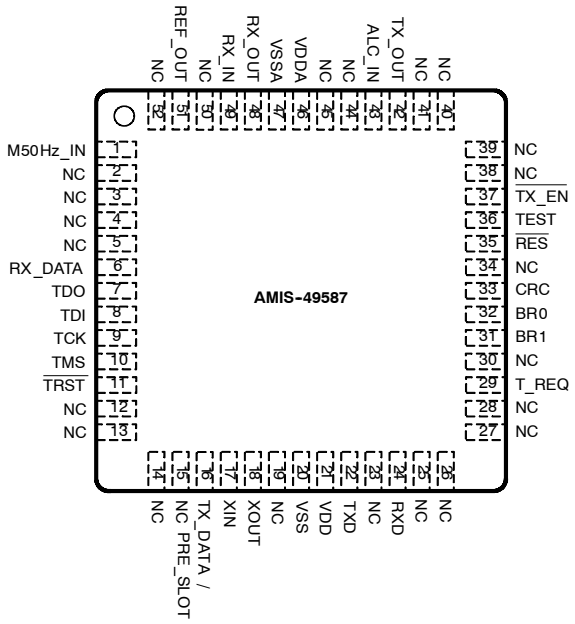


Figure 3. QFN Pin-out of AMIS-49587 (Top view)

Table 7. AMIS-49587 QFN PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
1	M50HZ_IN	In	A	50/60Hz input for mains zero cross detection
6	RX_DATA	Out	D, 5V Safe	Data reception indication (open drain output)
7	TDO	Out	D	Test data output
8	TDI	In	D	Test data input (internal pull down)
9	TCK	In	D	Test clock (internal pull down)
10	TMS	In	D	Test mode select (internal pull down)
11	TRSTB	In	D	Test reset bar (internal pull down, active low)
16	TX_DATA/PRE_SLOT	Out	D, 5V Safe	Data output corresponding to transmitted data or PRE_SLOT signal (open drain)
17	XIN	In	A	Xtal input (can be driven by an internal clock)
18	XOUT	Out	A	Xtal output (output floating when XIN driven by external clock)
20	VSS		P	Digital ground
21	VDD		P	3.3 V digital supply
22	TXD	Out	D, 5V Safe	SCI transmit output (open drain)
24	RXD	In	D, 5V Safe	SCI receive input (Schmitt trigger input)
29	T_REQ	In	D, 5V Safe	Transmit Request input
31	BR1	In	D, 5V Safe	SCI baud rate selection
32	BR0	In	D, 5V Safe	SCI baud rate selection
33	CRC	Out	D, 5V Safe	Correct frame CRC indication (open drain output)
35	RESB	In	D, 5V Safe	Master reset bar (Schmitt trigger input, active low)
36	TEST	In	D	Test enable (internal pull down)

P: Power pin
A: Analog pin
D: Digital pin

5V Safe: IO that support the presence of 5 V on bus line
Out: Output signal
In: Input signal

Table 7. AMIS−49587 QFN PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
37	TX_ENB	Out	D, 5V Safe	TX enable bar (open drain)
42	TX_OUT	Out	A	Transmitter output
43	ALC_IN	In	A	Automatic level control input
46	VDDA		P	3.3 V analog supply
47	VSSA		P	Analog ground
48	RX_OUT	Out	A	Output of receiver low noise operational amplifier
49	RX_IN	In	A	Positive input of receiver low noise operational amplifier
51	REF_OUT	Out	A	Reference output for stabilization
2, 3, .. 50, 52	NC			Pins 2, 3, 4, 5, 12, 13, 14, 15, 19,23, 25, 26, 27, 28, 30, 34, 38, 39, 40, 42, 44, 45, 50, 52 are not connected. These pins need to be left open or connected to the GND plane

P: Power pin
A: Analog pin
D: Digital pin
5V Safe: IO that support the presence of 5 V on bus line
Out: Output signal
In: Input signal

3.3 Detailed Pin Description

VDDA
VDDA is the positive analog supply pin. Nominal voltage is 3.3 V. A ceramic decoupling capacitor C_{DA} = 100 nF ± 10% must be placed between this pin and the VSSA. Connection path of this capacitance to the VSSA on the PCB should be kept as short as possible in order to minimize the serial resistance.

REF_OUT
REF_OUT is the analog output pin which provides the voltage reference used by the A/D converter. This pin must be decoupled to the analog ground by a 1 μF ± 10 percent ceramic capacitance C_{DREF}. The connection path of this capacitor to the VSSA on the PCB should be kept as short as possible in order to minimize the serial resistance.

VSSA
VSSA is the analog ground supply pin.

VDD
VDD is the 3.3 V digital supply pin. A ceramic decoupling capacitor C_{DD} = 100 nF ± 10% must be placed between this pin and the VSS. Connection path of this capacitance to the VSS on the PCB should be kept as short as possible in order to minimize the serial resistance.

VSS
VSS is the digital ground supply pin.

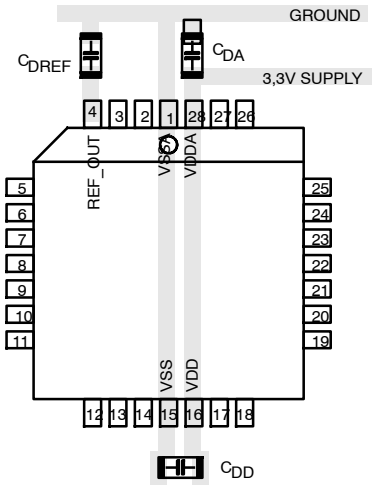


Figure 4. Recommended Layout of the Placement of Decoupling Capacitors for PLCC-28

RX_OUT

RX_OUT is the output analog pin of the receiver low noise input op-amp. This op-amp is in a negative feedback configuration.

RX_IN

RX_IN is the positive analog input pin of the receiver low noise input op-amp. Together with RX_OUT and REF_OUT, an active high pass filter is realized. This filter removes the main frequency (50 or 60 Hz) from the received signal. The filter characteristics are determined by external capacitors and resistors. A typical application schematic can be found in paragraph 50/60 Hz suppression filter.

M50Hz_IN

M50HZ_IN is the mains frequency analog input pin. The signal is used to detect the zero crossing of the 50 or 60 Hz sine wave. This information is used, after filtering with the internal PLL, to synchronize frames with the mains frequency. In case of direct connection to the mains it is advised to use a series resistor of 1 MΩ in combination with two external clamp diodes in order to limit the current flowing through the internal protection diodes.

RX_DATA

RX_DATA is a 5 V compliant open drain output. An external pull-up resistor defines the logic high level as illustrated in Figure 5. A typical value for the pull-up resistance “R” is 10 kΩ. The signal on this output depends on the status of the data reception. If AMIS-49587 waits for configuration RX_DATA outputs a pulse train with a 10 Hz frequency. After Synchronization Confirm Time out RX_DATA = 0. If AMIS-49587 is searching for synchronization RX_DATA = 1.

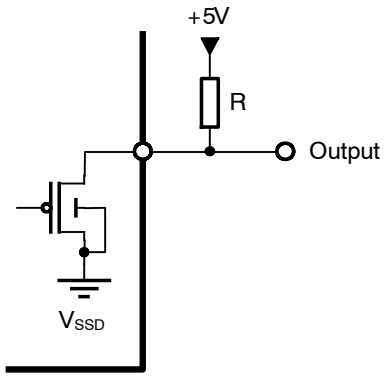


Figure 5. Representation of 5V Safe Output

TDO, TDI, TCK, TMS, and TRSTB

All these pins are part of the JTAG bus interface. The JTAG interface is used during production test of the IC and will not be described here. Input pins (TDI, TCK, TMS, and TRSTB) contain internal pull−down resistance. TDO is an output. When not used, the JTAG interface pins may be left floating.

TX_DATA/PRE_SLOT

TX_DATA/PRE_SLOT is the output for either the transmitting data (TX_DATA) or a synchronization signal with the time−slots (PRE_SLOT). More information can be found in paragraph Local Port.

XIN

XIN is the analog input pin of the oscillator. It is connected to the interval oscillator inverter gain stage. The clock signal can be created either internally with the external crystal and two capacitors or by connecting an external clock signal to XIN. For the internal generation case, the two external capacitors and crystal are placed as shown in Figure 6. For the external clock connection, the signal is connected to XIN and XOUT is left unused.

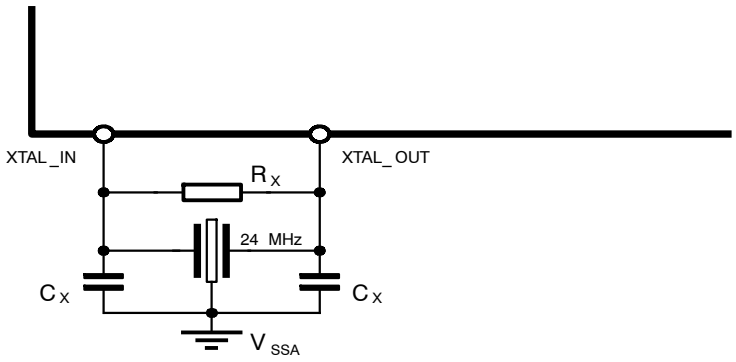


Figure 6. Placement of the Capacitors and Crystal with Clock Signal Generated Internally

The crystal is a classical parallel resonance crystal of 24 MHz. The values of the capacitors C_X are given by the manufacturer of the crystal. A typical value is 30 pF. The crystal has to fulfill impedance characteristics specified in the AMIS−49587 data sheet. As an oscillator is sensitive and precise, it is advised to put the crystal as close as possible on the board and to ground the case.

XOUT

XOUT is the analog output pin of the oscillator. When the clock signal is provided from an external generator, this output must be floating. When working with a crystal, this pin cannot be used directly as clock output because no additional loading is allowed on the pin (limited voltage swing).

TXD

TXD is the digital output of the asynchronous serial communication (SCI) unit. Only half−duplex transmission is supported. It is used to realize the communication between the AMIS−49587 and the application microcontroller. The TXD is an open drain IO (5 V safe). External pull−up resistances (typically 10 kΩ) are necessary to generate the 5 V level. See Figure 5 for the circuit schematic.

RXD

This is the digital input of the asynchronous SCI unit.
Only half−duplex transmission is supported. This pin supports a 5 V level. It is used to realize the communication between the AMIS−49587 and the application microcontroller. RXD is a 5 V safe input.

T_REQ

T_REQ is the transmission request input of the Serial Communication Interface. When pulled low its initiate a local communication from the application micro controller to AMIS−49587. T_REQ is a 5 V safe input.

BR1, BR0

BR0 and BR1 are digital input pins. They are used to select the baud rate (bits/second) of the Serial Communication Interface unit. The rate is defined according to Table 28: BR1, BR0 Baud Rates. The values are taken into account after a reset, hardware or software. Modification of the baud rate during function is not possible. BR0 and BR1 are 5 V safe.

CRC
CRC is a 5V compliant open drain output. An external pull-up resistor defines the logic high level as illustrated in Figure 5. A typical value for this pull-up resistance “R” is 10 kΩ. The signal on this output depends on the cyclic redundancy code result of the received frame. If the cyclic redundancy code is correct CRC = 1 during the pause between 2 time slots.

RESB
RESB is a digital input pin. It is used to perform a hardware reset of the AMIS-49587. This pin supports a 5 V voltage level. The reset is active when the signal is low (0 V).

TEST
TEST is a digital input pin. It is used to enable the test mode of the chip. Normal mode is activated when TEST signal is low (0 V). For normal operation, the TEST pin may be left unconnected. Due to the internal pulldown, the signal is maintained to low (0 V). TEST pin is not 5 V safe.

TX_ENB
TX_ENB is a digital output pin. It is low when the transmitter is activated. The signal is available to turn on the line driver. TX_ENB is a 5 V safe with open drain output, hence a pull-up resistance is necessary achieve the requested voltage level associated with a logical one. See also Figure 5 for reference.

TX_OUT
TX_OUT is the analog output pin of the transmitter. The provided signal is the S-FSK modulated frames. A filtering operation must be performed to reduce the second order harmonic distortion. For this purpose an active filter is realized. Figure 7 gives the representation of this filter.

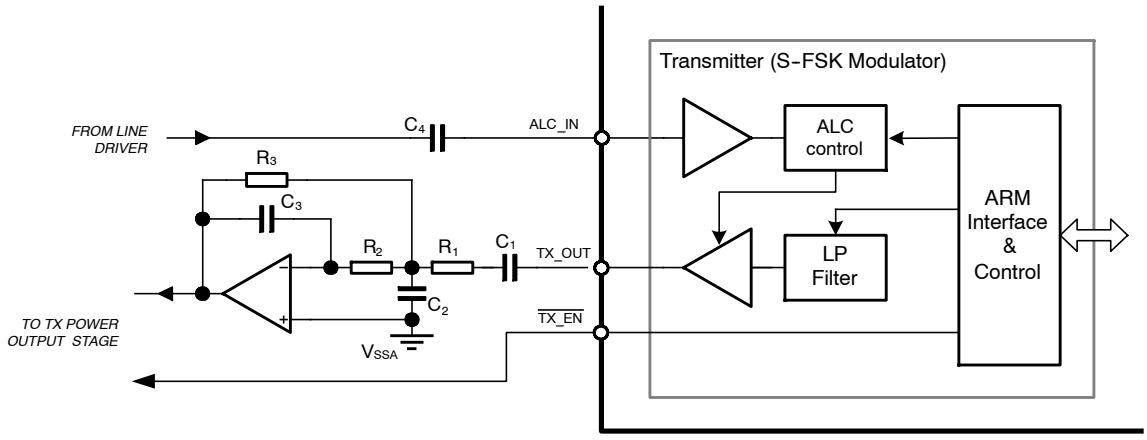


Figure 7. TX_OUT Filter

ALC_IN
ALC_IN is the automatic level control analog input pin. The signal is used to adjust the level of the transmitted signal. The signal level adaptation is based on the AC component. The DC level on the ALC_IN pin is fixed internally to 1.65 V. Comparing the peak voltage of the AC signal with two internal thresholds does the adaptation of the gain. Low threshold is fixed to 0.4 V. A value under this threshold will result in an increase of the gain. The high threshold is fixed to 0.6 V. A value over this threshold will result in a decrease of the gain. A serial capacitance is used to block the DC components. The level adaptation is performed during the transmission of the first two bits of a new frame. Eight successive adaptations are performed.

4 ELECTRICAL CHARACTERISTICS

4.1 DC AND AC CHARACTERISTICS

4.1.1 Oscillator: Pin XIN, XOUT

In production the actual oscillation of the oscillator and duty cycle will not be tested. The production test will be based on the static parameters and the inversion from XIN to XOUT in order to guarantee the functionality of the oscillator.

Table 8. OSCILLATOR

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Crystal frequency	(Note 1)	f_{CLK}	−100 ppm	24	+100 ppm	MHz
Duty cycle with quartz connected	(Note 1)		40		60	%
Start−up time	(Note 1)	$T_{startup}$			50	ms
Maximum Capacitive load on XOUT	XIN used as clock input	CL_{XOUT}			50	pF
Low input threshold voltage	XIN used as clock input	VIL_{XOUT}	0.3 V_{DD}			V
High input threshold voltage	XIN used as clock input	VIH_{XOUT}			0.7 V_{DD}	V
Low output voltage	XIN used as clock input, XOUT = 2 mA	VOL_{XOUT}			0.3	V
High input voltage	XIN used as clock input	VOH_{XOUT}			V_{DD}−0.3	V

1. Guaranteed by design. Maximum allowed series loss resistance up to 80 Ω.

4.1.2 Zero Crossing Detector and 50/60 Hz PLL: Pin M50HZ_IN

Table 9. ZERO CROSSING DETECTOR AND 50/60 Hz PLL

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum peak input current		$Imp_{M50HZIN}$	−20		20	mA
Maximum average input current	During 1 ms	$Imavg_{M50HZIN}$	−2		2	mA
Mains voltage (ms) range	With protection resistor at M50HZIN	V_{MAINS}	90		550	V
Rising threshold level	(Note 2)	$VIRM_{50HZIN}$			1.9	V
Falling threshold level	(Note 2)	$VIFM_{50HZIN}$	0.9			V
Hysteresis	(Note 2)	VHY_{50HZIN}	0.4			V
Lock range for 50 Hz (Note 3)	MAINS_FREQ = 0 (50 Hz)	$Flock_{50Hz}$	45		55	Hz
Lock range for 60 Hz (Note 3)	MAINS_FREQ = 0 (60 Hz)	$Flock_{60Hz}$	54		66	Hz
Lock time (Note 3)	MAINS_FREQ = 0 (50 Hz)	$Tlock_{50Hz}$			15	s
Lock time (Note 3)	MAINS_FREQ = 0 (60 Hz)	$Tlock_{60Hz}$			20	s
Frequency variation without going out of lock (Note 3)	MAINS_FREQ = 0 (50 Hz)	DF_{60Hz}			0.1	Hz/s
Frequency variation without going out of lock (Note 3)	MAINS_FREQ = 0 (60 Hz)	DF_{50Hz}			0.1	Hz/s
Jitter of CHIP_CLK (Note 3)		$Jitter_{CHIP\_CLK}$	−25		25	μs

2. Measured relative to V_{SS}.
3. These parameters will not be measured in production since the performance is totally dependent of a digital circuit which will be guaranteed by the digital test patterns.

4.1.3 Transmitter External Parameters: Pin TX_OUT, ALC_IN, TX_ENB

To guarantee the transmitter external specifications the TX_CLK frequency must be 12 MHz ± 100 ppm.

Table 10. TRANSMITTER EXTERNAL PARAMETERS

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum peak output level	fTX_OUT = 23.75 kHz fTX_OUT = 95 kHz Level control at max. output	V_{TX_OUT}	0.85 0.76		1.15 1.22	Vp
Second order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output	HD2			−56	dB
Third order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output	HD3			−58	dB
Frequency accuracy of the generated sine wave	(Notes 4 and 6)	Df_{TX_OUT}			30	Hz
Capacitive output load at pin TX_OUT	(Note 4)	CL_{TX_OUT}			20	pF
Resistive output load at pin TX_OUT		RL_{TX_OUT}	5			kΩ
Turn off delay of TX_ENB output	(Note 5)	Td_{TX_ENB}	0.25		0.5	ms
Automatic level control attenuation step		ALC_{step}	2.9		3.1	dB
Maximum attenuation		ALC_{range}	20.3		21.7	dB
Low threshold level on ALC_IN		VTL_{ALC_IN}	−0.46		−0.36	V
High threshold level on ALC_IN		VTH_{ALC_IN}	−0.68		−0.54	V
Input impedance of ALC_IN pin		R_{ALC_IN}	111		189	kΩ
Power supply rejection ration of the transmitter section		$PSRR_{TX\_OUT}$	10 (Note 7)		35 (Note 8)	dB

4. This parameter will not be tested in production.
5. This delay corresponds to the internal transmit path delay and will be defined during design.
6. Taking into account the resolution of the DDS and an accuracy of 100 ppm of the crystal.
7. A sinusoidal signal of 10 kHz and 100 mVpp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.
8. A sinusoidal signal of 50 Hz and 100 mVpp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.

The LPF filter + amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 11. TRANSMITTER FREQUENCY CHARACTERISTICS

	Attenuation		
Frequency (kHz)	Min	Max	Unit
10	−0.5	0.5	dB
95	−1.3	0.5	dB
130	−4.5	−2.0	dB
165		−3.0	dB
330		−18.0	dB
660		−36.0	dB
1000		−50	dB
2000		−50	dB

4.1.4 Receiver External Parameters: Pin RX_IN, RX_OUT, REF_OUT

Table 12. RECEIVER EXTERNAL PARAMETERS: Pin RX_IN, RX_OUT, REF_OUT

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Input offset voltage 42 dB	AGC gain = 42 dB	$V_{OFFS\_RX\_IN}$			5	mV
Input offset voltage 0 dB	AGC gain = 0 dB	$V_{OFFS\_RX\_IN}$			50	mV
Max. peak input voltage (corresponding to 62.5% of the SD full scale)	AGC gain = 0 dB (Note 9)	$V_{MAX\_RX\_IN}$	0.85		1.15	V_p
Input referred noise of the analog receiver path	AGC gain = 42 dB (Notes 9 and 10)	NF_{RX_IN}			150	$nV/\sqrt{Hz}$
Input leakage current of receiver input		$I_{LE\_RX\_IN}$	−1		1	μA
Max. current delivered by REF_OUT		$I_{Max\_REF\_OUT}$	−300		300	mA
Power supply rejection ratio of the receiver input section	AGC gain = 42 dB (Note 11) AGC gain = 42 dB (Note 12)	$PSRR_{LPF\_OUT}$	10 35			dB
AGC gain step		AGC_{step}	5.7		6.3	dB
AGC range		AGC_{range}	39.9		44.1	dB
Analog ground reference output voltage		V_{REF_OUT}	1.52		1.78	V
Signal to noise ratio at 62.5% of the SD full scale	(Notes 9 and 13)	SN_{AD_OUT}	54			dB
Clipping level at the output of the gain stage (RX_OUT)		$V_{CLIP\_AGC\_IN}$	1.15		1.65	Vp

9. Input at RX_IN, no other external components.
10. Characterization data only. Not tested in production.
11. A sinusoidal signal of 10 kHz and 100 mVpp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT and REF_OUT output is measured to determine the parameter.
12. A sinusoidal signal of 50 Hz and 100 mVpp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT output is measured to determine the parameter.
13. These parameters will be tested in production with an input signal of 95 kHz and 1 Vp by reading out the digital samples at the point AD_OUT with the default settings of T_RX_MOD[7], SDMOD_TYP, DEC_TYP, and COR_F_ENA. The AGC gain is switched to 0 dB.

The receive LPF filter + AGC + low noise amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 13. RECEIVER FREQUENCY CHARACTERISTICS

Frequency (kHz)	Attenuation		Unit
	Min	Max	
10	−0.5	0.5	dB
95	−1.3	0.5	dB
130	−4.5	−2.0	dB
165		−3.0	dB
330		−18.0	dB
660		−36.0	dB
1000		−50	dB
2000		−55	dB

4.1.5 Power−on−Reset (POR)

Table 14. POWER−ON−RESET (POR)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POR threshold		V_{POR}	1.7		2.7	V
Power supply rise time	0 V to 3 V	T_{RPOR}	1			ms

4.1.6 Digital Outputs: TDO, CLK_OUT

Table 15. DIGITAL OUTPUTS: TDO, CLK_OUT

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V
High output voltage	I_{XOUT} = −4 mA	V_{OH}	0.85 V_{DD}			V

4.1.7 Digital Outputs with Open Drains: TX_ENB, TXD

Table 16. DIGITAL OUTPUTS WITH OPEN DRAIN: TX_END, TXD

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V

4.1.8 Digital Inputs: BR0, BR1

Table 17. DIGITAL INPUTS: BR0, BR1

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low input level		V_{IL}			0.2 V_{DD}	V
High input level	0 V to 3 V	V_{IH}	0.8 V_{DD}			V
Input leakage current		I_{LEAK}	−10		10	μA

4.1.9 Digital Inputs with Pulldown: TDI, TMS, TCK, TRSTB, TEST

Table 18. DIGITAL INPUTS WITH PULLDOWN: TDI, TMS, TCK, TRSTB, TEST

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low input level		V_{IL}			0.2 V_{DD}	V
High input level		V_{IH}	0.8 V_{DD}			V
Pulldown resistor	(Note 14)	R_{PU}	7		50	kΩ

14. Measured around a bias point of $V_{DD}/2$.

4.1.10 Digital Schmitt Trigger Inputs: RXD, RESB

Table 19. DIGITAL SCHMITT TRIGGER INPUTS: RXD, RESB

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Rising threshold level		V_{T+}			0.8 V_{DD}	V
Falling threshold level		V_{T-}	0.2 V_{DD}			V
Input leakage current		I_{LEAK}	−10		1−	μA

4.1.11 Current Consumption

Table 20. CURRENT CONSUMPTION

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Current consumption in receive mode	Current through V_{DD} and V_{DDA} (Note 15)	I_{RX}	60		80	mA
Current consumption in transmit mode	Current through V_{DD} and V_{DDA} (Note 15)	I_{TX}	60		80	mA
Current consumption when RESB = 0	Current through V_{DD} and V_{DDA} (Note 15)	I_{RESET}			4	mA

15. CLKARM is < 12 MHz, fCLK = 24 MHz.

4.1.12 Main Modem Characteristics

Table 21. OPERATING CHARACTERISTICS

Parameter	Value	Unit
Positive supply voltage Negative supply voltage	3.0 to 3.6 −0.7 to + 0.3	V V
Max peak output level	1.2	Vp
HD2	−60	dB
HD3	−60	dB
ALC Steps	3	dB
ALC Range	(0 ... −21)	dB
Maximum input signal	1.15	Vp
Input impedance	100	kΩ
Input sensitivity	0.4	mV
AGC steps	6	dB
AGC range	(0 ... +42)	dB
Maximum 50 Hz variation	0, 1	Hz/s
Data rate	300/360 (Note 22) 600/720 (Note 22) 1200/1440 (Note 22) 2400/2880(Note 22)	baud baud baud baud
Programmable carrier (Note 21)		
Frequency band		
Frequency minimum	9	kHz
Frequency maximum	95	kHz
Frequency deviation between pairs	>10	kHz
Dynamic range	40 (Note 16) 60 (Note 17) 80 (Note 18)	dB dB dB
Narrow band interfere BER (Note 19)	10E−5	
Maximum 50 Hz variation	0.1	Hz/s

16. FER = 0%.
17. FER = 0.3%.
18. FER = 8.0%.
19. Signal between −60 dB and 0 dB interference signal level is 30 dB above signal level between 20 kHz and 95 kHz.
20. Input at −40 dB, duty cycle between 10 − 50% pulse noise frequency between 100 to 1000 Hz. BER: Bit error rate FER: Frame error rate (1frame is 288 bits).
21. Carriers frequency is programmable by steps of 10 Hz.
22. 60 Hz mains frequency.

5 INTRODUCTION

5.1 GENERAL DESCRIPTION

The AMIS-49587 is a single chip half duplex S-FSK modem dedicated to power line carrier (PLC) data transmission on low- or medium-voltage power lines. The device offers complete handling of the protocol layers from the physical up to the MAC. AMIS-49587 complies with the CENELEC EN 50065-1 and the IEC 61334-5-1 standards. It operates from a single 3.3 V power supply and is interfaced to the power line by an external power driver and transformer. An internal PLL is locked to the mains frequency and is used to synchronize the data transmission at data rates of 300, 600, 1200 and 2400 baud for a 50Hz mains frequency, or 360, 720, 1440 and 2880 baud for a 60 Hz mains frequency. In both cases this corresponds to 3,6,12 or 24 data bits per half cycle of the mains period.

S-FSK is a modulation and demodulation technique that combines some of the advantages of a classical spread spectrum system (e.g. immunity against narrow band interferers) with the advantages of the classical FSK system (low complexity). The transmitter assigns the space frequency f_S to “data 0” and the mark frequency f_M to “data 1”. The difference between S-FSK and the classical FSK lies in the fact that f_S and f_M are now placed far from each other, making their transmission quality independent from each other (the strengths of the small interferences and the signal attenuation are both independent at the two frequencies). The frequency pairs supported by the AMIS-49587 are in the range of 9-95 kHz with a typical separation of 10 kHz.

The conditioning and conversion of the signal is performed at the analog front-end of the circuit. The further processing of the signal and the handling of the protocol is digital. At the back-end side, the interface to the application is done through a serial interface. The digital processing of the signal is partitioned between hardwired blocks and a microprocessor block. The microprocessor is controlled by firmware. Where timing is most critical, the functions are implemented with dedicated hardware. For the functions where the timing is less critical, typically the higher level functions, the circuit makes use of the ARM 7TDMI microprocessor core.

The processor runs DSP algorithms and, at the same time, handles the communication protocol. The communication protocol, in this application, contains the MAC = Medium Access Control Layer. The program running on the microprocessor is stored into ROM. The working data necessary for the processing is stored in an internal RAM. At the back-end side the link to the application hardware is provided by a Serial Communication Interface (SCI). The SCI is an easy to use serial interface, which allows communication between an external processor used for the application software and the AMIS-49587 modem. The SCI works on two wires: TXD and RXD. Baud rate is programmed by setting 2 bits (BR0, BR1).

Because the low protocol layers are handled in the circuit, the AMIS-49587 provides an innovative architectural split. Thanks to this, the user has the benefit of a higher level interface of the link to the PLC medium. Compared to an interface at the physical level, the AMIS-49587 allows faster development of applications. The user just needs to send the raw data to the AMIS-49587 and no longer has to take care of the protocol detail of the transmission over the specific medium. This last part represents usually 50 percent of the software development costs.

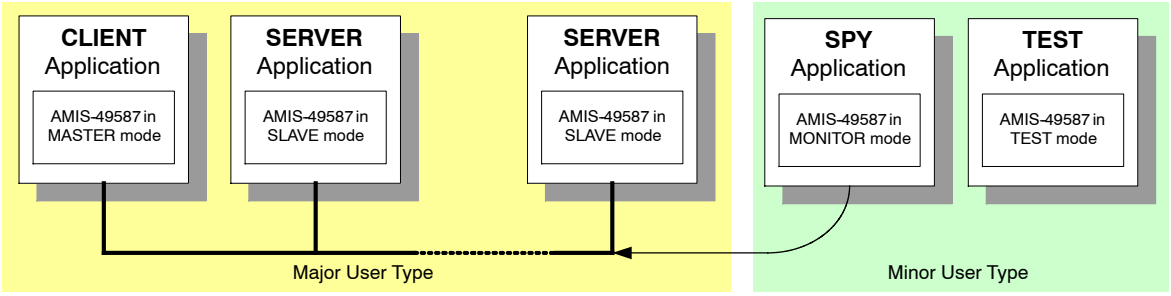


Figure 8. Application Examples

AMIS-49587 intended to connect equipment using Distribution Line Carrier (DLC) communication. It serves two major and two minor types of applications:

- Major types:
  - Master or Client:
    A Master is a client to the data served by one or many slaves on the power line. It collects data from and controls the slave devices. A typical application is a concentrator system.
  - Slave or Server:
    A Slave is a server of the data to the Master. A typical application is an electricity meter equipped with a PLC modem.
- Minor type:
  - Spy or Monitor:
    Spy or Monitor mode is used to only listen to the data that comes across the power line. Only the physical layer frame correctness is checked. When

the frame is correct, it is passed to the external processor.

- Test Mode:
  The Test Mode is used to test the compliance of a PLC modem conforms to CENELEC. EN 50065−1 by a Continuous broadcast of f_S or f_M.

5.2 FUNCTIONAL DESCRIPTION

The block diagram below represents the main functional units of the AMIS−49587:

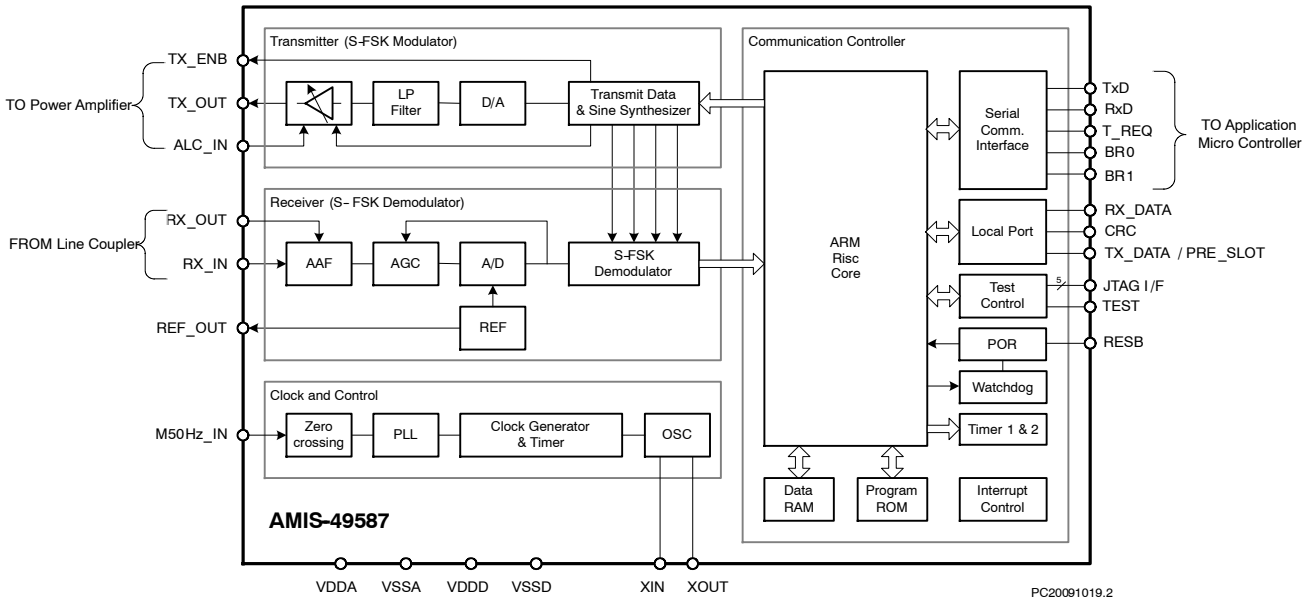


Figure 9. S−FSK Modem AMIS−49587 Block Diagram

5.2.1 Transmitter

The AMIS−49587 Transmitter function block prepares the communication signal which will be sent on the transmitting channel during the transmitting phase. This block is connected to a power amplifier which injects the output signal on the mains through a line−coupler.

5.2.2 Receiver

The analog signal coming from the line−coupler is low pass filtered in order to avoid aliasing during the conversion. Then the level of the signal is automatically adapted by an automatic gain control (AGC) block. This operation maximizes the dynamic range of the incoming signal. The signal is then converted to its digital representation using sigma delta modulation. From then on, the processing of the data is done in a digital way. By using dedicated hardware, a direct quadrature demodulation is performed. The signal demodulated in the base band is then low pass filtered to reduce the noise and reject the image spectrum.

Clock and Control

According to the IEC−61334−5−1 standard, the frame data is transmitted at the zero crossing of the mains voltage. In order to recover the information at the zero crossing, a zero crossing detection of the mains is performed. A phase−locked loop (PLL) structure is used in order to allow a more reliable reconstruction of the synchronization. This PLL permits as well a safer implementation of the ”repetition with credit” function (also known as chorus transmission). The clock generator makes use of a precise quartz oscillator master. The clock signals are then obtained by the use of a programmed division scheme. The support circuits are also contained in this block. The support circuits include the necessary blocks to supply the references voltages for the AD and DA converters, the biasing currents and power supply sense cells to generate the right power off and startup conditions.

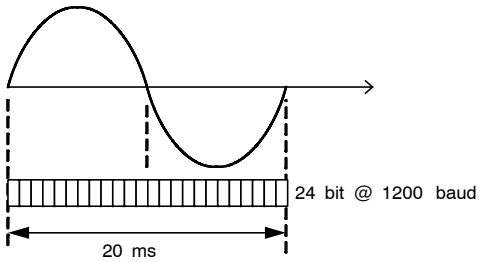


Figure 10. Data Stream is in Sync with Zero Crossings of the Mains (Example for 50 Hz)

5.2.3 Communication Controller

The Communication Controller block includes the micro−processor, its peripherals: RAM, ROM, UART, TIMER, and the Power on reset. The processor uses the ARM Reduced Instruction Set Computer (RISC)

architecture optimized for IO handling. For most of the instructions, the machine is able to perform one instruction per clock cycle. The microcontroller contains the necessary hardware to implement interrupt mechanisms, timers and is able to perform byte multiplication over one instruction cycle. The microcontroller is programmed to handle the physical layer (chip synchronization), and the MAC layer conform to IEC 61334-5-1. The program is stored in a masked ROM. The RAM contains the necessary space to store the working data. The back-end interface is done through the Serial Communication Interface block. This back-end is used for data transmission with the application micro controller (containing the application layer for concentrator, power meter, or other functions) and for the definition of the modem configuration.

5.2.4 Local Port

The controller uses 3 output ports to inform about the actual status of the PLC communication. RX_DATA indicates if Receiving is in progress, or if AMIS-49587 is waiting for synchronization, or of it configures. CRC indicates if the received frames are valid (CRC = OK). TX_DATA / PRE_SLOT is the output for either the transmitting data (TX_DATA) or a synchronization signal with the time-slots (PRE_SLOT).

5.2.5 Serial Communication Interface

The local communication is a half duplex asynchronous serial link using a receiving input (RxD) and a transmitting output (TxD). The input port T_REQ is used to manage the local communication with the application micro controller and the baud rate can be selected depending on the status of two inputs BR0, BR1. These two inputs are taken in account after an AMIS-49587 reset. Thus when the application micro controller wants to change the baud rate, it has to set the two inputs and then provoke a reset.

6 DETAILED HARDWARE DESCRIPTION

6.1 CLOCK AND CONTROL

According to the IEC 61334-5-1 standard, the frame data is transmitted at the zero crossing of the mains voltage. In order to recover the information at the zero crossing, a zero crossing detection of the mains is performed. A phase-locked loop (PLL) structure is used in order to allow a more reliable reconstruction of the synchronization. The output of this block is the clock signal CHIP_CLK, 8 times over sampled with the bit rate. The oscillator makes use of a precise 24 MHz quartz. This clock signal together with CHIP_CLK is fed into the Clock Generator and time block. Here several internal clock signals and timings are obtained by the use of a programmed division scheme.

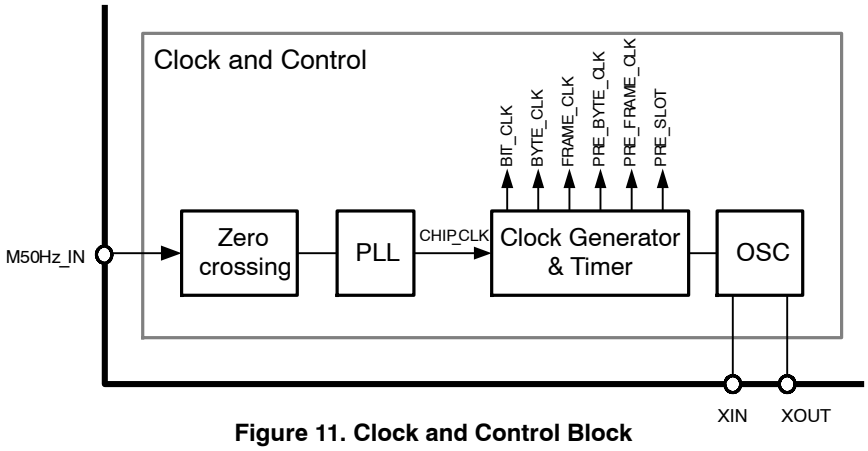


Figure 11. Clock and Control Block

6.1.1 Zero Crossing Detector

M50HZ_IN is the mains frequency analog input pin. The signal is used to detect the zero crossing of the 50 or 60 Hz sine wave. This information is used, after filtering with the internal PLL, to synchronize frames with the mains frequency. In case of direct connection to the mains it is advised to use a series resistor of 1 MΩ in combination with two external clamp diodes in order to limit the current flowing through the internal protection diodes.

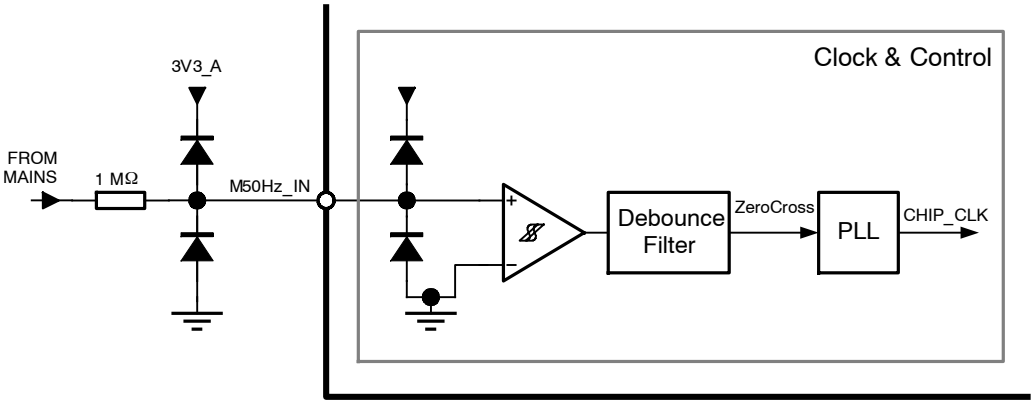


Figure 12. Zero Cross Detector with Falling Edge Debouncer

The zero crossing detector output is logic zero when the input is lower than the falling threshold level and a logic one when the input is higher than the rising threshold level. The falling edges of the output of the zero crossing detector are de-bounced by a period between 0.5 ms and 1 ms. The Rising edges are not de-bounced.

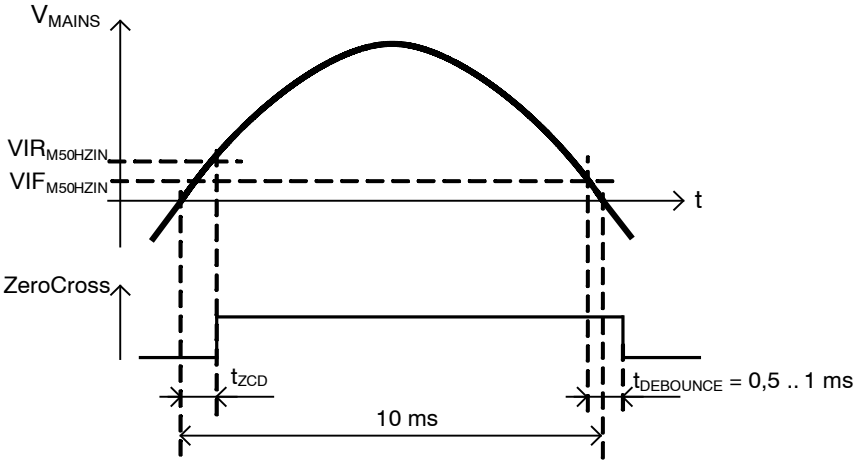


Figure 13. Zero Cross Detector Signals and Timing (Example for 50 Hz)

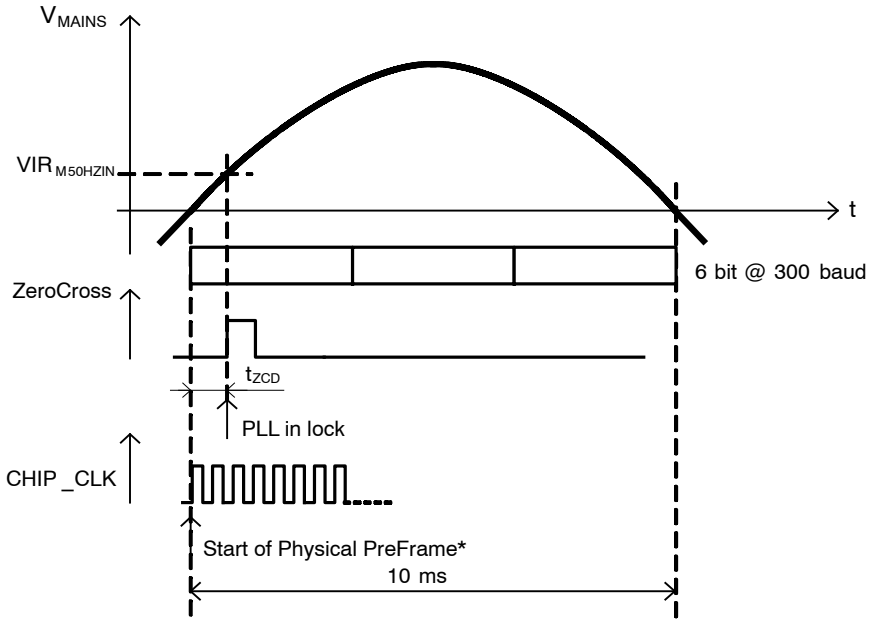
6.1.2 50/60 Hz PLL

The output of the zero crossing detector is used as an input for a PLL. The PLL generates the clock CHIP_CLK which is 8 times the bit rate and which is in phase with the rising edge crossings. The PLL locks on the zero crossing from negative to positive phase. The bit rate is always an even multiple of the mains frequency, so following combinations are possible:

Table 22. CHIP_CLK IN FUNCTION OF SELECTED BAUD RATE AND MAINS FREQUENCY

BAUD[1:0]	MAINS_FREQ	Baudrate	CHIP_CLK
00	50 Hz	300	2400 Hz
01		600	4800 Hz
10		1200	9600Hz
11		2400	19200 Hz
00	60 Hz	360	2880 Hz
01		720	5760 Hz
10		1440	11520Hz
11		2880	23040 Hz

In case no zero crossings are detected the PLL freezes its internal timers in order to maintain the CHIP_CLK timing.



*The start of the Physical Subframe is shifted back with R_ZC_ADJUST[7:0] x 26 μS = t_{ZCD} to compensate for the zero cross delay

Figure 14. Zero Cross Adjustment to Compensate for Zero Cross Delay (Example for 50 Hz)

The phase difference between the zero crossing of the mains and CHIP_CLK can be tuned. This opens the possibility to compensate for external delay t_{ZCD}(e.g. opto coupler) and for the 1.9 V positive threshold $VIR_{M50HZIN}$ of the zero crossing detector. This is done by pre-loading the PLL counter with a number value stored in register R_ZC_ADJUST[7:0]. The adjustment period or granularity is 26 μs. The maximum adjustment is 255 x 26 μs = 6.6 ms which corresponds with 1/3rd of the mains sine period.

Table 23. ZERO CROSS DELAY COMPENSATION

R_ZC_ADJUST[7:0]	Compensation
0000 0000	0 μs
0000 0001	26 μs
0000 0010	52 μs
0000 0011	78 μs
…	…
1111 1101	6589 μs
1111 1110	6615 μs
1111 1111	6641 μs

6.1.3 Oscillator

The oscillator works with a standard parallel resonance crystal of 24 MHz. XIN is the input to the oscillator inverter gain stage and XOUT is the output.

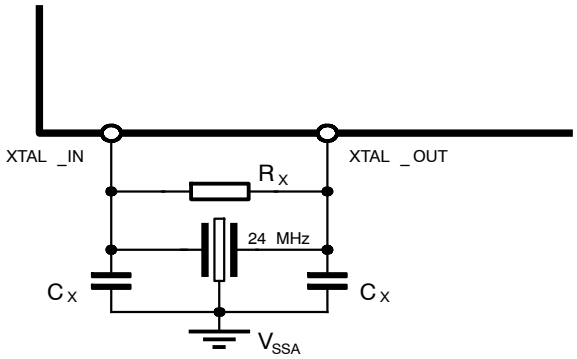


Figure 15. Placement of the Capacitors and Crystal with Clock Signal Generated Internally

For correct functionality the external circuit illustrated in Figure 15 must be connected to the oscillator pins. For a crystal requiring a parallel capacitance of 20 pF C_X must be around 30 pF. (Values of capacitors are indicative only and are given by the crystal manufacturer). To guarantee startup the series loss resistance of the crystal must be smaller than 80 Ω. A parallel resistor R_X = 1 MΩ is recommended to improve the clock symmetry.

The oscillator output f_{CLK} = 24 MHz is the base frequency for the complete IC. The clock frequency for the ARM $f_{ARM} = f_{CLK}$. The clock for the transmitter, f_{TX_CLK} is equal to f_{CLK} / 2 or 12 MHz. All the transmitter internal clock signals will be derived from f_{TX_CLK}. The clock for the receiver, f_{RX_CLK} is equal to f_{CLK} / 4 or 6 MHz. All the receiver internal clock signals will be derived from f_{RX_CLK}.

6.1.4 Clock Generator and Timer

The CHIP_CLK and f_{CLK} are used to generate a number of timing signals used for the synchronization and interrupt generation. The timing generation has a fixed repetition rate which corresponds to the length of a physical subframe. (see paragraph Send and Receive network data).

The timing generator is the same for transmit and receive mode. When AMIS−49587 switches from receive to transmit and back from transmit to receive, the R_CHIP_CNT counter value is maintained. As a result all timing signals for receive and transmit have the same relative timing. The following timing signals are defined as:

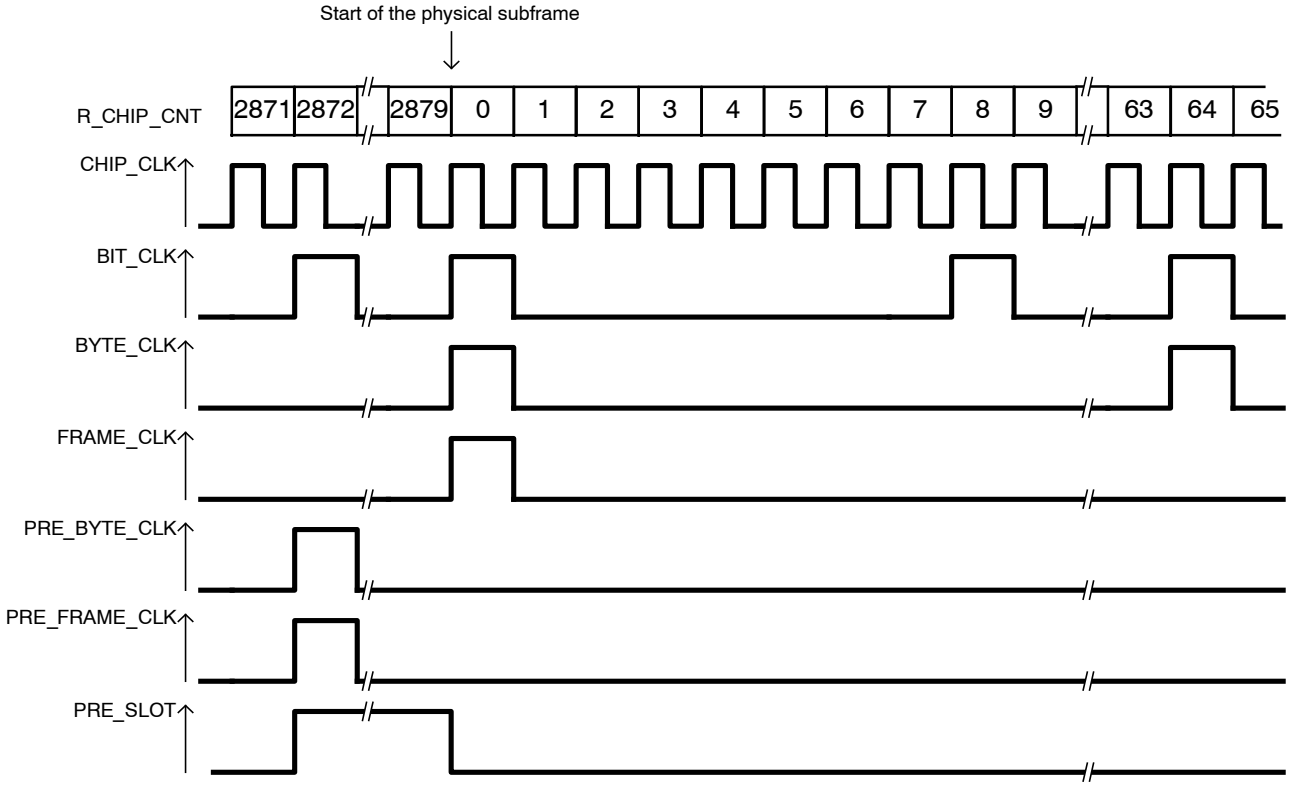


Figure 16. Timing Signals

CHIP_CLK is the output of the PLL and 8 times the bit rate on the physical interface. See also paragraph 50/60 Hz PLL
BIT_CLK is active at counter values 0,8,16, .. 2872 and inactive at all other counter values. This signal is used to indicate the transmission of a new bit.
BYTE_CLK is active at counter values 0,64,128, .. 2816 and inactive at all other counter values. This signal is used to indicate the transmission of a new byte.
FRAME_CLK is active at counter values 0 and inactive at all other counter values. This signal is used to indicate the transmission or reception of a new frame.
PRE_BYTE_CLK is a signal which is 8 CHIP_CLK sooner than BYTE_CLK. This signal is used as an interrupt for the internal microcontroller and indicates that a new byte for transmission must be generated.
PRE_FRAME_CLK is a signal which is 8 CHIP_CLK sooner than FRAME_CLK. This signal is used as an interrupt for the internal microcontroller and indicates that a new frame will start at the next FRAME_CLK.
PRE_SLOT is logic 1 between the rising edge of PRE_FRAME_CLK and the rising edge of FRAME_CLK. This signal can be provided at the digital output pin TX_DATA_PRE_SLOT when R_CONF[7] = 0 (See paragraph WriteConfigRequest, field TX_DATA_PRE−SLOT_SEL) and can be used by the external host controller to synchronize its software with the FRAME_CLK of AMIS−49587.

6.2 TRANSMITTER PATH DESCRIPTION (S−FSK MODULATOR)

For the generation of the space and mark frequencies, the direct digital synthesis (DDS) of the sine wave signals is performed under the control of the microprocessor. After a signal conditioning step, a digital to analog conversion is performed. As for the receive path, a sigma delta modulation technique is used. In the analog domain, the signal is low pass filtered, in order to remove the high frequency quantization noise, and passed to the automatic level controller (ACL) block, where the level of the transmitted signal can be adjusted. The determination of the signal level is done through the sense circuitry.

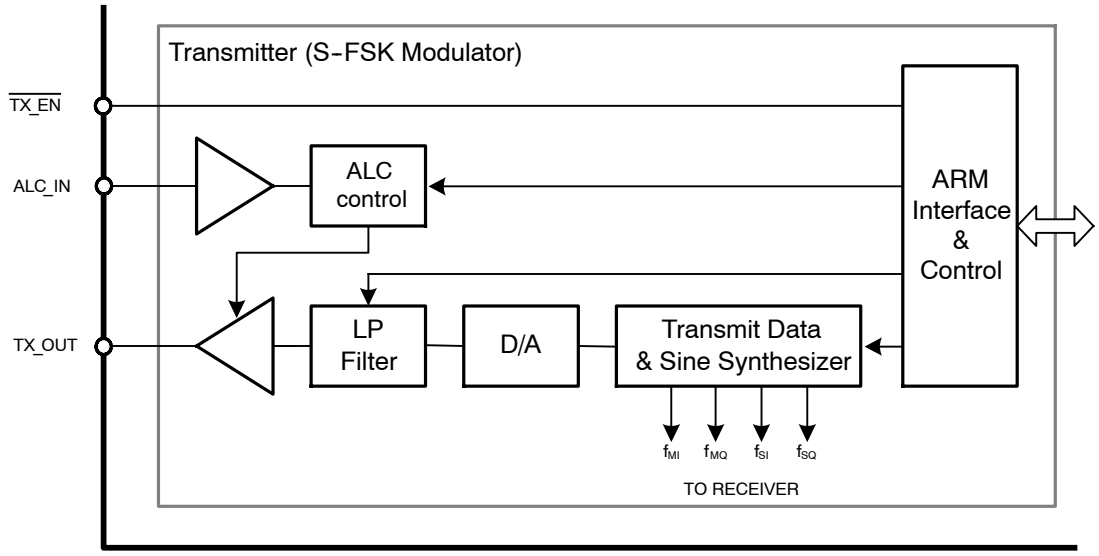


Figure 17. Transmitter Block Diagram

6.2.1 ARM Interface and Control

The interface with the ARM consists in a 8−bit data registers R_TX_DATA, 2 control registers R_TX_CTRL and R_ALC_CTRL, a flag TX_RXB defining transmit and receive and 2 16−bit wide frequency step registers R_FM and R_FS defining f_M (mark frequency = data 1) and f_S (space frequency = data 0). All these registers are memory mapped. Some of them are for internal use only and cannot be accessed by the user.

The processing of the physical frame (preamble, MAC address, CRC) is done by the ARM.

6.2.2 Sine Wave Generator

A sine wave is generated with a direct digital synthesizer DDS. The synthesizer generates in transmission mode a sine wave either for the space frequency (f_S, data 0) or for the mark frequency (f_M, data1). In reception the synthesizer generates the sine and cosine waves for the mixing process, f_{SI}, f_{SQ}, f_{MI}, f_{MQ} (space and mark signals in phase and quadrature). The space and mark frequencies are defined in an individual step 16 bit wide register.

Table 24. FS AND FM STEP REGISTERS

ARM Register	Hard Reset	Soft Reset	Description
R_FS[15:0]	0000h	0000h	Step register for the space frequency f_S
R_FM[15:0]	0000h	0000h	Step register for the mark frequency f_M

The space and mark frequency can be calculated as:

- f_S = R_FS[15:0]_dec x $f_{DDS}/2^{18}$
- f_M = R_FM[15:0]_dec x $f_{DDS}/2^{18}$

Or the content of both R_FS[15:0] and R_FM[15:0] are defined as:

- R_FS[15:0]_dec = Round(2^{18} x f_S/f_{DDS})
- R_FM[15:0]_dec = Round(2^{18} x f_M/f_{DDS})
  Where f_{DDS} = 3 MHz is the direct digital synthesizer clock frequency.

After a hard or soft reset or at the start of the transmission (when TX_RXB goes from 0 to 1) the phase accumulator

must start at it's 0 phase position, corresponding with a 0 V output level. When switching between f_M and f_S the phase accumulator must give a continuous phase and not restart from phase 0.

When AMIS−49587 goes into receive mode (when TX_RXB goes from 1 to 0) the sine wave generator must make sure to complete the active sine period.

The control logic for the transmitter generates a signal TX_ENB to enable the external power amplifier. TX_ENB is 1 when the AMIS−49587 is in receive mode. TX_ENB is 0 when AMIS−49587 is in transmit mode. When going from transmit to receive mode (TX_RXB goes from 1 to 0) the TX_ENB signal is kept active for a short period of t_{dTX_ENB}.

The control logic for the transmitter generates a signal TX_DATA which corresponds to the transmitted S−FSK signal. When transmitting f_M TX_DATA is logic 1. When transmitting f_S TX_DATA is logic 0. When the transmitter is not enabled (TX_RXB = 0) TX_DATA goes to logic 1 at the next BIT_CLK.

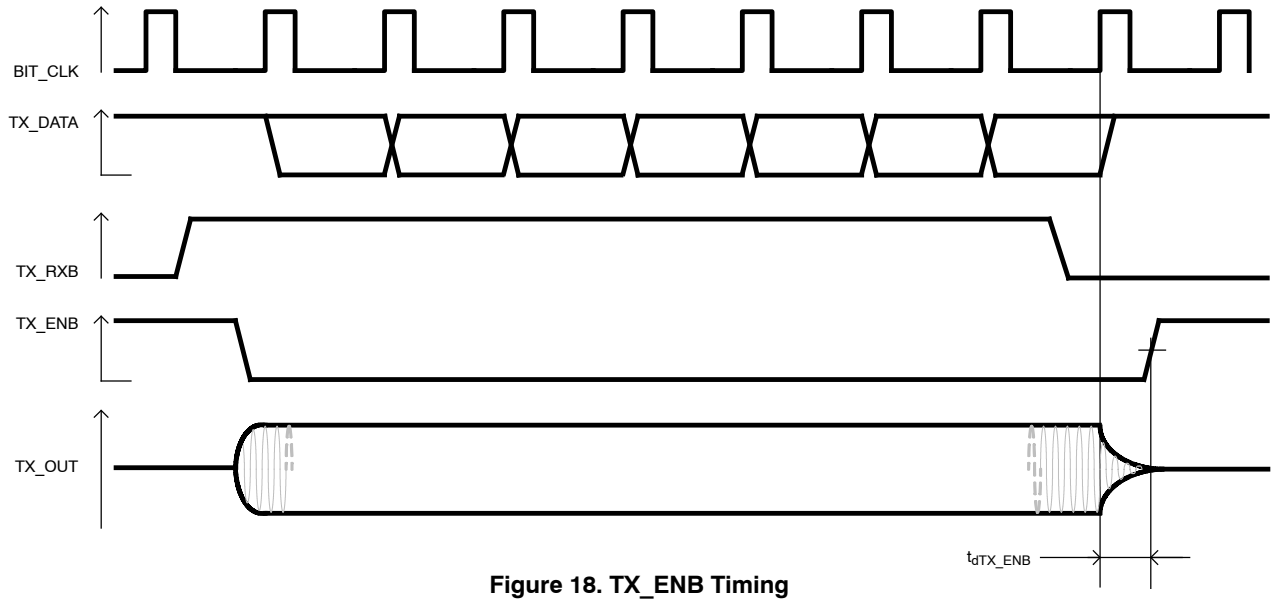


Figure 18. TX_ENB Timing

6.2.3 DA Converter

A digital to analog ΣΔ converter converts the sine wave digital word to a pulse density modulated (PDM) signal. The PDM signal is converted to an analog signal with a first order switched capacitor filter.

6.2.4 Low Pass Filter

A 3rd order continuous time low pass filter in the transmit path filters the quantization noise and noise generated by the ΣΔ DA converter. The low pass filter has a circuit which tunes the RC time constants of the filter towards the process characteristics. The C values for the LPF filter are controlled by the ARM micro controller.

6.2.5 Amplifier with Automatic Level Control (ALC)

The pin ALC_IN is used for level control of the transmitter output level. First a peak detection is done. The peak value is compared to 2 thresholds levels: VTL_{ALC_IN} and VTH_{ALC_IN}. The result of the peak detection is used to control the setting of the level of TX_OUT. The level of TX_OUT can be attenuated in 8 steps of 3 dB typical.

After hard or soft reset the level is set at minimum level (maximum attenuation) When going to reception mode (when TX_RXB goes from 1 to 0) the level is kept in memory so that the next transmit frame starts with the old level. The evaluation of the level is done during 1 CHIP_CLK period.

Depending on the value of peak level on ALC_IN the attenuation is updated:

- $Vp_{ALC\_IN} < VTL_{ALC}$: Increase the level with 1 step
- $VTL_{ALC} \leq Vp_{ALC\_IN} \leq VTH_{ALC}$: Don't change the level
- $Vp_{ALC\_IN} > VTH_{ALC}$: Decrease the level with 1 step

The gain changes in the next CHIP_CLK period.

An evaluation phase and a level adjustment takes 2 CHIP_CLK periods. ALC operation is enabled only during the first 16 CHIP_CLK cycles after a hard or soft reset or after going into transmit mode.

The automatic level control can be disabled by setting register R_ALC_CTRL[3] = 1. In this case the transmitter

output level is fixed to the programmed level in the register R_ALC_CTRL[2:0]. See also paragraph. WriteConfigRequest.

Table 25. FIXED TRANSMITTER OUTPUT ATTENUATION

ALC_CTRL[2:0]	Attenuation
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-15 dB
110	-18 dB
111	-21 dB

Remark: The analog part of AMIS-49587 works with an analogue ground REF_OUT. When connecting AMIS-49587 to external circuitry working with another ground one must make sure to place a decoupling capacitor.

6.3 RECEIVER PATH DESCRIPTION

6.3.1 Receiver Block Diagram

The receiver takes in the analog signal from the line coupler, conditions it and demodulates it in a data-stream to the communication controller. The operation mode and the baud rate are made according to the setting in R_CONF, R_FS and R_FM. The receive signal is applied first to a high pass filter. Therefore AMIS-49587 has a low noise operational amplifier at the input stage which can be used to make a high pass active filter to attenuate the mains frequency. This high pass filter output is followed by a gain stage which is used in an automatic gain control loop. This block also performs a single ended input to differential output conversion. This gain stage is followed by a continuous time low pass filter to limit the bandwidth. A 4th order sigma delta converter converts the analog signal to digital samples. A quadrature demodulation for f_S and f_M is than performed by the ARM micro, as well the handling of the bits and the frames.

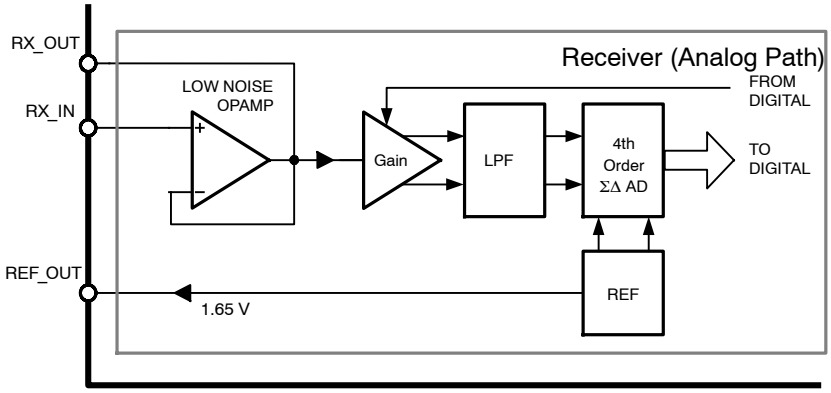


Figure 19. Analog Path of the Receiver

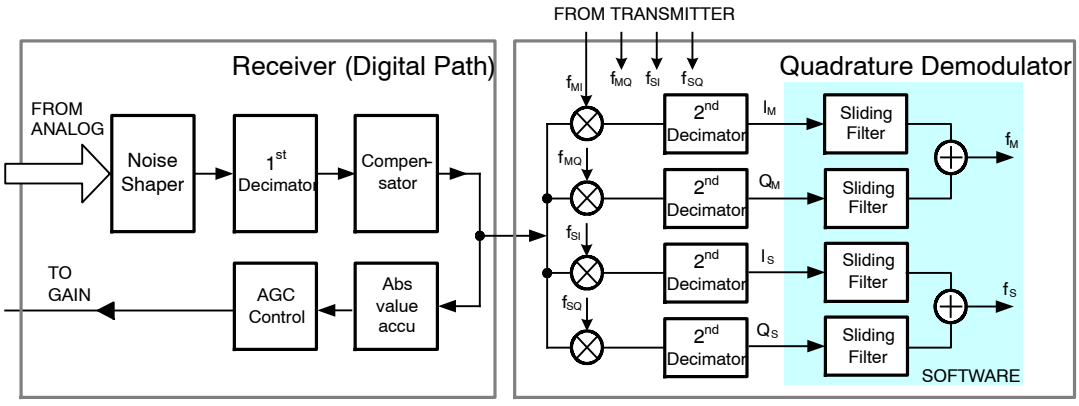


Figure 20. Digital Path of the Receiver ADC and Quadrature Demodulation

6.3.2 50/60 Hz Suppression Filter

AMIS-49587 receiver input provides a low noise input operational amplifier in a follower configuration which can be used to make a 50/60 Hz suppression filter with a minimum number of external components. Pin RX_IN is the positive input and RX_OUT is the output of the input low noise operational amplifier. The pin REF_OUT can be use as an analog ground (1.65 V) for the external circuitry.

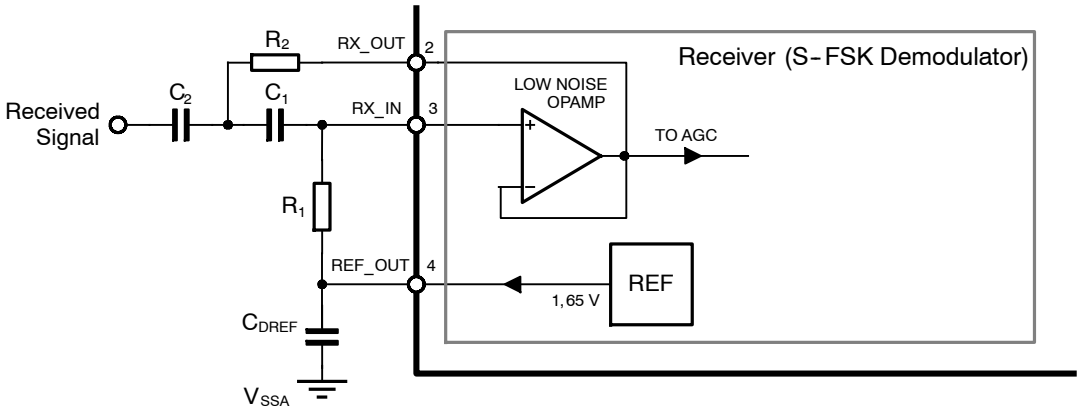


Figure 21. External Component Connection for 50/60 Hz Suppression Filter

RX_IN is the positive analog input pin of the receiver low noise input op-amp. Together with the output RX_OUT an active high pass filter is realized. This filter removes the main frequency (50 Hz or 60 Hz) from the received signal. The filter characteristics are determined by external capacitors and resistors. Typical values are given in Table 26. For these values and after this filter, a typical attenuation of 85 dB at 50 Hz is obtained. Figure 21 represents external components connection. In a typical application the coupling transformer in combination with a parallel capacitance forms a high pass filter with a typical attenuation of 60 dB. The combined effect of the two filters decreases the voltage level of 230 Vrms at the mains frequency well below the sensitivity of the AMIS-49587.

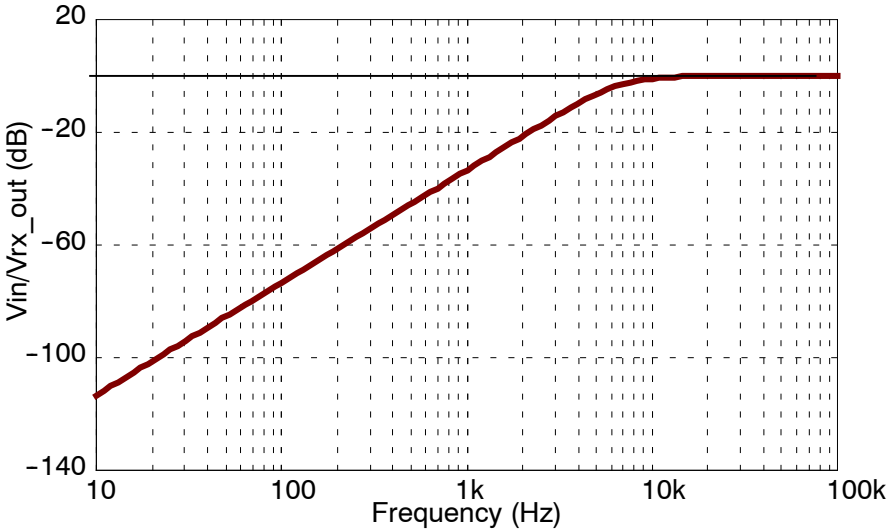


Figure 22. Transfer Function of 50 Hz Suppression Circuit

REF_OUT is the analog output pin which provides the voltage reference used by the A/D converter. This pin must be decoupled from the analog ground by a 1 μF ceramic capacitance (C_{DREF}). It is not allowed to load this pin.

The low noise operational amplifier can be bypassed and powered down by setting the bit R_RX_MOD[7] to 1. In this mode the pin RX_OUT must be used as input of the AGC.

Table 26. VALUE OF THE RESISTORS AND CAPACITORS

Component	Value	Unit
C_1	1.5	nF
C_2	1.5	nF
C_{DREF}	1	μF
R_1	22	kΩ
R_2	11	kΩ

Remark: The analog part of AMIS−49587 is referenced to the internal analog ground REF_OUT = 1.65 V (typical value). If the external circuitry works with a different analogue reference level one must be sure to place a decoupling capacitor.

6.3.3 Auto Gain Control (AGC)

The receiver path has a gain stage which is used for automatic gain control. The gain can be changed in 8 steps of 6 dB. The control of the AGC is done by a digital circuit which measures the signal level after the AD converter, and regulates the average signal in a window around a percentage of the full scale. The AGC works in 2 cycles: a measurement cycle at the rising edge of the CHIP_CLK and an update cycle starting at the next CHIP_CLK.

6.3.4 Low Noise Anti Aliasing Filter

The receiver has a 3rd order continuous time low pass filter in the signal path. This filter is in fact the same block as in the transmit path which can be shared because AMIS−49587 works in half duplex mode. It has a circuit which tunes the RC time constants of the filter towards the process characteristics. The C values for the LPF filter are controlled by the ARM micro controller. When switching between receive and transmit mode (and visa versa) the tune circuit does not need to be updated.

6.3.5 A/D Converter

The output of the low pass filter is input for an analog 4th order sigma−delta converter. The DAC reference levels are supplied from the reference block. The digital output of the converter is fed into a noise shaping circuit blocking the quantization noise from the band of interest, followed by a sinc5 decimation and a compensation step.

6.3.6 Quadrature Demodulator

The quadrature demodulation block takes the AD signal and mixes it with the in−phase and quadrature phase of the f_S and f_M carrier frequencies. After a low pass filter and rectification the mixer output signals are further processed in software. There the accumulation over a period of CHIP_CLK is done which results in the discrimination of data 0 and data 1.

6.4 COMMUNICATION CONTROLLER

The Communication Controller block includes the ARM 32 bit RISC processor operating in the 16−bit Thumb mode, its peripherals: Data RAM, Program ROM, TIMERS 1 & 2, Interrupt Control, TEST Control, Watchdog & Power On Reset (POR), I/O ports and the Serial Communication Interface (SCI). The micro−processor is programmed to handle the physical layer (chip synchronization), and the MAC layer conform to IEC 61334−5−1. The program is stored in a masked ROM. The RAM contains the necessary space to store the working data. The back−end interface is done through the Local Port and Serial Communication Interface block. This back−end is used for data transmission with the application micro controller (containing the application layer for concentrator, power meter, or other functions) and for the definition of the modem configuration.

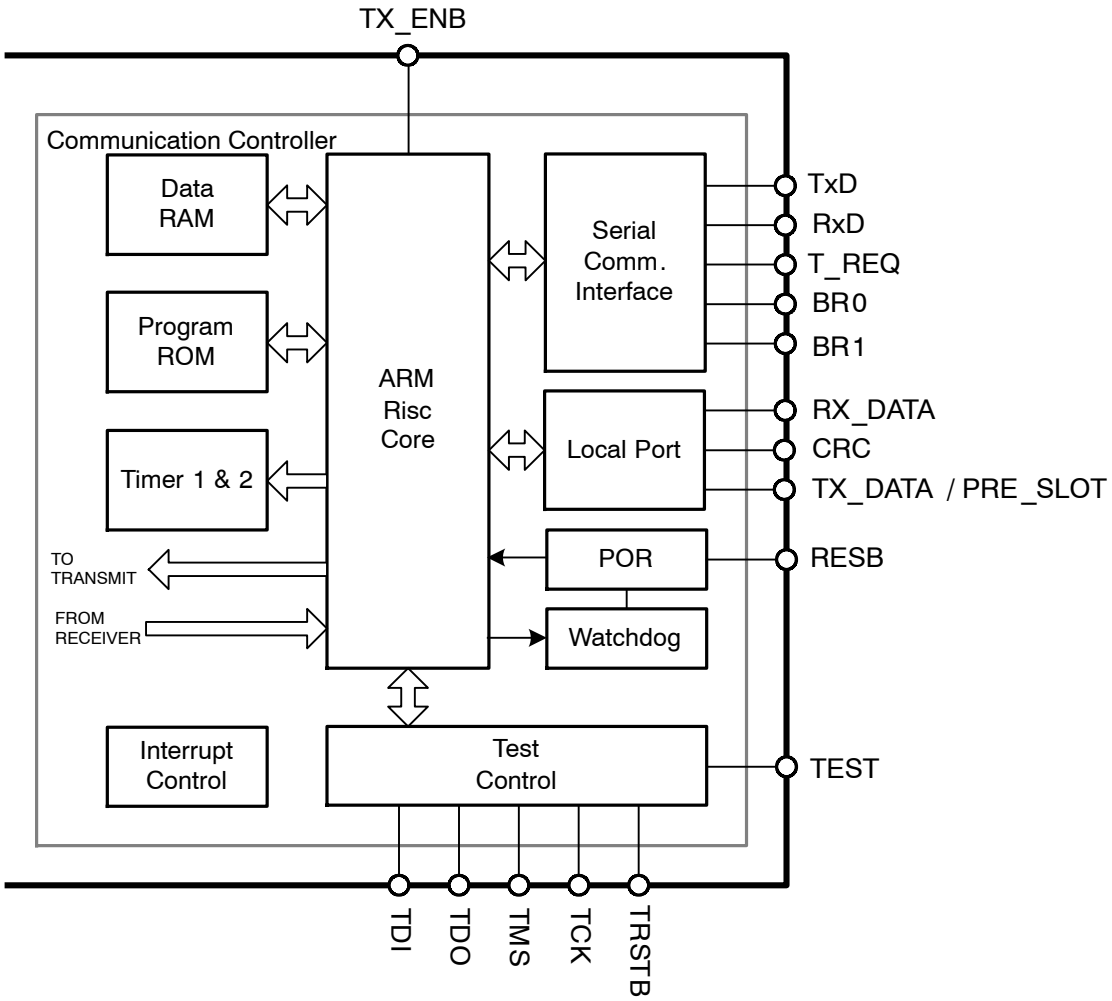


Figure 23. Communication Controller

6.4.1 Local Port

The controller uses 3 output ports to inform the actual status of the PLC communication. RX_DATA indicates if AMIS-49587 is waiting for its configuration, if it is in research of synchronization, or if it is receiving data. CRC indicates if the received frames are valid: the cyclic redundancy code (CRC) is correct. TX_DATA/PRE_SLOT is the output for either the transmitting data (TX_DATA) or a synchronization signal with the time-slots (PRE_SLOT).

Table 27. OVERVIEW FUNCTIONALITY LOCAL PORT

Port	Function	Value	Explanation	Remark
RX_DATA	Data reception	10 Hz	Waiting for configuration	Output is oscillating
		0	After Synchro Confirm Time−out	
		1	Research of synchronization	
CRC	CRC OK	0		
		1	During the pause between 2 timeslots when a correct frame is received	See paragraph Send and Receive Network Data with the AMIS−49587
TX_DATA / PRE_SLOT	TX_DATA	0	Transmit of f_S	R_CONF[7] = 1
		1	Transmit of f_M	
	PRE_SLOT	0	See Figure 16: Timing Signals	R_CONF[7] = 0
		1	See Figure 16: Timing Signals	

6.4.2 Serial Communication Interface (SCI)

The Serial Communication Interface allows asynchronous communication. It can communicate with a UART = Universal Asynchronous Receiver Transmitter, ACIA = Asynchronous Communication Interface Adapter and all other chips that employ standard asynchronous serial communication. The serial communication interface has following characteristics:

- Half duplex.
- Standard NRZ format.
- Start bit, 8 data bits and 1 stop bit.
- Hardware programmable baud−rate (4800, 9600, 19200 and 38400 baud).
- 0−5 V levels with open drain for TxD.
- 0−5 V levels for RxD and T_REQ.

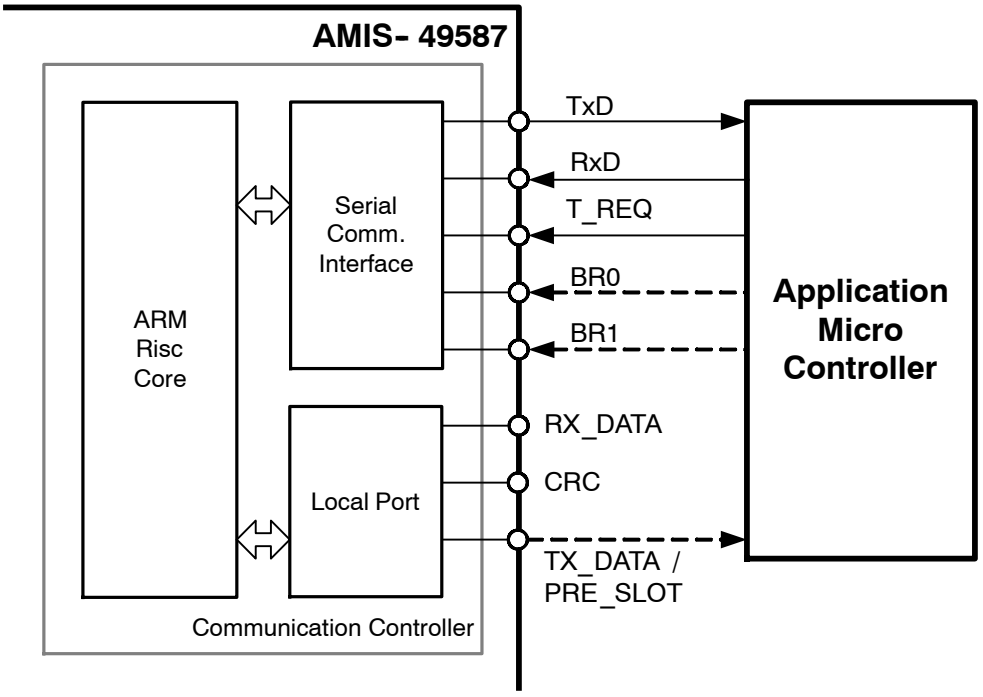


Figure 24. Connection to the Application Microcontroller

6.4.3 Serial Communication Interface Physical Layer Description

The following pins control the serial communication interface.

TXD: Transmit data output.
It is the data output of the AMIS-49587 and the input of the application micro controller.

RXD: Receive data input.
It is the data input of the AMIS-49587 and the output of the application micro controller.

T_REQ:Transmit Request input
Request for data transmission received from the application micro controller.

BR0, BR1: Baud rate selection inputs.
These pins are externally strapped to a value or controlled by the external application micro controller.

Table 28. BR1, BR0 BAUD RATES

BR1	BR0	SCI Baud Rate
0	0	4800
0	1	9600
1	0	19200
1	1	38400

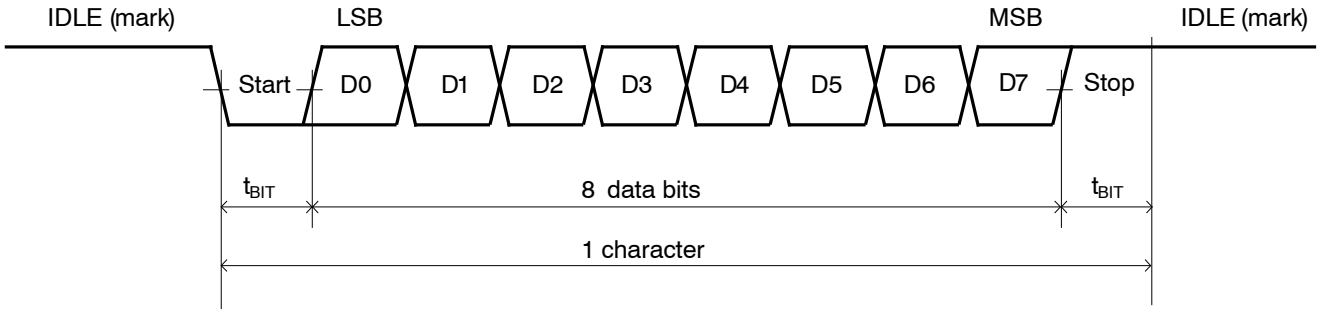


Figure 25. Data Format

6.4.4 Arbitration and Transfer

In order to avoid collisions between the data sent by the AMIS-49587 and the application micro controller, the AMIS-49587 is chosen as the transmitting controller. This means that when there is no local transfer, the AMIS-49587 can initiate a local communication without taking account of the application micro controller state. On the other hand, when the application micro controller wants to send data (using a local frame), it must first send a request for communication through the local input port named T_REQ (Transmitting Request). Then the AMIS-49587 answers with a status message.

6.4.5 Transfer from Application Microcontroller to AMIS-49587

When the application micro controller wants to initiate a local transfer, it must pull down the T_REQ signal. The AMIS-49587 answers within the t_{POLL} delay with the status message in which the application micro controller can read if the communication channel is available. If the communication is possible, the application micro controller can start to send its local frame within the t_{SR} delay. It should pull up the T_REQ signal as soon as the first character (STX) has been sent. If the beginning of the local frame is not received before the t_{SR} delay was issued, the AMIS-49587 ignores the local frame. At the end of the data reception sent by the application micro controller on the RxD line, the AMIS-49587 sends a byte on the TxD line in order to inform about the status of the transmitting <ACK> (=0x06) or <NAK> (=0x15).

Remark: If the application micro controller only wants to know the state of the AMIS-49587, it has just to pull up the T_REQ signal after the reception of the status message.

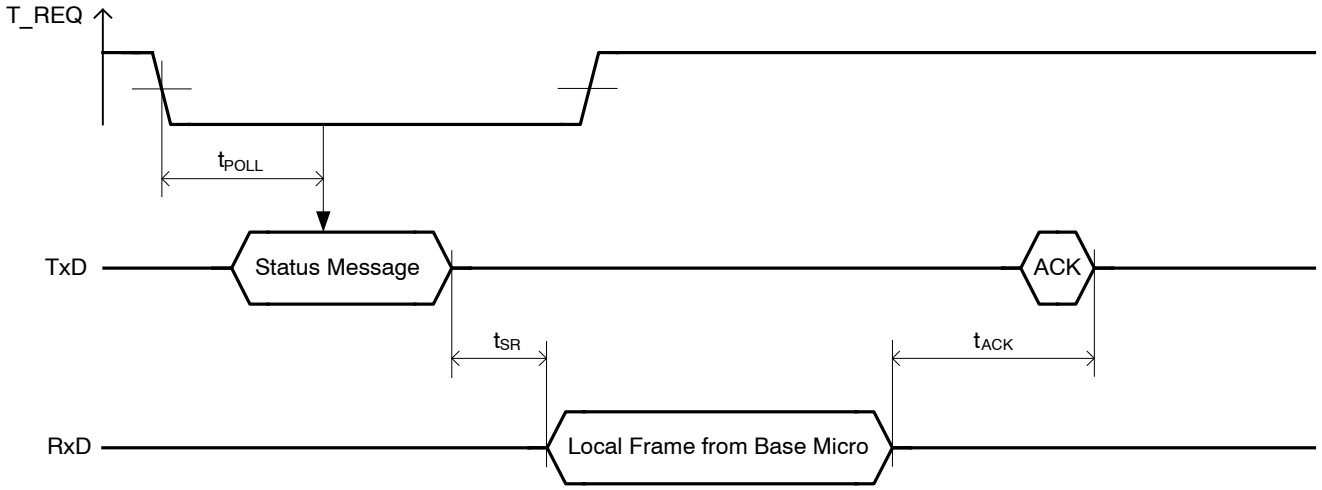


Figure 26. Transfer from Application Microcontroller to AMIS-49587

If the length and the checksum of the local frame are both correct, the AMIS-49587 acknowledges with an <ACK> character. In other cases, it answers with a <NAK> character. In case of <NAK> response, or no acknowledgement from AMIS-49587 in the t_{ACK} time-out, a complete sequence must be restarted to repeat the frame.

6.4.6 Transfer from AMIS-49587 to Application Microcontroller

When the AMIS-49587 wants to send a frame, it can directly send it without any previous request.

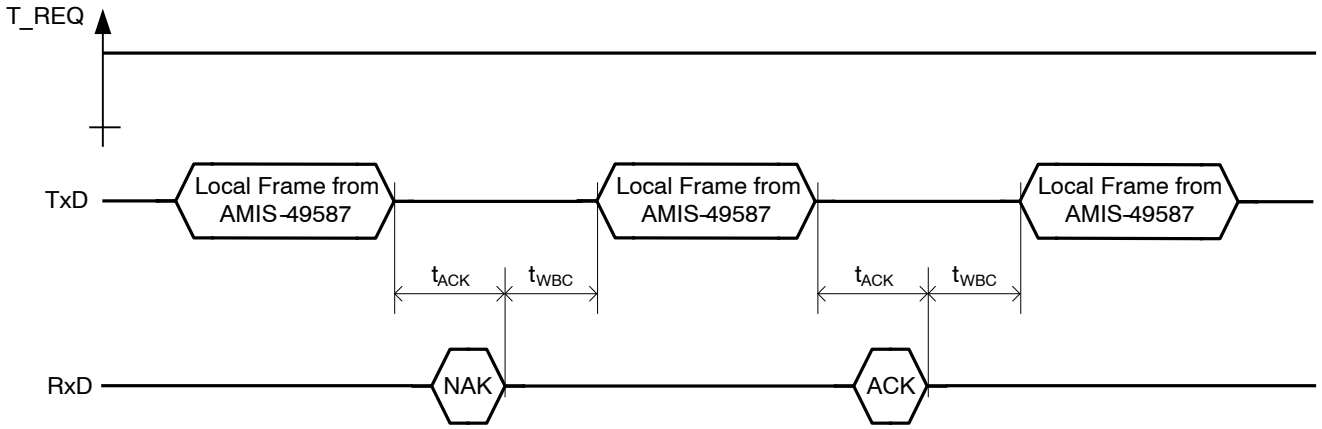


Figure 27. Transfer from AMIS-49587 to Application Microcontroller

If the length and the checksum of the local frame are both correct, the application micro controller acknowledges with an <ACK> character. In other cases, it answers with a <NAK> character. In case of <NAK> response from the Application micro controller, the AMIS-49587 will repeat the frame only once after a delay corresponding to t_{WBC} (Wait Before Continue). A non response from the application micro controller or a framing error when an <ACK> character is awaited is considered as an acknowledgment.

6.4.7 Character Time-out in Reception

The time between two consecutive characters in a local frame should not exceed t_{IC} (Time-out Inter Character):

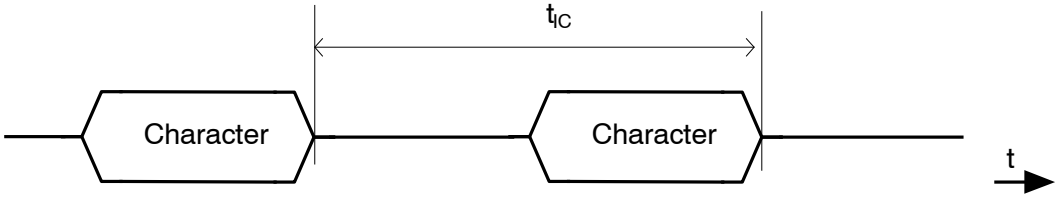


Figure 28. Character Time-out

After this delay, the frame reception is finished. If the length and the checksum are both correct, the local frame is taken in account otherwise all previous characters are discarded. The time out Inter Character (t_{IC}) is set by default at 10 ms after a reset. The time out Inter character (t_{IC}) is modified by the bit 7 of repeater parameter in the configuration frame:

- bit 7 = 1 −> the t_{IC} value is constant at 10 ms,
- bit 7 = 0 −> the t_{IC} value represents 5 characters depending on the communication speed (defined by two local input ports BR0 and BR1).

See Table 29: Timings for Time−out Values.

Table 29. TIME-OUT VALUES

Time-out	Meaning		Value	
Tpoll	Delay max. awaited by the base micro between the T_REQ pull down and the status message transmission (delay polling)		20 ms	
Tsr	Delay max. awaited by the AMIS−49587 between the end of the status transmitting and the reception of the STX character in the base micro frame (delay status/reception)		200 ms	
Tack	Delay max. awaited by either the AMIS−49587 or the base micro between the end of a transmitting and the reception of the ACK or NAK character sent by the other (delay ACK).		40 ms	
Twbc	Delay max. awaited by either the AMIS−49587 or the base micro between the end of a reception and the transmission of the next frame (delay waiting before continue).		5 ms	
Tic	Delay max. awaited by either the AMIS 49587 or the base micro between two characters (delay inter characters) Programmable with bit 7 of the repeater parameter in the configuration frame	Bit 7 = 1	10 ms	
		Bit 7 = 0	4800 baud	10 ms
			9600 baud	5 ms
			19200 baud	2.5 ms
			38400 baud	1.25 ms

6.4.8 Watchdog

The watchdog supervises the ARM and in case the firmware doesn't acknowledge at periodic times, a hard reset is generated.

6.4.9 Configuration Registers

A number of configuration registers can be accessed by the user by sending a WriteConfig_Request over the SCI interface. See also paragraph Configuration of the AMIS−49587. An overview of the accessible configuration registers is given below:

R_CONFIG register configures the AMIS_49587 in the correct mode. The R_CONFIG register is controlled by the embedded software and can be accessed via a WriteConfig_Request.

Table 30. R_CONF[9:0] (See Table 41: Configuration Parameters)

ARM Register	Hard Reset	Soft Reset	Description
R_CONF[7]	0	−	TX_DATA_PRE_SLOT_SEL
R_CONF[5:3]	000	−	MODE
R_CONF[2:1]	00	−	BAUDRATE
R_CONF[0]	0	−	MAINS_FREQ

Where:

TX_DATA_PRE_SLOT_SEL:	0:	TX_DATA/PRE_SLOT is PRE_SLOT output pin
	1:	TX_DATA/PRE_SLOT is TX_DATA output pin
MODE:	000:	Initialization
	001:	Master Mode
	010:	Slave Mode
	011:	Reserved
	1xx:	Test Mode
BAUDRATE:	00:	6 data bits per mains period = 300 baud @ 50 Hz
	01:	12 data bits per mains period = 600 baud @ 50 Hz
	10:	24 data bits per mains period = 1200 baud @ 50 Hz

	11:	48 data bits per mains period = 2400 baud @ 50 Hz
MAINS_FREQ:	0:	50 Hz
	1:	60 Hz

R_FS and R_FM step registers are defining the space and mark frequency. Explanation on the values can be found in paragraph Sine wave generator. This register can be accessed via a WriteConfig_Request.

Table 31. FS AND FM STEP REGISTERS (See Table 41: Configuration Parameters)

ARM Register	Hard Reset	Soft Reset	Description
R_FS[15:0]	0000h	0000h	Step register for the space frequency f_S
R_FM[15:0]	0000h	0000h	Step register for the mark frequency f_M

R_ZC_ADJUST register defines the value which is pre-loaded in the PLL counter. This is used to fine tune the phase difference between HIP_CLK, CIP_CLK and the – to + zero crossing of the mains. Explanation on the values can be found in paragraph 50/60 Hz PLL. This register can be accessed via a WriteConfig_Request.

Table 32. ZC_ADJUST REGISTERS (See Table 41: Configuration Parameters)

ARM Register	Hard Reset	Soft Reset	Description
R_ZC_ADJUST[7:0]	02h	02h	Fine tuning of phase difference between CHIP_CLK and rising edge of Mains zero crossing

R_ALC_CTRL register enables or disables the Automatic Level Control. In case ALC is disabled the attenuation of the TX output driver is fixed according to the value in R_ALC_CTRL[2:0]. Explanation on the attenuation values can be found in paragraph Amplifier with Automatic Level Control. This register can be accessed via a WriteConfig_Request.

Table 33. ALC_CTRL REGISTERS (See appendix C)

ARM Register	Hard Reset	Soft Reset	Description
R_ALC_CTRL[3:0]	00h	00h	Control register for the automatic level control

Where:

R_ALC_CTRL[3]:	0:	Automatic level control is enabled
	1:	Automatic level control is disabled and attenuation is fixed
R_ALC_CTRL[2:0]:	Fixed attenuation value	

Table 34. FIXED TRANSMITTER OUTPUT ATTENUATION

ALC_CTRL[2:0]	Attenuation
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-15 dB
110	-18 dB
111	-21 dB

6.4.10 Reset and Low Power

AMIS-49587 has 2 reset mode: hard reset and soft reset.

The hard reset initializes the complete IC (hardware and ARM) excluding the data RAM for the ARM. This makes sure that start-up of hardware and ARM is guaranteed. A hard reset is active when pin RESB = 0 or when the power supply $V_{DD} < V_{POR}$ (See Table 14 Power On Reset). When switching on the power supply the output of the crystal oscillator is disable until a few 1000 clock pulses have been detected, this to enable the oscillator to start up.

The soft reset initializes part of the hardware. The soft reset is activated when going into initialization mode for the duration of maximum 1 CHIP_CLK. Initialization mode is entered by R_CONF[5:3] = 000.

The concept of AMIS-49587 has a number of provisions to have low power consumption. When working in transmit mode the analogue receiver path and most of the digital receive parts are disabled. When working in receive mode the analog transmitter and most of the digital transmit parts, except for the sine generation, are disabled.

When the pin RESB = 0 the power consumption is minimal. Only a limited power is necessary to maintain the bias of a minimum number of analog functions and the oscillator cell.

7 DETAILED SOFTWARE DESCRIPTION

Figure 29 depicts a typical PLC network with one master and 2 slaves. Each AMIS−49587 is controlled by an external CPU over a RS232 interface. See paragraph Serial Communication Interface Physical Layer Description for a description on hardware signals and timings.

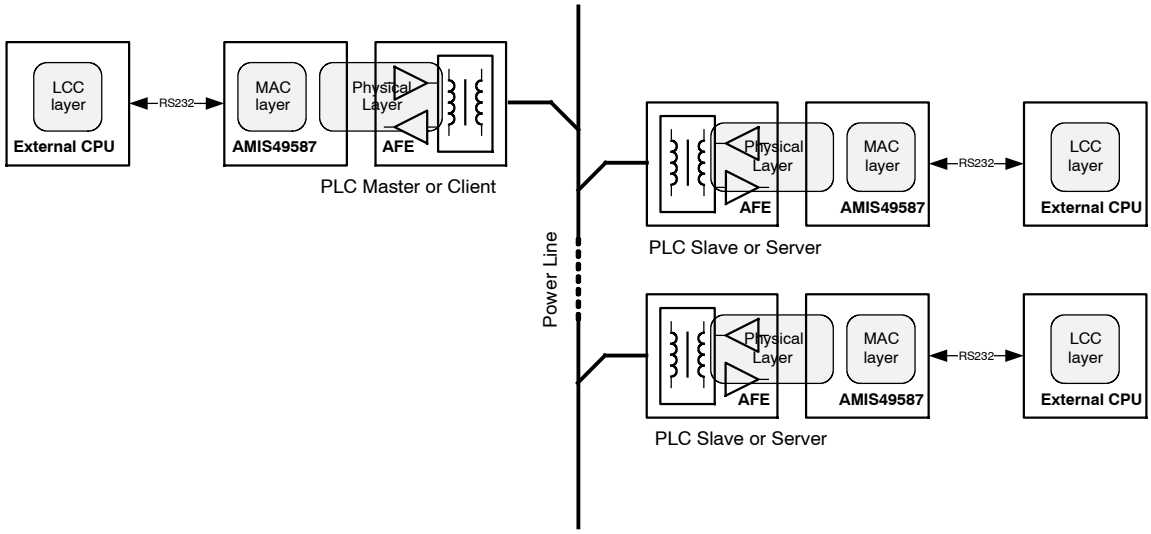


Figure 29. Typical PLC Network Architecture

This document describes how the RS232 frames need to be composed to:

- Get status information from the AMIS−49587
- Configure the AMIS−49587
- Send and Receive network data with the AMIS−49587
- Get performance and data path statistics from AMIS−49587

7.1 CONFIGURE THE AMIS−49587

The AMIS−49587 can operate in different configurations:

- Master or Client configuration: A Master is a client to the data served by one or many slaves on the power line. It collects data from and controls the slave devices.
- Slave or Server configuration: A Slave is a server of the data to the Master.
- Spy or Monitor configuration: Spy or Monitor mode is used to only listen to the data that comes across the power line. Only the physical layer frame correctness is checked (preamble and SSD, see Figure 34 Power Line Data Frame Structure). When the frame is correct, it is passed to the external processor.
- Not set configuration: No valid configuration command has been passed to the AMIS−49587 after reset. No power line communication is possible. This is the state of the AMIS−49587 after a hardware reset or after a reset command has been sent to it.

Each mode has its own configuration parameters and subset of commands.

7.2 OBTAINING STATUS MESSAGES

Opposite to all other commands over the serial interface, the status message is retrieved from the AMIS−49587 by a hardware event only. To get the status message the serial driver on the external CPU needs to pull the T_REQ HW pin low, like described in paragraph Serial Communication Interface Physical Layer Description.

Whenever the external controller sends a command to the AMIS−49587, the T_REQ HW pin should be pulled low to get a new status message from the MODEM. Only when the status message indicates that the buffer is not busy, the command may be send. The AMIS49587 is the master on the serial interface and needs to be queried to get access to the bus.

The format of the status message depends on the active configuration of the AMIS−49587 (not set, slave, master or monitor).

Table 35. SERIAL PORT STATUS FRAME LAYOUT

START	Status_Data

Table 36.

Field	Byte Length	Value	Description
START	1	3Fh	Character (”?”), indicating start of status message.
Status_Data	4	Byte String	4 bytes encoding different status bits

Important: Frame in little endian format (LSByte first)

STATUS MESSAGE IN NOT SET MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
2	Data 1	x	x	x	x	x	x	Not SET	X
3	Data 2	RSV[7:0]							
4	Data 3	SVN[7:4]				SVN[3:0]			

Where:

Not SET	Indicates if AMIS-49587 has received a valid configuration
RSV[7:0]	Reserved
SVN[7:4]	Software Version Number: major release
SVN[3:0]	Software Version Number: minor release
x	Not Used

7.2.1 Status Message in SLAVE or SERVER MODE:

STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
2	Data 1	x	x	x	Not LOCKED	NEW	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	DEP[2:0]			MDC[2:0]			REP[1:0]	

Where:

Not LOCKED	Indication if AMIS 4958x is Unlocked
NEW	Indication if AMIS 4958x is New
Not SYNC	Indication of synchronization with mains
Not SET	Indicates if AMIS-49587 has received a valid configuration
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
DEP[2:0]	Delta Electrical Phase
MDC[2:0]	Minimum Delta Credit Value
REP[1:0]	Repeater Mode
x	Not Used

7.2.2 Status Message in MASTER or CLIENT MODE:

STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
2	Data 1	x	x	x	x	x	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	InvalFrCnt[7:0]							

Where:

Not SYNC	Indication of synchronization with mains
Not SET	Indicates if AMIS-49587 has received a valid configuration
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
InvalFrCnt[7:0]	Invalid Frame counter
x	Not Used

7.2.3 Status Message in MONITOR MODE:

STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
2	Data 1	x	x	x	x	x	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	DEP[2:0]			x	x	x	x	x

Where:

Not SYNC	Indication of synchronization with mains
Not SET	Indicates if AMIS-49587 has received a valid configuration
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
DEP[2:0]	Delta Electrical Phase
x	Not Used

7.3 CONFIGURATION OF THE AMIS-49587

The serial port frame format is the same for RX and TX and is different from the status data frames.

Table 37. SERIAL PORT CONFIGURATION AND DATA PATH FRAME LAYOUT

<STX>	Length	Command	User_Data	CHK

Table 38.

Field	Byte Length	Value	Description
<STX>	1	02h	Start of text delimiter
Length	1	03h .. 250	Length of the Command, User_Data fields and CHK.
Command	1	00h .. FEh	Command code
User_Data	0 .. 247	Byte String	Zero to 247 data bytes.
CHK	2	0000h .. 65535	The checksum of the local frame is the result of the addition of the elements of the frame, from length up to the last UserData byte, or up to the Command byte if there is no UserData byte. The CHK is sent with LSB first.

Important: Frame in little endian format (LSByte first)

Table 39. SUMMARY OF FRAME DELIMITERS

Character	Definition	ASCII Code
<STX>	Start of text; first char of frame	02h
<ACK>	Acknowledgment	06h
<NAK>	Non Acknowledgment	15h
<?>	Start of Status Message	3Fh

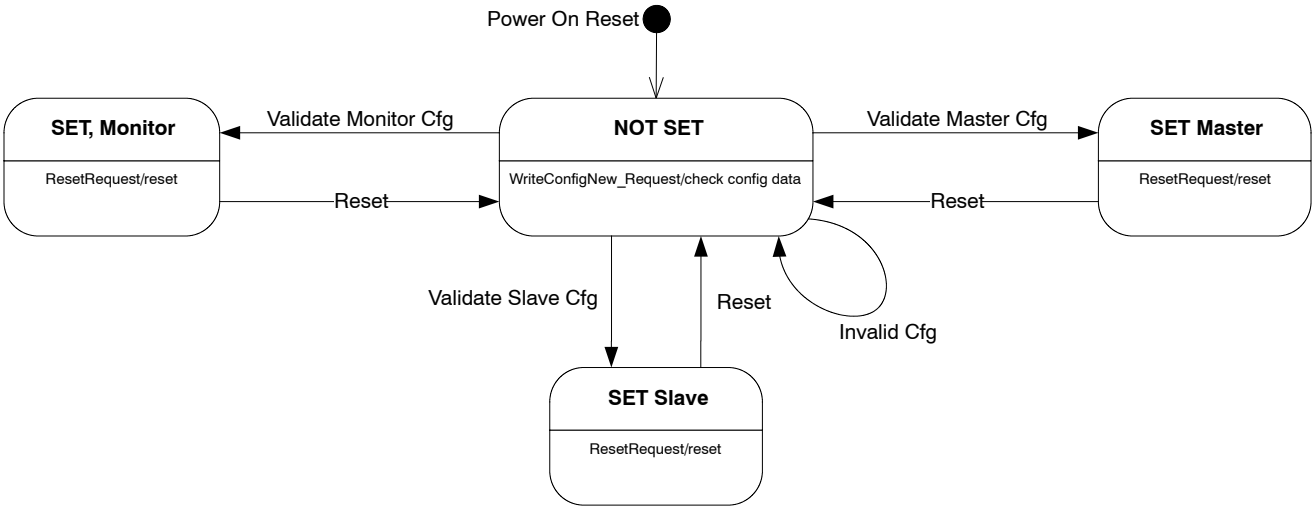


Figure 30. PLC MODEM State Diagram

Table 40. CONFIGURATION COMMANDS AND RESPONSES

Command	Unsolicited*	Initiator	Valid Command in Mode:	Code
Reset_Request	no	Application micro controller ()	Master / Slave / Monitor/ Not Set	21h
WriteConfig_Request	no	Application micro controller (Data_Config)	Master / Slave / Monitor/ Not Set	71h
WriteConfig_Confirm	no	AMIS−49587 (Data_Config_Echo)	Master / Slave / Monitor/ Not Set	72h
WriteConfig_Error	no	AMIS−49587 (Error_Code)	Master / Slave / Monitor/ Not Set	73h
AccessDB_Request	no	Application micro controller (DB_Data_Id)	Master / Slave	41h
AccessDB_Confirm	no	AMIS−49587 (DB_Data_Id_Echo)	Master / Slave	42h
AccessDB_Error	no	AMIS−49587 (Error_Code)	Master / Slave	43h

*An unsolicited message is a message that is originating from the AMIS−49587, based upon an AMIS−49587 internal event. The message is not provoked by a prior command sent by the external processor.

The state diagram in Figure 30 shows how a PLC MODEM can be placed into one of the 4 main modes by issuing a WriteConfig_Request message with accompanying configuration values. Most configuration parameters can be changed after the MODEM is in a ‘set’ mode by the AccessDB_Request message. All settings can be undone by sending the Reset_Request message.

7.3.1 Reset_Request

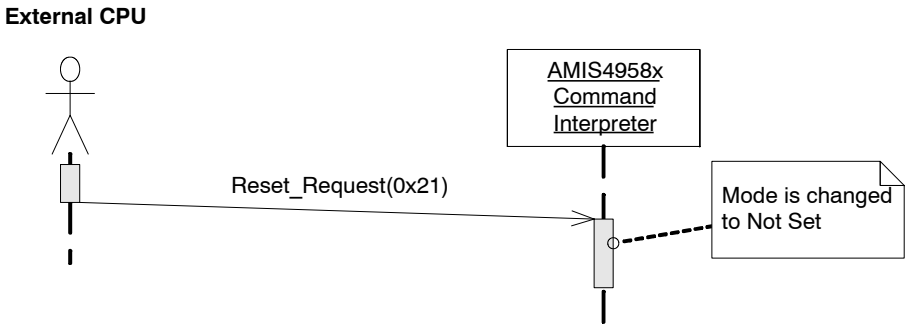


Figure 31. Sequence Diagram for Reset_Request

Use the Reset_Request to bring the MODEM in a ‘NOT SET’ mode. No power line data transmission is possible; it is as if the MODEM comes out of reset. The MODEM does only reply with the <ACK> (=0x06) character, no additional data is sent from the MODEM.

<STX>	0x03 (Length)	0x21 (Reset_Request)	CHK

7.3.2 WriteConfig_Request

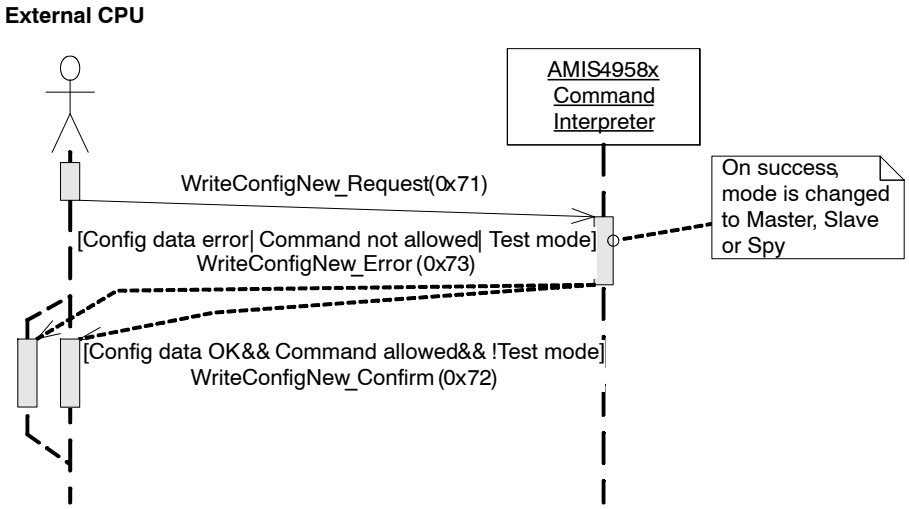


Figure 32. Sequence Diagram for WriteConfig_Request

Command can be issued at any time (If the status message allows it to be send) and will bring the MODEM in a ‘SET’ state if the configuration data is correct. Depending on the configuration data, the final state of the MODEM will be Master, Slave or Monitor.

<STX>	0x26 (Length)	0x71 (WriteConfig_Request)	Data_Config	CHK

With Data_Config, 36 bytes of configuration data as laid out in Tables 41 and 43.

Table 41. CONFIGURATION PARAMETERS

Field	Length	Value	Description
First Initiator MAC Address (FIMA)	2 bytes	0001 to 0FFF	Slave: First value for Initiator MAC address
		XXXX	Master & Monitor: don’t care
Last Initiator MAC Address (LIMA)	2 bytes	0001 to 0FFF	Slave: Last value for Initiator MAC address
		XXXX	Master & Monitor: don’t care
Local MAC Address	2 bytes	0FFE or	Slave Mode: New
		0001 to (FIMA−1) FIMA to LIMA	Slave (Registered) Master
		XXXX	Monitor
Active Initiator Address	2 bytes	0000	Master, Slave (unlocked)
		FIMA to LIMA	Slave (locked on an initiator)
		XXXX	Monitor
Time−out−synchro−confirm	2 bytes	0000 to FFFF	Slave: In seconds. (Not used in Master mode)
Time−out−frame−not−ok	2 bytes	0000 to FFFF	Slave: In seconds (Not used in Master mode)
Time−out−not−addressed	2 bytes	0000 to FFFF	Slave: In minutes (Not used in Master & Monitor mode)
		XXXX	Monitor: Don’t care
Mac−group−addresses	10 bytes	0000 to 0FFF	Slave: 5 MAC group addresses (Not used in Master mode)
Fs	2 bytes	0000 to FFFF	Step Register for the Space Frequency Fs
Fm	2 bytes	0000 to FFFF	Step Register for the Mark Frequency Fm
R_ZC_ADJUST	1 byte	00 to FF	Value according to the voltage level of the 50 Hz information for the input of the PLL.

Table 41. CONFIGURATION PARAMETERS

Field	Length	Value	Description
NbAlarm	4 bits (b7 to b4)	XXXX	Number of repetitions of a Phy Alarm
		0000	Disable Phy Alarm functionality
R_ALC_CTRL→Value Max_Transmitting_Gain→Value	3 bits (b3 to b1)	XXX	Attenuation value in fixed mode
R_ALC_CTRL→Value Max_Transmitting_Gain→Mode	1 bit (b0)	0	Automatic level control
		1	Fixed mode
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	0	The output pin is the PRE_SLOT signal or Mode = Master
		1	The output pin is the transmitted DATA (for Radio)
Pad	1 bit (b6)	0	This bit is not used (adjust length at 1 byte)
R_CONF→MODE	3 bits (b5 to b3)	001	Master mode for client station
		010	Slave mode for server station
		011	Monitor mode to spy and test of the DLC communication
R_CONF→BAUDRATE	2 bits (b2, b1)	00	300 baud @ 50 Hz or 360 baud @ 60 Hz
		01	600 baud @ 50 Hz or 720 baud @ 60 Hz
		10	1200 baud @ 50 Hz or 1440 baud @ 60 Hz
		11	2400 baud @ 50 Hz or 2880 baud @ 60 Hz
R_CONF→MAINS_FREQ	1 bit (b0)	0	mains frequency = 50 Hz
		1	mains frequency = 60 Hz
Pad	1 bit (b7)	0	This bit is not used (adjust length at 1 byte)
Search method	1 bit (b6)	0	Method V6, favors FSK
		1	Method V3, favors ASK
SINC Filter	1 bit (b5)	0	Disabled
		1	Enabled
SYNCHRO−Type→Mode	1 bit (b4)	0	Must be set to 0 (Synchronization on sub−frame preamble)
SYNCHRO−Bit→Value	3 bits (b3 to b1)	XXX	Synchro−bit value (in chip clock) in fixed mode
SYNCHRO−Bit→Mode	1 bit (b0)	1	Must be set to 1 (Fixed synchro bit)
SearchInitiatorGain or Min−ReceivingGain Mode	1 bit (b7)	1	Search Initiator Gain selected
		0	Min Receiving Gain selected
Search Initiator Gain or Min−Receiving Gain	3 bits (b6 to b4)	XXX	Value of the gain for Intelligent Synchronization or Min Receiving Value Min Gain of reception = (value * 6 db)
Max−Receiving−Gain→Value	3 bits (b3to b1)	XXX	Max Receiving gain value in limited mode Range of reception = (value * 6 db)
Max−Receiving−Gain→Mode	1 bit (b0)	0	Non limited Max−Receiving−Gain
		1	Limited Max−Receiving−Gain
Time out Inter Character TIC	1 bit (b7)	0	Constant of 10 ms
		1	5 characters depending on communication speed
Bad CRC transmitting	1 bit (b6)	0	Disables the transmitting of bad CRC frames
		1	Enables the transmitting of bad CRC frames
		X	Monitor: Don’t care

Table 41. CONFIGURATION PARAMETERS

Field	Length	Value	Description
Pad correcting	1 bit (b5)	0	Enables the Pad correcting
		1	Disables the Pad correcting
		X	Monitor: Don't care
FSK +	1 bit (b4)	0	Disables the improvement of FSK
		1	Enables the improvement of FSK
		X	Slave and Monitor: Don't care
Synchro Master	1 bit (b3)	0	Enables the Master Synchro
		1	Disables the Master synchro
		X	Slave and Monitor: Don't care
Synchro without Gain Min	1 bit (b2)	0	disabled
		1	Enabled
		X	Monitor: Don't care
Repeater	2 bits (b1,b0)	00	Never Repeater or Mode = Maste
		01	Always Repeater
		10	Not Repeater (accept frame ISACall)
		11	Repeater (accept frame ISACall)
		XX	Monitor: Don't care
Time−out−search−initiator	2 bytes	0 to FFFF	In seconds
		XXXX	Master, Monitor: Don't care

23. When a time−out is written with a **0x0000** value using either the WriteConfig_Request or the AccessDB_Request command, this time−out will not be activated.
24. After a AccessDB_Request for either the Time−out−not−addressed or the Time−out−frame−not−ok, the new value is immediately taken in account (the time−out is restarted) except when the local MAC address is NEW and the initiator MAC address is nobody.
25. The envelops are calculated using square root values or absolute values, depending on the baud rate and on the main frequency. The following table describes the different modes:

	300, 600, 1200 bps		**2400 bps**	
	50 Hz	**60 Hz**	**50 Hz**	**60 Hz**
Synchro	Square Root	Square Root	ABS	ABS
Reception	Square Root	Square Root	Square Root	ABS

26. When FSK+ option is enabled, new thresholds are calculated. Than if the two envelops are under the threshold, the envelop which has the smallest gap with his threshold is used to determinate which bit is received. Or, if the two envelops are over the threshold, the envelop which has the biggest gap with his threshold is used.

7.3.3 WriteConfig_Confirm

<STX>	0x26 (Length)	0x72 (WriteConfig_Confirm)	Data_Config_Echo	CHK

When the complete set of configuration parameters has been evaluated and stored by the MODEM, it replies with success and echoes the configuration data for the external processor to see if all parameters are correctly stored.

7.3.4 WriteConfig_Error

<STX>	0x04 (Length)	0x73 (WriteConfig_Error)	Error_Code, Table 43	CHK

An error is raised when the external processor issues a WriteConfig_Request command in which the fields listed in Table 42 are modified with respect to the previously issued WriteConfig_Request command. All other data fields of the WriteConfig_Request may be changed.

Table 42. NON CHANGEABLE PARAMETERS AFTER AMIS 49587 IS SET

Field	Length	Value	Description
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	x	No action
R_CONF→MODE	3 bits (b5 to b3)	xxx	No action
R_CONF→BAUDRATE	2 bits (b2,b1)	xx	No action
R_CONF→MAINS_FREQ	1 bit (b0)	x	No action

Table 43. WriteConfig ERROR CODES

Error Identifier	Error_Code
ERR_UNAVAILABLE_MODE	21h
ERR_ILLEGAL_DATA_COMMAND	22h
ERR_ILLEGAL_LOCAL_MAC_ADR	23h
ERR_ILLEGAL_INITIATOR_MAC_ADR	24h
ERR_UNAVAILABLE_COMMAND	25h

7.3.5 AccessDB_Request

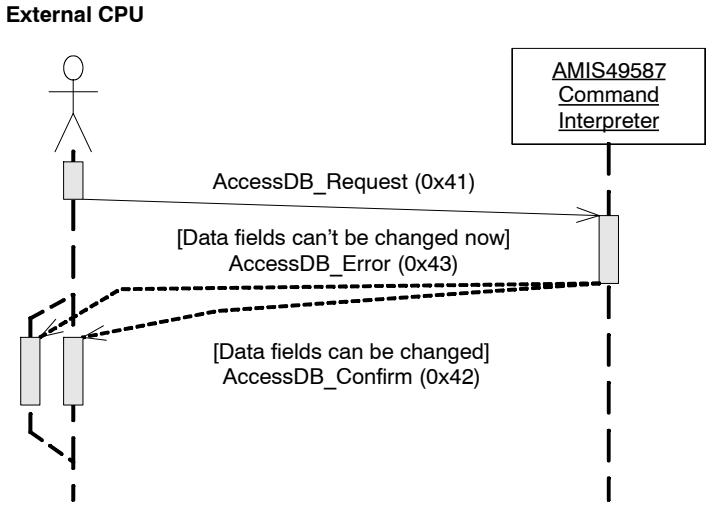


Figure 33. Sequence Diagram for AccessDB_Request

<STX>	0x07 + length of data (Length)	0x41 (AccessDB_Request)	Data Field Identifier (Table44)	Data	CHK

Note that although the name of the AccessDB_Request command suggests only write operations are possible, there are subcommands to read from the data base.

Each AccessDB_Request command is answered by the MODEM with either a AccessDB_Confirm or AccessDB_Error frame.

For better readability, the AccessDB_Confirm frames and explanation are listed here and not grouped into a separate chapter.

Table 44. DATA BASE ENTRIES THAT MODIFY THE CONFIGURATION

Field Name	Ident	Description
FIMA/LIMA	**0000**	Changes the value of First Initiator MAC Address (FIMA) and Last Initiator MAC Address (LIMA)
LocalMacAdd/InitMacAdd	**0001**	Changes the value of Local MAC Address and Active Initiator Address
Time−out−synchro−confirm	**0002**	Changes the value of the TO synchro confirm (In seconds.)
Time−out−frame−not−ok	**0003**	Changes the value of the TO frame not ok (In seconds)
Time−out−not−addressed	**0004**	Changes the value of the TO not addressed (In minutes)
Mac−group−addresses	**0005**	Changes the value of the 5 MAC group addresses
Min−delta−credit	**0007**	Read the value of the Min delta credit and then set to 7
Max_Transmitting_Gain: Mode and Value (R_ALC_CTRL)	**0008**	Changes the mode and the value of the max transmitting gain
SYNCHRO−Type:Mode SYNCHRO−Bit:Value	**0009**	Changes sychro mode and the synchro bit value
Max−Receiving−Gain: Mode and Value	**000A**	Changes the mode and the value of the Max Receiving gain
Repeater	**000B**	Changes the repeater state
Frequency	**000C**	Changes the value of the frequencies Fs and Fm
Time−SearchInitiator	**0011**	Changes the value of the TO Search Initiator (In seconds)
ReadConfig	**0012**	To get an echo of the current configuration of the FPMA
Read SoftVersion	**0013**	Read the version of the FPMA
Min−ReceivingGain Value	**0014**	Changes the value of the Min Receiving Gain
Gain−SearchInitiator	**0015**	Changes the value of the Gain−SearchInitiator

7.3.5.1 FIMA/LIMA

This request is used to modify the value of the FIMA and LIMA addresses. The values of FIMA and LIMA must be in the field 0001 to 0FFF, and must be compatible with current value of LocalMacAdd and InitMacAdd.

Request Format:

<STX>	0x09(Length)	0x41 (AccessDB_Request)	0x0000	FIMA (2 bytes), LIMA (2 bytes)	CHK

Confirm Format:

<STX>	0x09(Length)	0x42 (AccessDB_Confirm)	0x0000	FIMA (2 bytes), LIMA (2 bytes)	CHK

7.3.5.2 LocalMacAdd/InitMacAdd

This request is used to modify the value of the Local Mac Address and the Initiator Mac Address. The values of LocalMacAdd and InitMacAdd must be in the field 0001 to 0FFF, and must be compatible with current value of FIMA and LIMA.

Request Format:

<STX>	0x09(Length)	0x41 (AccessDB_Request)	0x0100	LocalMacAdd (2 bytes), InitMacAdd (2 bytes)	CHK

Confirm Format:

<STX>	0x09(Length)	0x42 (AccessDB_Confirm)	0x0100	LocalMacAdd (2 bytes), InitMacAdd (2 bytes)	CHK

7.3.5.3 TimeoutSynchro

This request is used to modify the value of the timeout synchro confirmation. The Timeout Synchro Confirm is set in seconds.

Request Format:

<STX>	0x07(Length)	0x41 (AccessDB_Request)	0x0200	TO Synchro Confirm (2 bytes)	CHK

Confirm Format:

<STX>	0x07(Length)	0x42 (AccessDB_Confirm)	0x0200	TO Synchro Confirm (2 bytes)	CHK

7.3.5.4 TimeoutNotOK

This request is used to modify the value of the timeout Frame Not OK. The Timeout Frame Not OK is set in seconds.

Request Format:

<STX>	0x07(Length)	0x41 (AccessDB_Request)	0x0300	TO Frame Not OK (2 bytes)	CHK

Confirm Format:

<STX>	0x07(Length)	0x42 (AccessDB_Confirm)	0x0300	TO Frame Not OK (2 bytes)	CHK

7.3.5.5 TimeoutNotAddressed

This request is used to modify the value of the timeout Not Addressed. The Timeout Not Addressed is set in minutes.

Request Format:

<STX>	0x07(Length)	0x41 (AccessDB_Request)	0x0400	TO Not Addressed (2 bytes)	CHK

Confirm Format:

<STX>	0x07(Length)	0x42 (AccessDB_Confirm)	0x0400	TO Not Addressed (2 bytes)	CHK

7.3.5.6 MacGroupAddress

This request is used to modify the values of the 5 Mac Group Addresses. The Mac Group Addresses must be in the field LIMA(not included) to 0FFB.

If the first address of the 5 MacGroup addresses is set to 0xFFF, every frame with destination MAC address in the field LIMA(not included) to 0FFB will be transmitted by the FPMA. This makes it possible to manage more than 5 MAC address of group by the external micro controller.

Request Format:

<STX>	0x0E(Length)	0x41 (AccessDB_Request)	0x0500	Mac Group Addresses (5 *2 bytes)	CHK

Confirm Format:

<STX>	0x0E(Length)	0x42 (AccessDB_Confirm)	0x0500	Mac Group Addresses (5 *2 bytes)	CHK

7.3.5.7 Min Delta Credit

This request is used to read the Min Delta Credit in the AMIS-49587. Once the request sent to the AMIS-49587, the Min Delta Credit is automatically set to 7. The AMIS-49587 answers with the value of the Min Delta Credit (before it was set to 7).

Request Format:

<STX>	0x05(Length)	0x41 (AccessDB_Request)	0x0700	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x0700	Min Delta Credit (1 byte)	CHK

7.3.5.8 MaxTransmittingGain

This request is used to modify the Max Transmitting Gain of the AMIS-49587. The Max Transmitting Gain can be reduced from 0 to 21 dB by step of step 3 dB. The data value for the request is in the field 01 to 0F by step of 2, it indicates an attenuation of ((N - 1) / 2) dB. The data value for the Confirm is in the field 00 to 07, indicating an attenuation of N * 3 dB.

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x0800	Transmitting Attenuation (1 byte)	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x0800	Transmitting Attenuation (1 byte)	CHK

7.3.5.9 MaxReceivingGain

This request is used to modify the Max Receiving Gain of the AMIS-49587. The Max Receiving Gain can be set from 1 to 42 dB by step of step 6 dB, or unlimited. The data value for the request is in the field 01 to 0F by step of 2, it indicates a Max Receiving Gain of ((N - 1) / 2) * 6 dB; or 00, which indicates an unlimited Max Receiving Gain. The data value for the Confirm is in the field 00 to 07, indicating a Max Receiving Gain of (N * 6) dB, or 08, which indicates an unlimited Max Receiving Gain.

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x0A00	Max Receiving Gain (1 byte)	CHK

Confirm Format:

<STX>	0x06(Length)	42h (AccessDB_Confirm)	0x0A00	Max Receiving Gain (1 byte)	CHK

7.3.5.10 Repeater

This request is used to modify the repeater state of the AMIS-49587. The repeater state can be

Repeater: 0x00
No Repeater: 0x01

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x0B00	Repeater State (1 byte)	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x0B00	Repeater State (1 byte)	CHK

7.3.5.11 Frequency

This request is used to modify the values of the frequencies Fs and Fm used for the PLC communication. To calculate the value of the data field, read paragraph Sine Wave generator.

Request Format:

<STX>	0x09(Length)	0x41 (AccessDB_Request)	0x0C00	Fs (2 bytes), Fm (2 bytes)	CHK

Confirm Format:

<STX>	0x09(Length)	0x42 (AccessDB_Confirm)	0x0C00	Fs (2 bytes), Fm (2 bytes)	CHK

7.3.5.12 TimeoutSearchInitiator

This request is used to modify the value of the timeout Search Initiator. The timeout Search Initiator is set in seconds.

Request Format:

<STX>	0x07(Length)	0x41 (AccessDB_Request)	0x1100	TO Search Initiator (2 bytes)	CHK

Confirm Format:

<STX>	0x07(Length)	0x42 (AccessDB_Confirm)	0x1100	TO Search Initiator (2 bytes)	CHK

7.3.5.13 ReadConfig

This request is used to get an echo of the configuration of the AMIS-49587.

Request Format:

<STX>	0x05(Length)	0x41 (AccessDB_Request)	0x1200	CHK

Confirm Format:

<STX>	0x29(Length)	0x42 (AccessDB_Confirm)	0x1200	Current configuration (36 bytes)	CHK

7.3.5.14 Read Version Soft

This request is used to read the soft version of the AMIS-49587.

Request Format:

<STX>	0x05(Length)	0x41 (AccessDB_Request)	0x1300	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x1300	Soft Version (1 byte)	CHK

7.3.5.15 Min−ReceivingGain

This request is used to modify the Min Receiving Gain of the AMIS−49587. The Min Receiving Gain can be set from 1 to 42 dB by step of step 6 dB, or unlimited. The data value for the request is in the field 01 to 0F by step of 2, it indicates a Min Receiving Gain of ((N − 1) / 2) * 6 dB; or 00, which indicates that the Min Receiving Gain is not used. The data value for the Confirm is in the field 00 to 07, indicating a Min Receiving Gain of (N * 6) dB, or 08, which indicates an unlimited Max Receiving Gain.

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x1400	Min Receiving Gain (1 byte)	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x1400	Min Receiving Gain (1 byte)	CHK

7.3.5.16 Gain Search Initiator

This request is used to modify the value of the Gain Search Initiator.

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x1500	Gain Search Initiator (1 byte)	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x1500	Gain Search Initiator (1 byte)	CHK

7.3.6 AccessDB_Confirm

Like already described in AccessDB_Request, on success the MODEM answers with a AccessDB_Confirm frame.

Frame Format:

<STX>	Length	0x42 (AccessDB_Confirm)	DB_Data_Id_Echo	CHK

7.3.7 AccessDB_Error

If any error occurs during AccessDB_Request, the MODEM answers with a AccessDB_Error frame.

Frame Format:

<STX>	Length	0x43 (AccessDB_Error)	Error_Code	CHK

Table 45. AccessDB_Request ERROR CODES

Error Identifier	Error_Code
ERR_UNAVAILABLE_RESOURCE	0x11
ERR_REQUEST_NOT_ALLOWED	0x12
ERR_UNAVAILABLE_MODE	0x21
ERR_ILLEGAL_DATA_COMMAND	0x22
ERR_ILLEGAL_LOCAL_MAC_ADR	0x23
ERR_ILLEGAL_INITIATOR_MAC_ADR	0x24
ERR_UNAVAILABLE_COMMAND	0x25

7.4 SEND AND RECEIVE NETWORK DATA WITH THE AMIS-49587

The data path should be implemented like specified in IEC 61334-5-1. The MAC layer is implemented by the AMIS-49587, the LLC layer should be implemented by the external processor (See Figure 29).

Figure 34 shows how a complete frame like it shows up on the power line (Physical Layer Frame) is composed of a MAC Layer Frame, taken care of by the AMIS-49587, encapsulating a LLC Layer Frame that should be provided by the external processors LLC layer.

Note that IEC 61334-5-1 specifies that the maximum length of a MAC layer frame is only 38 bytes. The maximum number of bytes that the AMIS-49587 accepts in one transmit command is 242 bytes. The AMIS-49587 takes care of splitting these 242 bytes in smaller chunks, encapsulate them in correct frames and send them over the power line.

The "Frame Indicator" and the "Number of the subframe" fields are omitted when the MAC frame is sent to the external processor since they don't contain useful information to the LLC layer.

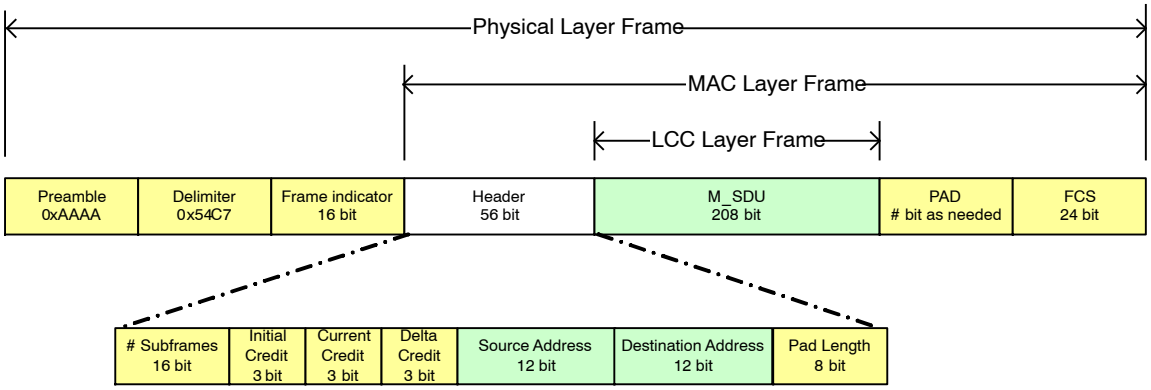


Figure 34. Power Line Data Frame Structure (IEC 61334-5-1)

Table 46. DATA PATH COMMANDS AND RESPONSES

Command	Unsolicited*	Initiator	Valid Command in Mode:	Code
MA_DATA_Indication	√	AMIS-49587 (MAC_Frame)	Master / Slave	50h
MA_DATA_Request	no	Application micro controller (MAC_Frame)	Master / Slave	51h
MA_DATA_Confirm	no	AMIS-49587 (Transmission_Status)	Master / Slave	52h
MA_DATA_Indication_Bad_CRC	√	AMIS-49587 (MAC_Frame)	Master / Slave	53h
ISA_Request	no	Application micro controller (Data_ISA)	Master / Slave	61h
ISA_Confirm	no	AMIS-49587 (Transmission_Status)	Master / Slave	62h
SPY_No_SubFrame	√	AMIS-49587 (SpyData)	Monitor	A0h
SPY_SubFrame	√	AMIS-49587 (SpyData, PHY_sdu)	Monitor	B0h
SPY_Search_Synchro	√	AMIS-49587 ()	Monitor	C0h
SPY_Synchro_Found	√	AMIS-49587 (SpyData)	Monitor	D0h
Spy_Alarm_Found	√	AMIS-49587 (SpyData, AlarmPattern)	Monitor	F0h
Spy_No_Alarm_Found	√	AMIS-49587 (SpyData, AlarmPattern)	Monitor	E0h
Synchro_Indication	√	AMIS-49587 (Synchro_Data)	Master / Slave	10h
Desynchro_Request	no	Application micro controller ()	Master / Slave / Monitor	11h
AccessDB_Request	no	Application micro controller (DB_Data_Id)	Master / Slave	41h
AccessDB_Confirm	no	AMIS-49587 (DB_Data_Id_Echo)	Master / Slave	42h
AccessDB_Error	no	AMIS-49587 (Error_Code)	Master / Slave	43h

*An unsolicited message is a message that is originating from the AMIS-49587, based upon an AMIS-49587 internal event. The message is not provoked by a prior command sent by the external processor.

7.4.1 MA_DATA_Indication

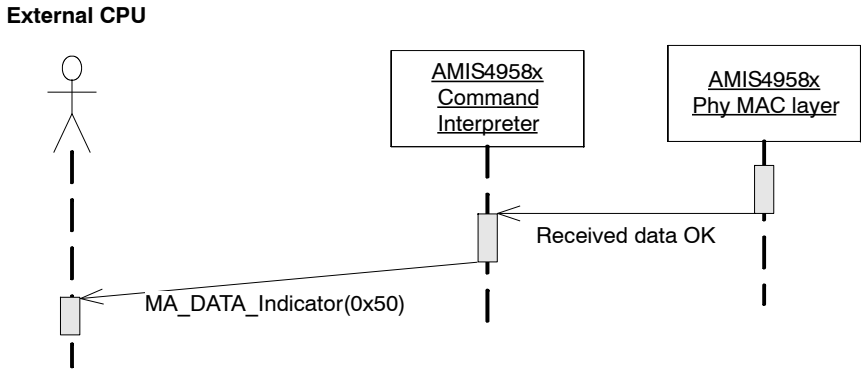


Figure 35. Sequence Diagram for MA_DATA_Indication

The MA_Data_Indication is sent from the AMIS-49587 (Client or Server) to the external controller to deliver the received DLC frame.

Frame Format:

<STX>	Length	MA_Data_Indication >	MAC_Frame	CHK

7.4.2 MA_DATA_Request

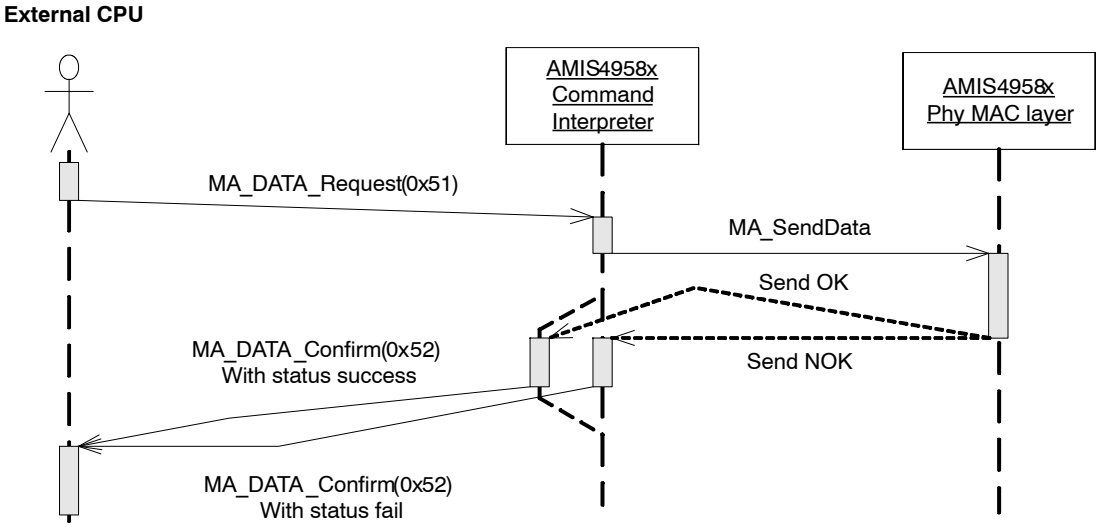


Figure 36. Sequence Diagram for MA_DATA_Request

The MA_Data_Request is sent from the external controller LLC layer to the AMIS-49587 local MAC sub-layer to request a DLC frame transmission. **This request must be received by the AMIS-49587 in the time-slot preceding the transmitting one.**

When the AMIS-49587 receives in the same time (same time-slot) an MA_Data_Request from the external controller and a frame made up of one sub-frame with a repetition credit at zero from the mains, it ignores the frame received from the mains. In all other conflict cases, it refuses the application micro controller request.

Frame Format:

<STX>	Length	0x51 (MA_Data_Request)	MAC_Frame	CHK

Table 47. DESCRIPTION OF THE MAC_Frame FIELD

Field Name	Length	Value	Description
Initial Credit	3 bits b7-b5	0h to 7h	Initial Credit
Current Credit	3 bits b4-b2	0h to 7h	Current Credit = Initial Credit
Delta Credit	2 bits b1,b0	0h to 3h	Delta Credit is Received Delta Credit for Slave mode and 0 for Master mode
Source Address	12 bits b23-b12	Not used	Slave Mode (Filled by MAC layer)
		000h to FFFh	Master Mode
Destination Address	12 bits b11-b0	000h to FFFh	Destination MAC address of the target station DLC
Pad length	1 byte	Not used	Filled by MAC layer
M_sdu	up to 242 bytes		MAC service data unit, the application data from the LLC layer implemented in the external processor.

7.4.3 MA_DATA_Confirm

The MA_DATA_Confirm is sent from AMIS-49587 to a external controller (SLAVE or MASTER) either as positive acknowledgment when a MA_DATA_Request has successfully been transmitted by the physical layer, or as negative acknowledgment when the transmission has been refused. The positive acknowledgment is sent after the frame transmission on the mains and before the beginning of the repetition (if the credit is higher than zero). The Transmission_Status byte contains a value corresponding at this positive or negative acknowledgment. The different values for the Transmission_Status field are described Table 48.

Table 48. TRANSMISSION STATUS

Field Name	Value	Description
OK	FFh	No error has been found
LM_TU1	00h	MA Data Confirm NEG Resources Temporary Unavailable at the MAC sub-layer
LM_SE	03h	Syntax Error at the MAC sub-layer
LM_TU2	0Ah	Command not authorized or Asic is not synchronized on the mains
LM_TU3	14h	PLC buffer not free or Asic is busy Resources Temporary Unavailable at the MAC sub-layer
LM_TU4	1Eh	PLC buffer not free or Asic is busy Resources Temporary Unavailable at the MAC sub-layer

Frame Format:

<STX>	Length	0x52 (MA_Data_Confirm)	Transmission_Status	CHK

7.4.4 MA_DATA_Indication_Bad_CRC

The MA_Data_Indication_Bad_CRC is sent from the AMIS-49587 (Client or Server) to the external micro controller to deliver an erroneous frame. This command is only used if the Bad CRC transmitting option is chosen during the configuration. The frame with errors can be used by the external controller to analyze the faults.

Frame Format:

<STX>	Length	0x53 (MA_Data_Indication_Bad_CRC)	MAC_Frame	CHK

7.4.5 SPY_No_SubFrame

The SPY_No_SubFrame is sent by the AMIS-49587 local PHY layer to indicate that a sub-frame has not been received correctly, due to either a method not found, or a non recognition of the Start Sub-frame Delimiter (SSD).

Frame Format:

<STX>	Length	0xA0 (SPY_No_SubFrame)	SpyData	CHK

Table 49. DESCRIPTION OF THE SpyData FIELD

Field Name	Length	Description
S0	2 Bytes	Value of the zero signal envelope
N0	2 Bytes	Value of the zero noise envelope
S1	2 Bytes	Value of the one signal envelope
N1	2 Bytes	Value of the one noise envelope
Threshold	2 Bytes	Indicates the threshold value for ASK method or the FSK factor.
Method	1 Byte	Indicates the found method: 0 ⇒ No method 1 ⇒ ASK0 2 ⇒ ASK1 3 ⇒ FSK (S0 ≅ S1) 4 ⇒ FSK0 (S0 > S1) 5 ⇒ FSK1 (S1 > S0)
PAD	1 Bit (b7)	0
Synchro_bit Value	3 Bits (b6,b5,b4)	Synchronization bit value when synchronization was found
PAD	1 Bit (b3)	0
Reception Gain	3 Bits (b2,b1,b0)	Indicates the gain value (0 to 7) used during the synchronization

7.4.6 SPY_SubFrame

The SPY_SubFrame is sent by the AMIS-49587 local PHY layer to indicate that a sub-frame has been correctly received. All information concerning the reception conditions (SpyData) and the data (PHY_sdu) are supplied in this command. For the format of the SpyData field, see Table 49.

Frame Format:

<STX>	Length	0xB0 (Spy_SubFrame)	SpyData Field, PHY_sdu	CHK

7.4.7 SPY_Search_Synchro

The SPY_Search_Synchro is sent periodically by the AMIS-49587 local MAC sub-layer to indicate synchronization is in progress.

Frame Format:

<STX>	Length	0xC0 (Spy_Search_Synchro)	CHK

7.4.8 SPY_Synchro_Found

The SPY_Synchro_Found is sent by the AMIS-49587 local MAC sub-layer as soon as it has correctly found synchronization when it was receiving a sub-frame. Thus, it is now synchronized and it is waiting for another correct frame for confirmation.

For the format of the SpyData field, see Table 49.

Frame Format:

<STX>	Length	0xD0 (Spy_ Synchro_Found)	SpyData	CHK

7.4.9 Spy_Alarm_Found

The SPY_No_Alarm_Found is sent by the AMIS-49587 local MAC sub-layer at the end of a time-slot, when it has not found an Alarm indication in the pause time.

For the format of the SpyData field, see Table 49.

The AlarmPattern has a length of 2 bytes.

Frame Format:

<STX>	Length	0xF0 (SPY_ No_Alarm_Found)	SpyData, AlarmPattern	CHK

7.4.10 Spy_No_Alarm_Found

The SPY_Alarm_Found is sent by the AMIS-49587 local MAC sub-layer as soon as it has correctly found a Alarm indication in the pause time.

For the format of the SpyData field, see Table 49.

The AlarmPattern has a length of 2 bytes.

Frame Format:

<STX>	Length	0xE0 (SPY__Alarm_Found)	SpyData, AlarmPattern	CHK

7.4.11 Synchro_Indication

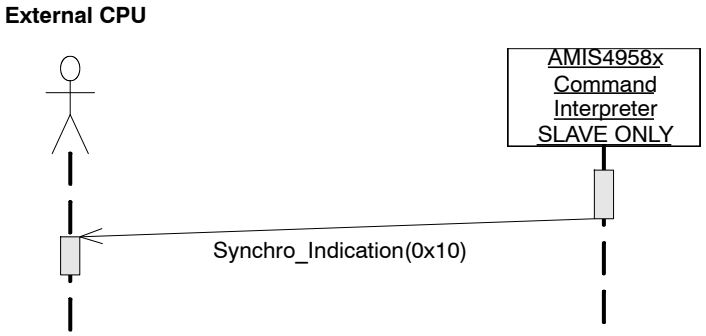


Figure 37. Sequence Diagram for Synchro_Indication

The Synchro_Indication is sent by the AMIS-49587 in order to indicate that something has changed in the synchronization state. The field Synchro_Data contains the change reason and data corresponding with this change.

Frame Format:

<STX>	Length	0x10 (Synchro_Indication)	Synchro_Data	CHK

The Synchro_Data field contains a synchronization event description of 1 or 2 bytes with accompanying data.

Table 50. Synchro_Data FIELDS

Event Description, byte 1	Event Description, byte 2	Length and Synchro_data Description	Remark
0x01 Synchronization Found		1 byte: Pad 2 bytes: Signal S0 2 bytes: Noise N0 2 bytes: Signal S1 2 bytes: Noise N1 2 bytes: ASK Threshold or FSK factor 1 byte : Method 1 byte : Synchro-Bit and Gain values	
0x02 Synchronization Confirmed		1 byte: Pad 2 bytes: Source MAC Address 2 bytes: Destination MAC Address	
0x04 Synchronization Lost	**0x01** Time-out not addressed has expired	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Slave mode
0x04 Synchronization Lost	**0x02** Time-out frame not OK has expired	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Master and Slave mode
0x04 Synchronization Lost	**0x03** Time-out synchro confirm has expired	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Master and Slave mode
0x04 Synchronization Lost	**0x04** Addressed by a wrong initiator	2 bytes: Source MAC Add 2 bytes: Dest. MAC Add	Slave mode
0x04 Synchronization Lost	**0x05** External desynchro command	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Master and Slave mode
0x04 Synchronization Lost	**0x06** Search Initiator active	2 bytes: Last initiator MAC Address received 2 bytes: Current initiator MAC Address choice	Slave mode

7.4.12 Desynchro_Request

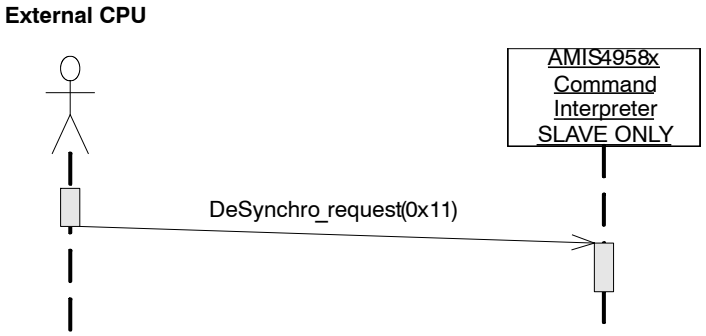


Figure 38. Sequence Diagram for DeSynchro_Request

The Desynchro_Request command is used by the external controller to enforce the not synchronized state in the AMIS-49587 and therefore it starts looking for a new synchronization.

Frame Format:

<STX>	0x03 (Length)	0x11 (Desynchro_Request)	CHK

7.4.13 AccessDB_Request

Field Name	Ident	Description
PhyAlarmRequest	**000F**	Request the transmission of a Phy Alarm

7.4.13.1 PhyAlarmRequest

Description:
This request is used to send a physical alarm pattern. No data is transmitted to indicate the number of repetitions, the AMIS−49587 already knows this number because it is in its set of configuration data.

Request Format:

<STX>	0x05(Length)	0x41 (AccessDB_Request)	0x0F00	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0F00h	Number of alarm Transmissions (1 byte)	CHK

7.4.14 AccessDB_Confirm
See paragraph AccessDB_Confirm.

7.4.15 AccessDB_Error
See paragraph AccessDB_Error.

7.5 RETRIEVE STATISTICAL DATA FROM THE AMIS−49587

Table 51. STATISTICS COMMAND AND RESPONSES

Command	Unsolicited*	Initiator	Valid Command in Mode:	Code
AccessDB_Request	no	Application micro controller (DB_Data_Id)	Master / Slave	41h
AccessDB_Confirm	no	AMIS−49587 (DB_Data_Id_Echo)	Master / Slave	42h
AccessDB_Error	no	AMIS−49587 (Error_Code)	Master / Slave	43h

*An unsolicited message is a message that is originating from the AMIS−49587, based upon an AMIS−49587 internal event. The message is not provoked by a prior command sent by the external processor.

7.5.1 AccessDB_Request
The AccessDB_Request command can be used to read data path statistical information from the AMIS−49587.
Like in all other AccessDB_Request commands, the specific identifier of the data that is to be read needs to be provided:

Field Name	Identifier	Description
Invalid−frame−counter	**0x0006**	Read the value of the invalid−frame counter and then set to 0
Counters	**0x000D**	Read the value of the data counters:Counter Crc Ok, Counter Crc Not Ok, Repeater counter, Transmit counter, corrected frames counter, and then set to 0 or not
DataStats	**0x0010**	Read the value of the Data statistics, and then set to 0 or not.

7.5.1.1 Invalid Frame Counter
This request is used to read the Invalid Frame Counter of the AMIS−49587. Once the request sent to the AMIS−49587, the Invalid Frame counter is automatically set to 0. The AMIS−49587 answers with the value of the Invalid Frame Counter

Request Format:

<STX>	0x05(Length)	0x41 (AccessDB_Request)	0x0600	CHK

Confirm Format:

<STX>	0x06(Length)	0x42 (AccessDB_Confirm)	0x0600	Invalid Frame Counter (1 byte)	CHK

7.5.1.2 Data Counters

The Data Counters request is used to read the value of the data counters in the AMIS-49587. It contains one byte which is used to know whether the counters must be reset or not (00: no reset, 01: reset) after reading them out.
There are 6 counters coded on 4 bytes each, which indicates:

1. number of CRC OK frames received
2. number of CRC not OK frames received
3. number of repeated frames
4. number of transmitted frames
5. number of corrected frames (with option Pad Correcting)
6. number of frames with bad Frame Indicator received

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x0D00	Request Counters (1 byte)	CHK

Confirm Format:

<STX>	0x1D(Length)	0x42 (AccessDB_Confirm)	0x0D00	CRC_OK (4 bytes), CRC_NOK (4 bytes), Rep_Frames (4 bytes), Tr_Frames (4 bytes), Corr_Frames (4 bytes), FI_NOK (4 bytes)	CHK

7.5.1.3 DataStats

The DataStats request is used to read the value of the current data statistics in the AMIS-49587. The request contains one byte which is used to know whether the counters must be reset or not (00: no reset, 01: reset) after reading them out.
If the AMIS-49587 is synchronized the counters consist of 30 bytes:

1. The value of signal and noise (S0, N0, S1, N1) for the last subframe received (4 * 2 bytes) + the method and gain used to demodulate this subframe (2 * 1 byte)
2. The method, gain and SNR (S0/N0, S1/N1) on the 5 last time slots in reception mode (5 * 4 bytes) + 1 byte to know the actual position in the table

If the AMIS-49587 is not synchronized the counters consist of 36 bytes:

1. The values of the real and imaginary parts of the signal for each frequency (I0, Q0, I1, Q1),
2. for the 4 last calculated time-slots (4 * (4 * 2 bytes))
3. The current position in the board (1 byte)
4. The software reception gain (1 byte)
5. The hardware reception gain (1 byte)
6. The R_ALC value (1 byte)

Request Format:

<STX>	0x06(Length)	0x41 (AccessDB_Request)	0x1000	Reset Counters (1 byte)	CHK

Confirm Format:

If the AMIS-49587 is synchronized:

<STX>	0x23(Length)	0x42 (AccessDB_Confirm)	0x1000	Signal_noise_subframe (10 bytes), SNRreception (20 bytes)	CHK

If the AMIS-49587 is not synchronized:

<STX>	0x29(Length)	0x42 (AccessDB_Confirm)	0x1000	I0,I1,Q1 (32 bytes), Pos (1 byte), GainSoft (1 byte), GainHard (1 byte), R_ALC (1 byte)	CHK

7.5.2 AccessDB_Confirm

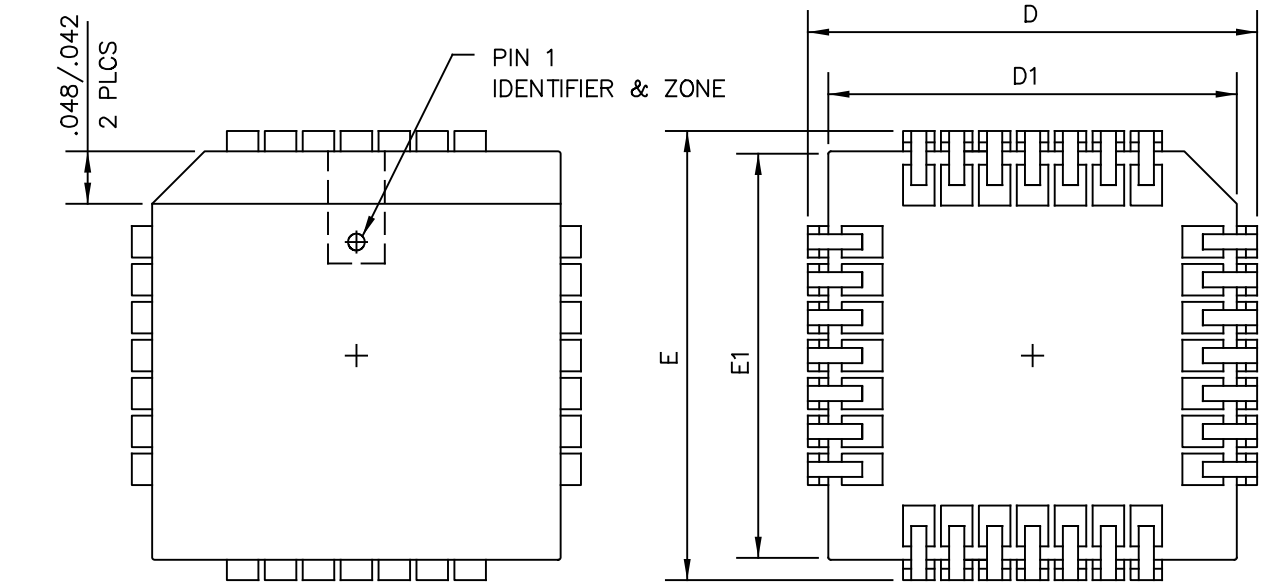
See paragraph AccessDB_Confirm.

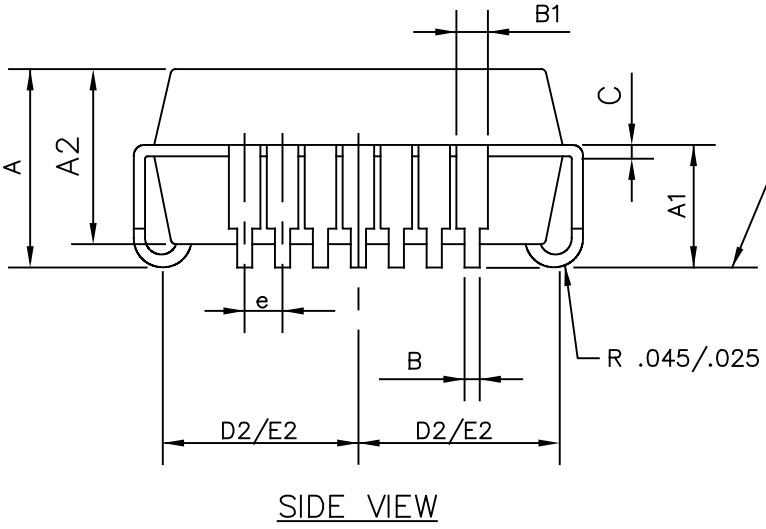
7.5.3 AccessDB_Error

See paragraph AccessDB_Error.

PACKAGE DIMENSIONS

PLCC 28 LEAD
CASE 776AA-01
ISSUE O





SYMBOL	MIN	NOM	MAX
A	0.165	0.172	0.180
A1	0.090	0.105	0.120
A2	0.148	0.152	0.156
B	0.013	0.017	0.021
B1	0.026	0.029	0.032
C	0.008	0.010	0.012
D	0.485	0.490	0.495
D1	0.450	0.453	0.456
D2	0.195	0.210	0.215
E	0.485	0.490	0.495
E1	0.450	0.453	0.456
E2	0.195	0.210	0.215
e	0.050 REF.		

ALL DIMENSIONS ARE IN INCHES.

PACKAGE DIMENSIONS

QFN52 8x8, 0.5P
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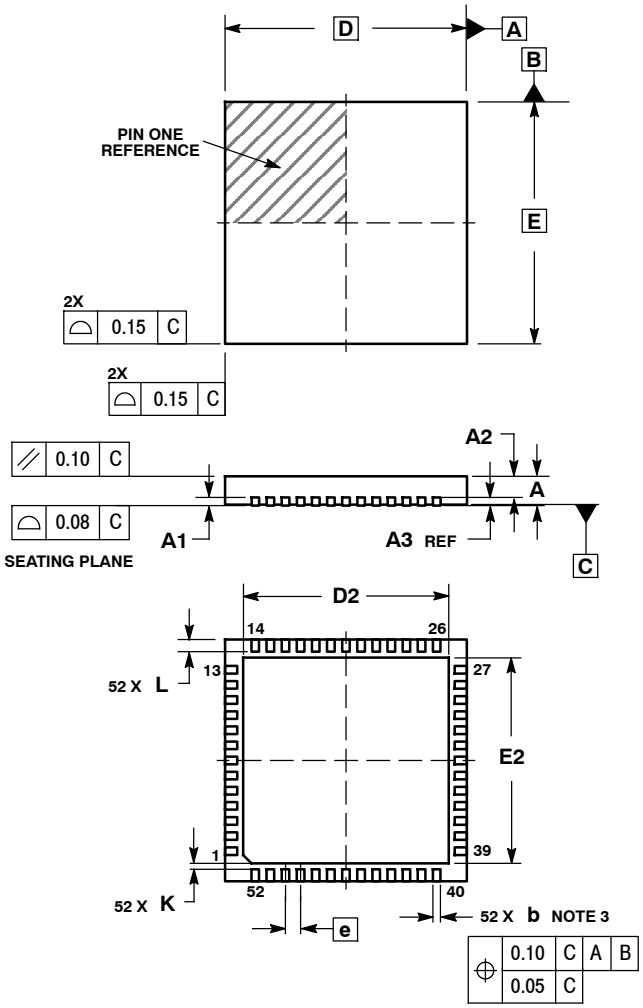

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

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