25LC010A
25LC020A
25LC040A

1K-4K SPI Serial EEPROM High Temp Family Data Sheet

Features:

- Max. Clock 5 MHz
- Low-Power CMOS Technology:
  - Max. Write Current: 5 mA at 5.5V, 5 MHz
  - Read Current: 5 mA at 5.5V, 5 MHz
  - Standby Current: 10 μA at 5.5V
- 128 x 8 through 512 x 8-bit Organization
- Byte and Page-level Write Operations
- Self-Timed Erase and Write Cycles (6 ms max.)
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability:
  - Endurance: >1M erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature Range Supported:
  - Extended (H): -40°C to +150°C
- Package is Pb-Free and RoHS Compliant

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
VCC	Supply Voltage

Description:

Microchip Technology Inc. 25LCXXXA* devices are low-density 1 through 4 Kbit Serial Electrically Erasable PROMs (EEPROM). The devices are organized in blocks of x8-bit memory and support the Serial Peripheral Interface (SPI) compatible serial bus architecture. Byte-level and page-level functions are supported.

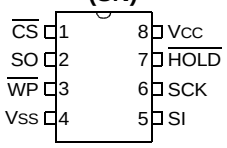
The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25LCXXXA is available in a standard 8-lead SOIC package. The package is Pb-free and RoHS Compliant.

Package Types (not to scale)

SOIC (SN)



*25LCXXXA is used in this document as a generic part number for the 25 series devices.

Device Selection Table

Part Number	Density (bits)	Organization	VCC Range	Max. Speed (MHz)	Page Size (Bytes)	Temp. Range	Package
25LC010A	1K	128 x 8	2.5V-5.5V	5	16	H	SN
25LC020A	2K	256 x 8	2.5V-5.5V	5	16	H	SN
25LC040A	4K	512 x 8	2.5V-5.5V	5	16	H	SN

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to 155°C

Ambient temperature under bias..... -40°C to 150°C(1)

ESD protection on all pins.....4 kV

Note 1: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time between 125°C and 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Extended (H): TA = -40°C to +150°C VCC = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-level input voltage	.7 VCC	VCC+1	V	
D002	VIL1	Low-level input voltage	-0.3	0.3VCC	V	VCC ≥ 2.7V
D003	VIL2		-0.3	0.2VCC	V	VCC < 2.7V
D004	VOL	Low-level output voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL		—	0.2	V	IOL = 1.0 mA
D006	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA
D007	ILI	Input leakage current	—	±2	µA	$\overline{CS}$ = VCC, VIN = VSS OR VCC
D008	ILO	Output leakage current	—	±2	µA	$\overline{CS}$ = VCC, VOUT = VSS OR VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(Note)**
D010	ICC Read	Operating Current	— —	5 2.5	mA mA	VCC = 5.5V; FCLK = 5.0 MHz; SO = Open VCC = 2.5V; FCLK = 3.0 MHz; SO = Open
D011	ICC Write		— —	5 3	mA mA	VCC = 5.5V VCC = 2.5V
D012	ICCS	Standby Current	— —	10	µA	$\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, 150°C

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Extended (H): T_A = -40°C to +150°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	— —	5 3	MHz MHz	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
2	TCSS	$\overline{CS}$ Setup Time	100 150	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
3	TCSH	$\overline{CS}$ Hold Time	200 250	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	—
5	Tsu	Data Setup Time	20 30	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
6	THD	Data Hold Time	40 50	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
7	TR	CLK Rise Time	—	100	ns	**(Note 1)**
8	TF	CLK Fall Time	—	100	ns	**(Note 1)**
9	THI	Clock High Time	100 150	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
10	TLO	Clock Low Time	100 150	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
11	TCLD	Clock Delay Time	50	—	ns	—
12	TCLE	Clock Enable Time	50	—	ns	—
13	TV	Output Valid from Clock Low	— —	100 160	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
14	THO	Output Hold Time	0	—	ns	**(Note 1)**
15	TDIS	Output Disable Time	— —	80 160	ns ns	4.5V ≤ Vcc ≤ 5.5V **(Note 1)** 2.5V ≤ Vcc ≤ 4.5V **(Note 1)**
16	THS	$\overline{HOLD}$ Setup Time	40 80	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
17	THH	$\overline{HOLD}$ Hold Time	40 80	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
18	THZ	$\overline{HOLD}$ Low to Output High-Z	60 160	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V **(Note 1)** 2.5V ≤ Vcc < 4.5V **(Note 1)**
19	THV	$\overline{HOLD}$ High to Output Valid	60 160	— —	ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V
20	TWC	Internal Write Cycle Time	—	6	ms	**(Note 2)**
21	—	Endurance	1,000,000	—	E/W Cycles	Page Mode, 25°C, V_{CC} = 5.5V **(Note 3)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
V_{LO} = 0.2V	—
V_{HI} = V_{CC} - 0.2V	**(Note 1)**
V_{HI} = 4.0V	**(Note 2)**
C_L = 50 pF	**—**
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For $V_{CC} \leq 4.0V$

2: For $V_{CC} > 4.0V$

FIGURE 1-1: HOLD TIMING

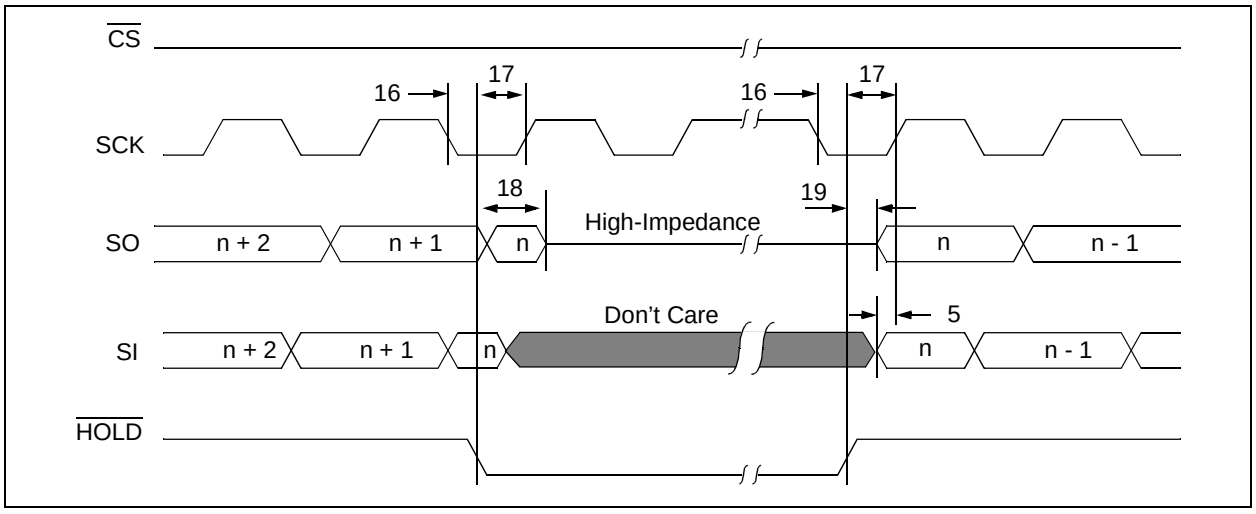


FIGURE 1-2: SERIAL INPUT TIMING

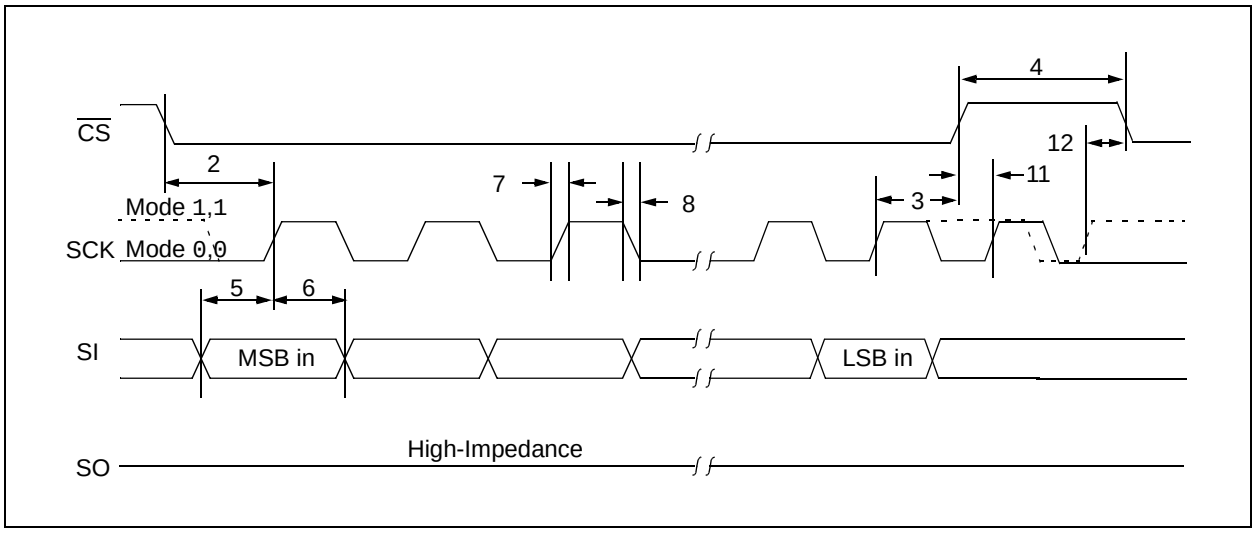
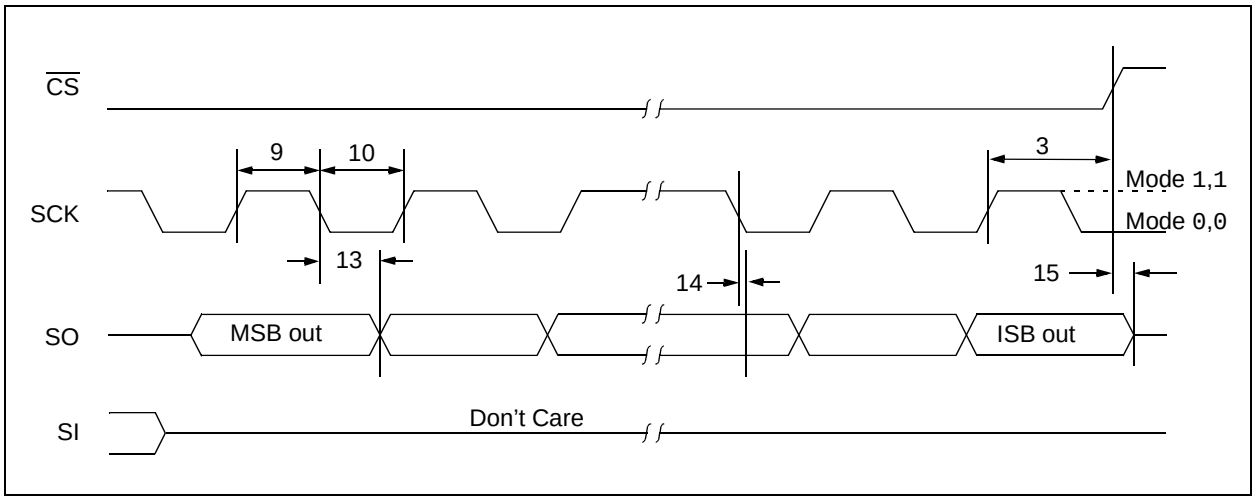


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{CS}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{WP}$	3	Write-Protect Pin
VSS	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{HOLD}$	7	Hold Input
VCC	8	Supply Voltage

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25LCXXXA. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{WP}$)

The WP pin is a hardware write-protect input pin. When it is low, all write to the array or STATUS registers are disabled, but any other operations function normally. When WP is high, all functions including nonvolatile writes, operate normally. At any time, when WP is low, the write enable Reset latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, WP going low will not change or disable the write cycle. See Table 5-1 for Write-Protect Functionality Matrix.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25LCXXXA. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25LCXXXA while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25LCXXXA must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25LCXXXA are low-density serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25LCXXXA contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25LCXXXA in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

BLOCK DIAGRAM

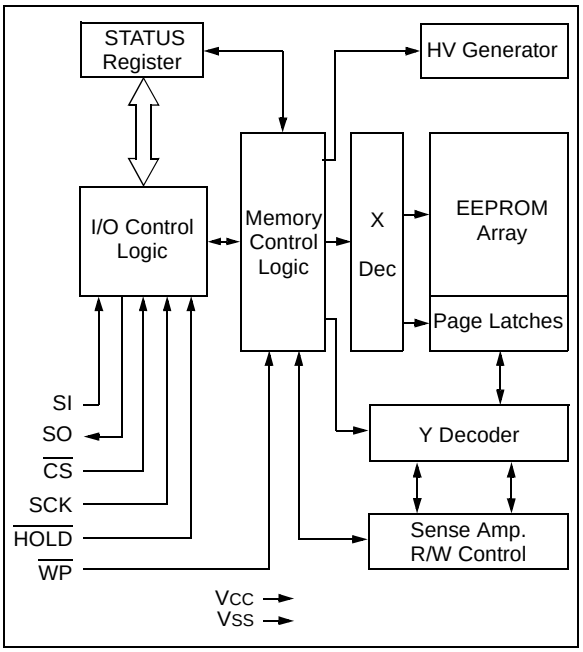


TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 $A_8$011	Read data from memory array beginning at selected address
WRITE	0000 $A_8$010	Write data to memory array beginning at selected address
WRDI	0000 x100	Reset the write enable latch (disable write operations)
WREN	0000 x110	Set the write enable latch (enable write operations)
RDSR	0000 x101	Read STATUS register
WRSR	0000 x001	Write STATUS register

Note: For the 24LC040A device, A_8 is the 9th address bit, which is used to address the entire 512 byte array. For the 24LC020A and 24LC010A devcies, A_8 is a don't care.

x = don't care.

3.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit READ instruction is transmitted to the 25LCXXXA followed by the 8-bit address. For the 25LC040A the MSb (A8) is sent to the slave during the instruction sequence. See Figure 3-1 for more details. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

3.3 Write Sequence

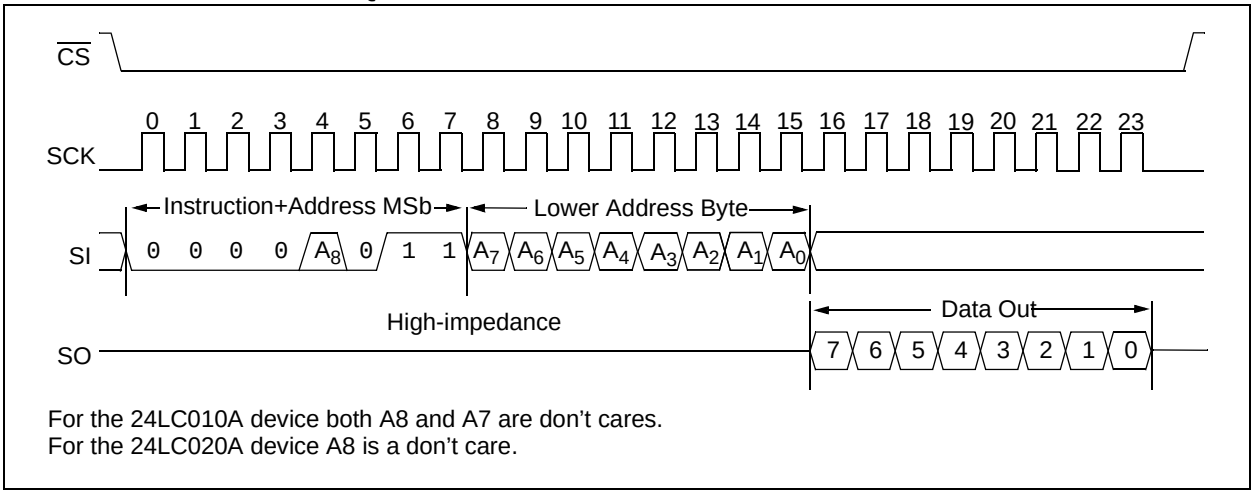
Prior to any attempt to write data to the 25LCXXXA, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25LCXXXA. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a WRITE instruction, followed by the 8-bit address, and then the data to be written. Up to 16 bytes can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally a page address begins with 'XXXX 0000' and ends with 'XXXX 1111'. If the internal address counter reaches 'XXXX 1111' and clock signals continue to be applied to the ship, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

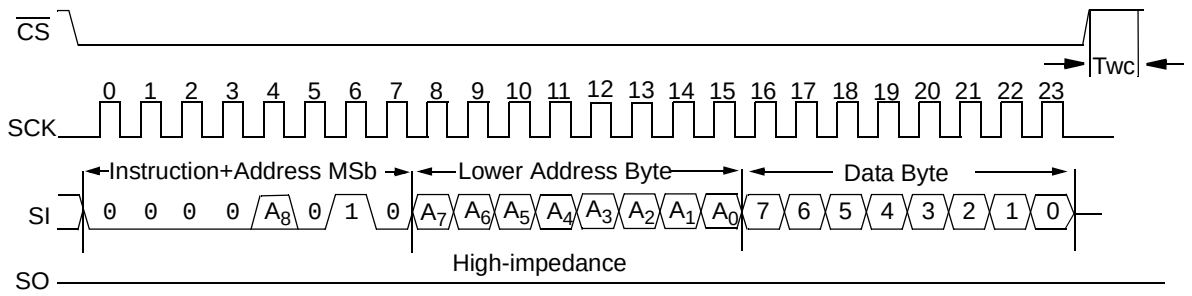
For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-6 and Figure 3-4 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

FIGURE 3-1: READ SEQUENCE



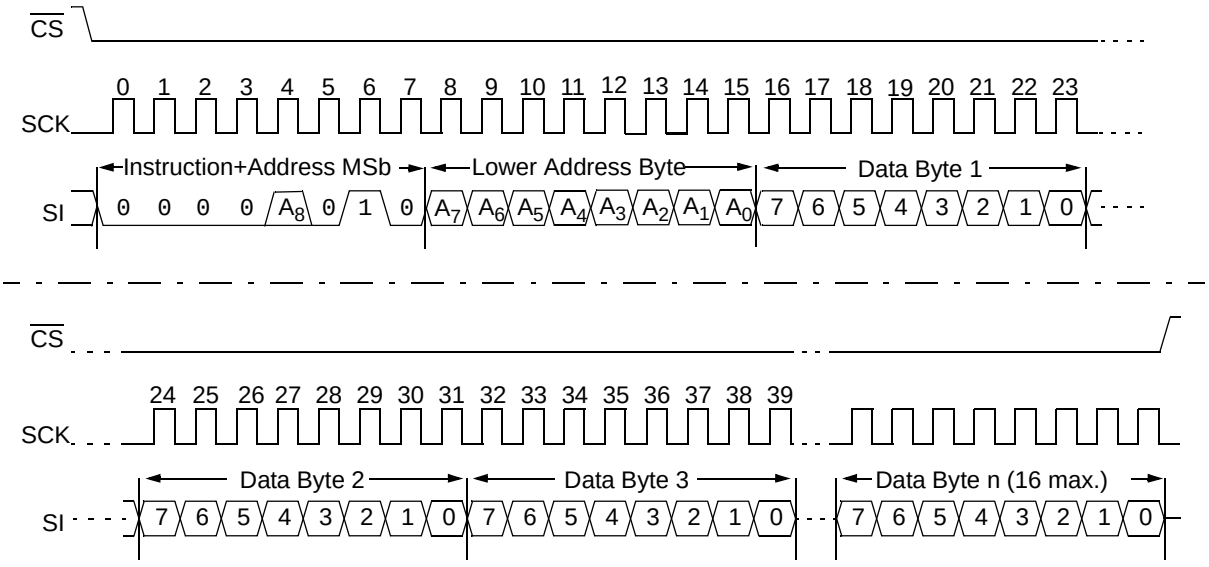
For the 24LC010A device both A8 and A7 are don't cares.
For the 24LC020A device A8 is a don't care.

FIGURE 3-2: BYTE WRITE SEQUENCE



For the 24LC010A device both A8 and A7 are don't cares.
For the 24LC020A device A8 is a don't care.

FIGURE 3-3: PAGE WRITE SEQUENCE



For the 24LC010A device both A8 and A7 are don't cares.
For the 24LC020A device A8 is a don't care.

3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25LCXXXA contains a write enable latch. See Table 5-1 for the write-protect functionality matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ pin is brought low

FIGURE 3-4: WRITE ENABLE SEQUENCE (WREN)

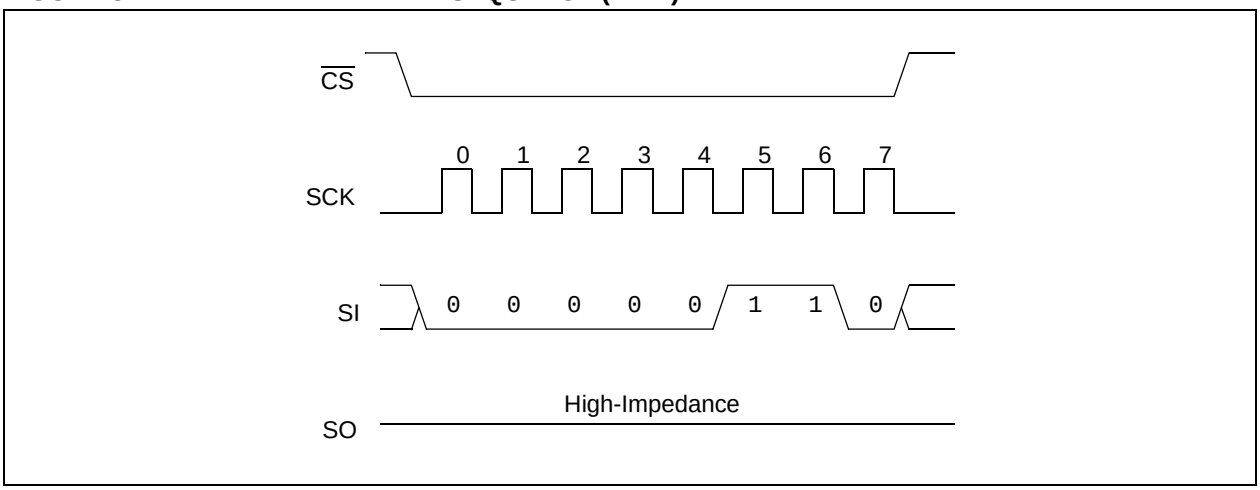
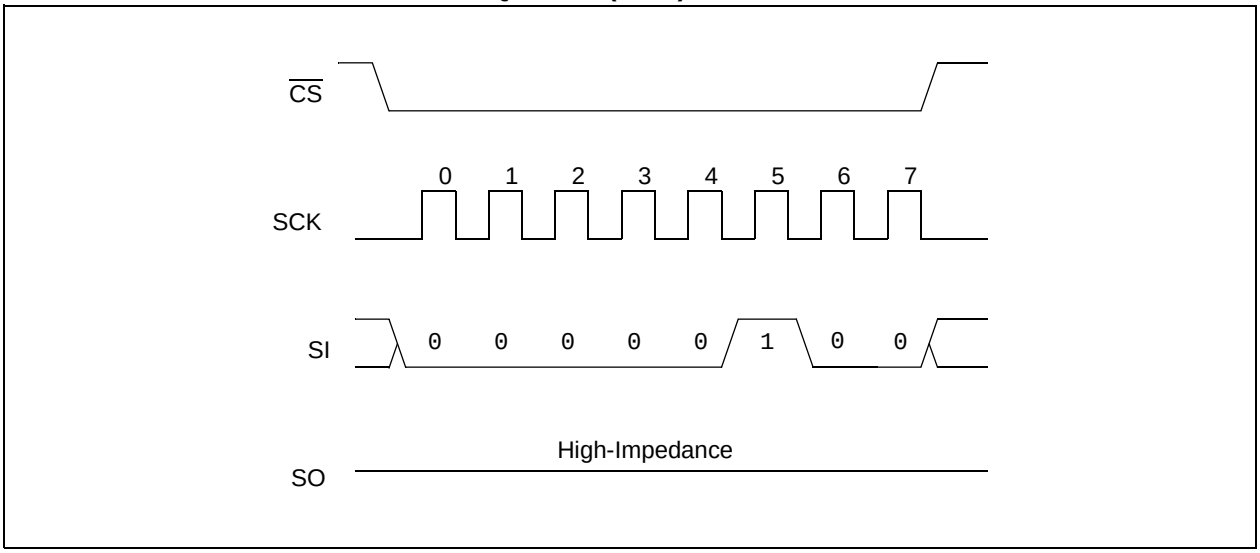


FIGURE 3-5: WRITE DISABLE SEQUENCE (WRDI)



3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 3-2: STATUS REGISTER

7	6	5	4	3	2	1	0
–	–	–	–	W/R	W/R	R	R
X	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

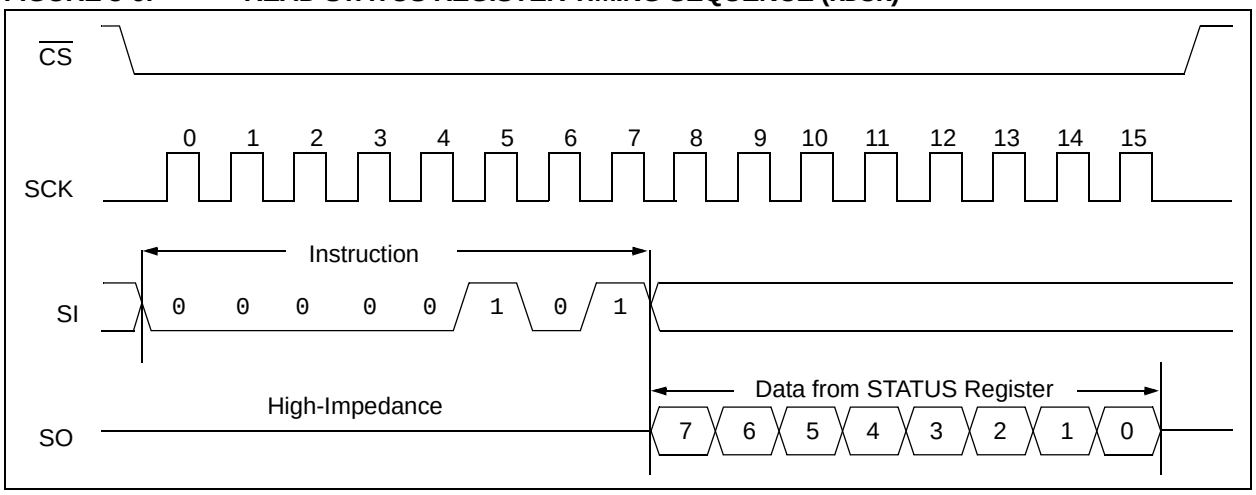
The **Write-In-Process (WIP)** bit indicates whether the 25LCXXXA is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile, and are shown in Table 3-3.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 3-3.

See Figure 3-6 for the WRSR timing sequence.

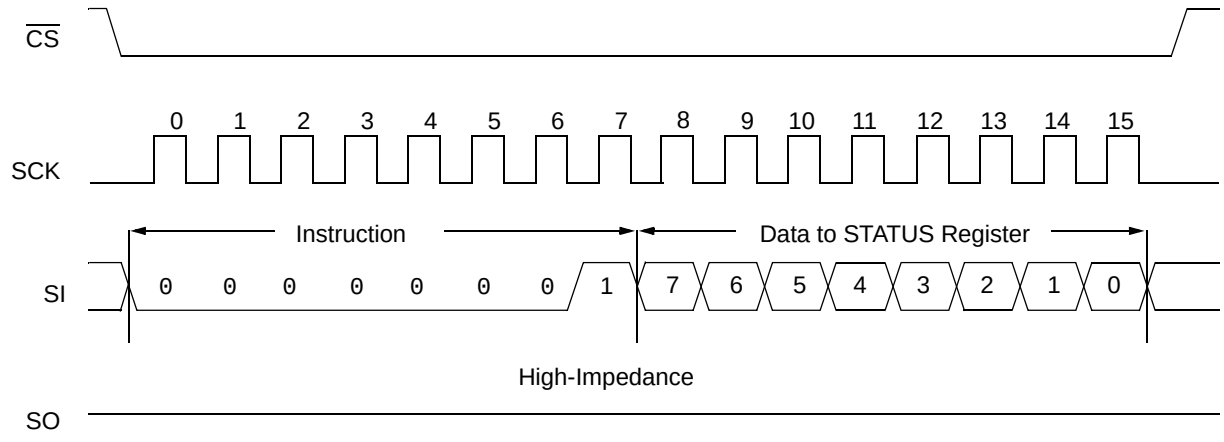
TABLE 3-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	None	All
0	1	Upper 1/4	Lower 3/4
1	0	Upper 1/2	Lower 1/2
1	1	All	None

TABLE 3-4: ARRAY PROTECTED ADDRESS LOCATIONS

Density	Upper 1/4	Upper 1/2	All
1K	60h - 7Fh	40h - 7Fh	00h - 7Fh
2K	C0h - FFh	80h - FFh	00h - FFh
4K	180h - 1FFh	100h - 1FFh	000h - 1FFh

FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note: An internal write cycle (Twc) is initiated on the rising edge of $\overline{CS}$ after a valid write STATUS register sequence.

4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

5.0 POWER-ON STATE

The 25LCXXXA powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

TABLE 5-1: WRITE-PROTECT FUNCTIONALITY MATRIX

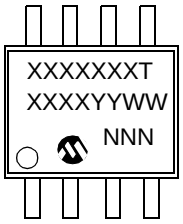
$\overline{WP}$ (pin 3)	WEL (SR bit 1)	Protected Blocks	Unprotected Blocks	STATUS Register
0 (low)	x	Protected	Protected	Protected
1 (high)	0	Protected	Protected	Protected
1 (high)	1	Protected	Writable	Writable

x = don't care

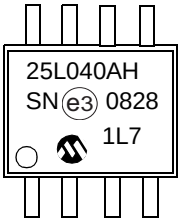
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

8-Lead SOIC



Example:



8-Lead SOIC Package Marking (Pb-Free)	
Device	**Line 1 Marking**
25LC010A	25L010AT
25LC020A	25L020AT
25LC040A	25L040AT
Note 1: T = Temperature Grade (H).	

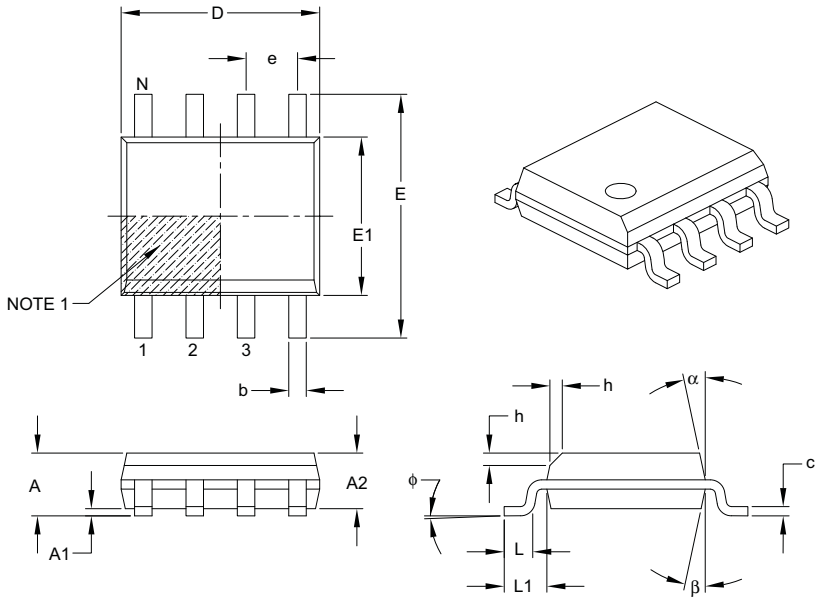
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Custom marking available.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

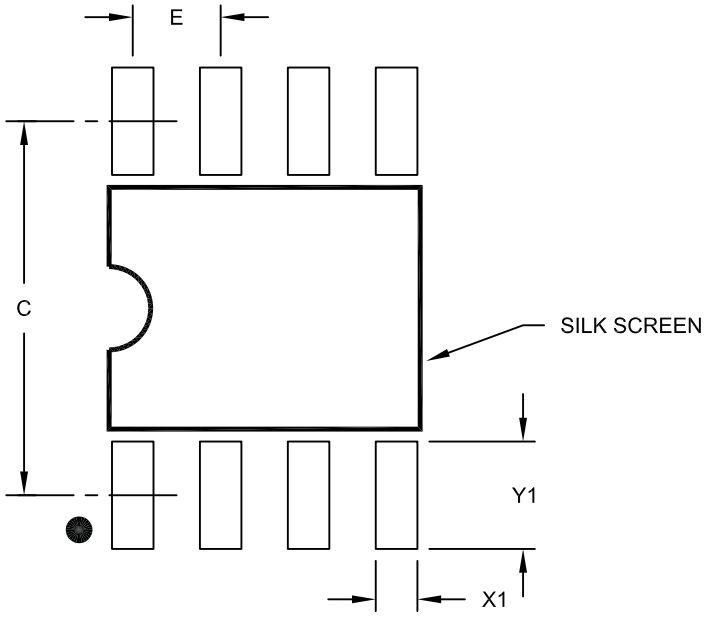
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision A (03/2009)

Original release.

Revision B (06/2009)

Revised Features: Endurance; Revised Note 1 in Section 1.0 Electrical Characteristics; Revised Table 1-2, Para. 21.

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4. What additions to the document do you think would enhance the structure and subject?

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–	X	/XX
Device	Tape & Reel		Temp Range	Package

Device:	25LC010A =		1k-bit, 2.5V, 16 Byte Page, SPI Serial EEPROM
	25LC020A =		2k-bit, 2.5V, 16 Byte Page, SPI Serial EEPROM
	25LC040A =		4k-bit, 2.5V, 16 Byte Page, SPI Serial EEPROM
Tape & Reel:	Blank	=	Standard packaging
	T	=	Tape & Reel
Temperature Range:	H	=	-40°C to+150°C
Package:	SN	=	Plastic SOIC (3.90 mm body), 8-lead

Examples:

a) 25LC010AT-H/SN = 1k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package

b) 25LC020A-H/SN = 2k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., SOIC package

c) 25LC040AT-H/SN = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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