VR 12 Compatible Single Phase MOSFET Driver with Diode Emulation

IDTP67001

Description

The IDTP67001 is a high frequency single-phase MOSFET driver that delivers 12V gate drive to both high and low side power N-Channel MOSFETs in synchronous rectifier buck regulator power supply applications. The IDTP67001 is compatible with IDT VR12 controller (IDTP63041 and IDTP63031) and external MOSFETs to form complete core voltage regulator for advanced microprocessors. The IDTP67001 detects the DE# active low signal sent by PWM controller and activates diode emulation for high efficiency light load operation. In normal conditions IDTP67001 operates in Continuous Conduction mode (CCM) PWM mode.

The output drivers of IDTP67001 can efficiently switch power MOSFETs up to a frequency of 1 MHz, maximizing power supply efficiency and minimizing size. The outputs of the IDTP67001 provide less than 30ns typical rise and fall times with 3nF loading.

The IDTP67001 incorporates shoot-through circuitry to prevent both upper and lower MOSFETs from conducting simultaneously. The IDTP67001 can detect fault conditions during initial start-up before the multi-phase PWM controller takes control of the system to prevent catastrophic high voltages at the buck regulator output.

The internal boostrap diode reduces the total solution cost and the external component count. The IDTP67001 implements a diode emulation mode with the low side MOSFET to prevent reverse inductor current. IDTP67001 is available in thermally enhanced SO-8 package with metal paddle.

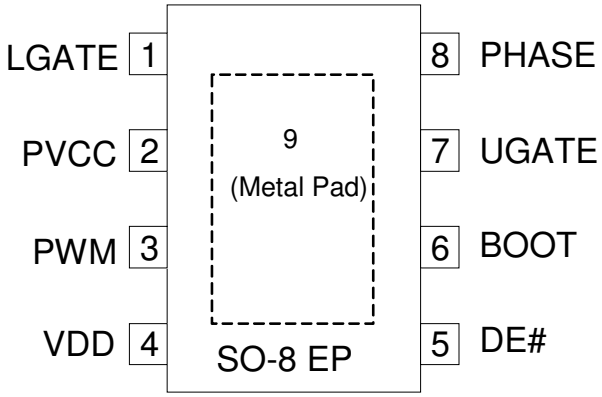
Features

- Drives high and low side N-Channel power MOSFETs.
- 50V Internal Bootstrap Schottky diode.
- 6-Ω series resistance with Schottky diode to protect driver from voltage spikes due to board parasitics.
- Shoot-Through protection
- High switching frequency up to 1 MHz
- 1A Source and 2A Sink capability
- Fast rise/Fall times for reduced switching losses
- Propagation Delay time < 30ns
- Fault detection and load protection circuitry
- Tri-State PWM input allows both gate outputs to drive low and disconnect inductor from the load during shutdown.
- Synchronous FET diode emulation mode with control pin provides improved light load efficiency.
- Packaged in thermally enhanced 8-pin SOIC with metal pad for low thermal impedance.
- Pb-free and RoHS compliant.

Applications

- Desktop/Enterprise Computing
- VR12 CPU/GPU Multiphase Regulators
- Battery Powered equipment
- Voltage Regulator Modules

Pin Configuration



Absolute Maximum Ratings (All voltages referred to GND, unless specified)

PVCC	15V
VDD	7V
PHASE	-5 to 15V (DC) < 30V (<200 ns)
BOOT to PHASE	15V
BOOT	-0.3V to (PVCC+15)V (DC) -0.3V to 50V (<200ns)
PHASE	-4V to 15V -0.3V to 38V (<200ns)
PWM, DE Voltage	GND-0.3 to 7V
UGATE Voltage.	(VPHASE-0.3)V to (VBOOT+0.3)V
LGATE Voltage	-0.3V to (PVCC+0.3)V
ESD, HBM	2kV
ESD MM	200V

Continuous Power Dissipation (T_A=25 °C)--		
8 pin SOIC (JEDEC-51 STD conditions)----		1.61W
Operating Junction Temperature	------	125°C
Ambient operating temperature	------	0°C to 70 °C
Soldering Temperature (10 Sec)	------	260°C
Storage Temperature	------	-40 °C to +150 °C

Electrical Characteristics

4.5V ≤ VDD ≤ 5.5V, 10.8V ≤ PVCC ≤ 13.2V, 0°C ≤ T_J ≤ 125°C Unless stated otherwise. Typical data at T_J = 25 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SUPPLY CURRENT						
Operating Supply Current	IVDD	PWM = open,unloaded output		2.9	4.8	mA
		PWM=250kHz square wave, GND to VDD, unloaded output		3.1	5.0	mA
Operating Supply Current	IPVCC	PWM = Open, unloaded output		230	590	µA
		PWM=250kHz square wave, GND to VDD, unloaded output		2.3	3.3	mA
UNDER VOLTAGE LOCK OUT						
VDD Threshold Rising	VDDTHR		3.35	3.80	4.20	V
VDD Threshold Falling	VDDTHF		2.65	3.25	3.70	V
VDD Hysteresis	VDDHYS	VDDTHR-VDDTHF	220	580	770	mV
PVCC Threshold Rising	PVCCTHR		5.5	6.7	7.7	V
PVCC Threshold Falling	PVCCTHF		5.3	6.5	7.5	V
PVCC Hysteresis	PVCCHYS	PVCCTHR-PVCCTHF	100	230	350	mV
PWM INPUT						
Input Current	IPWM	PWM=VDD or GND		350	435	µA
Open Voltage	VFLP	IPWM=0		1.90		V
Input Threshold HI, rising	VIHRP		3.00	3.50	4.00	V

Electrical Characteristics (Continued)

4.5V ≤ VDD ≤ 5.5V, 10.8V ≤ PVCC ≤ 13.2V, 0°C ≤ T_J ≤ 125°C Unless stated otherwise. Typical data at T_J = 25 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Threshold HI, falling	VIHFP		2.80	3.30	3.85	V
Input Hysteresis, HI	VIHHYSP	VIHRP- VIHFP		180		mV
Input Threshold LO, rising	VILRP		1.13	1.3	1.43	V
Input Threshold LO, falling	VILFP		1.05	1.15	1.32	V
Input Hysteresis, LO	VILHYSP	VILRP- VILFP		150		mV
LGATE						
Source Current	ILGH	3nF load		1.0		A
Sink Current	ILGL	3nF load		2.0		A
Sink Impedance	RSGL	I=150mA		0.4	1.5	Ω
Rise Time	TRGL	3nF load, 20% to 80%		23		ns
Fall Time	TFGL	3nF load, 80% to 20%		12		ns
UGATE						
Source Current	IUGH	3nF load		0.9		A
Sink Current	IUGL	3nF load		2.0		A
Rise Time	TRGH	3nF load, 20% to 80%		27		ns
Fall Time	TFGH	3nF load, 80% to 20%		12		ns
PROPAGATION DELAYS						
PWM rising to LGATE falling	TPPH	3nF load, PWM at 50% to LGATE at 90%		17		ns
PWM falling to UGATE falling	TPPL	3nF load, PWM at 50% to UGATE at 90%		24		ns
LGATE falling to UGATE rising	TIHX	LGATE at 1V to UGATE at 1V		25		ns
UGATE falling to LGATE rising	TILX	PHASE at 3V to LGATE at 1V		13		ns
PWM Low Tri-state Delay	PLHZ	3nF load, PWM input = 0V, release to HiZ, time to LGATE falling to < 1V		95		ns
PWM High Tri-state Delay	PHHZ	3nF load, PWM input = 5V, release to HiZ, time to UGATE falling to < 1V		110		ns
PWM Low to LGATE ON timeout when Phase held high	PLTO	3nF load, PHASE > 6V, PWM falling to 50% VDD to LGATE rising to 1V		115		ns

Electrical Characteristics (Continued)

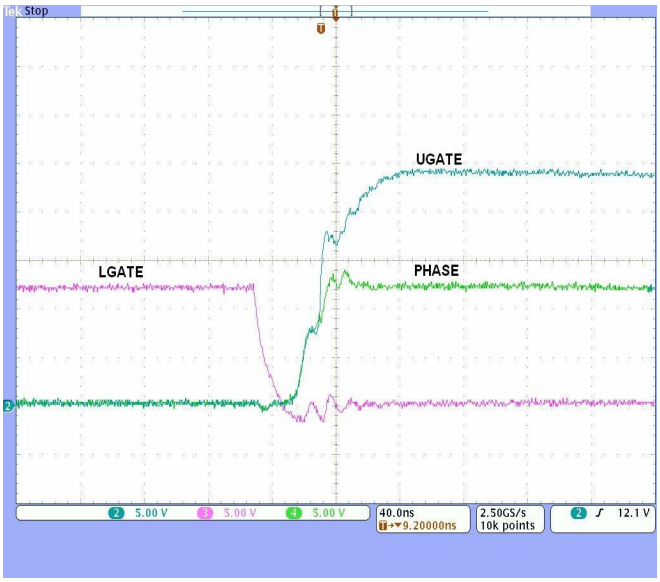
4.5V ≤ VDD ≤ 5.5V, 10.8V ≤ PVCC ≤ 13.2V, 0°C ≤ T_J ≤ 125°C Unless stated otherwise. Typical data at T_J = 25 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
BOOT DIODE						
Forward Voltage	BDFV	I=10mA		0.77	1.02	V
Reverse Leakage	BDRL	V=PVCC		0.1		µA
DIODE EMULATION						
DE# Input Current	IDEH	DE = VDD		0	1.0	µA
	IDEL	DE = GND		5	10	µA
DE# Input EnableThreshold	VILDE				1.35	V
DE# Input DisableThreshold	VIHDE		2.5			V
DE# Input Thresold Hysteresis	VHYSDE	VIHDE-VILDE		250		mV
Minimum LGATE high time	TMINONLG	PHASE = 1V, Measure at 50%		250		ns
Phase Comparator detection time	TPHCOMPDET	PHASE = VOFFSET to LGATE = 90% PVCC		60		ns

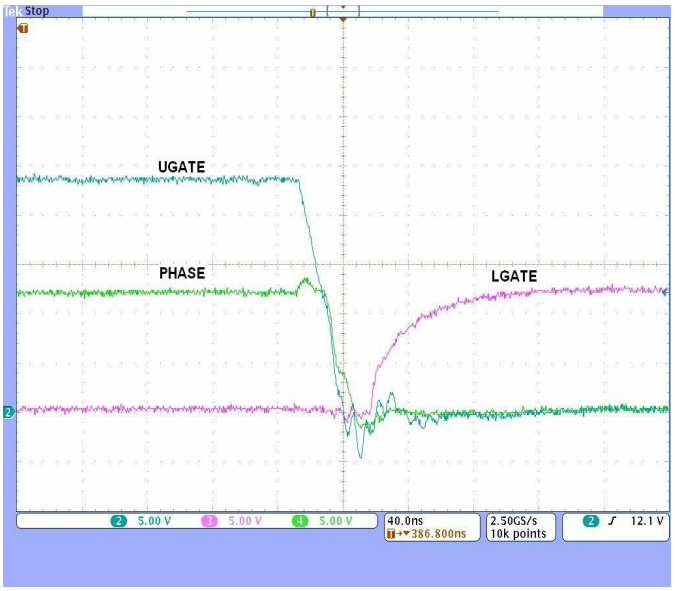
Typical Operating Characteristics

(T_A=25°C, unless otherwise specified. V_{DD}=5V, PV_{CC}=12V Refer Figure 1.)

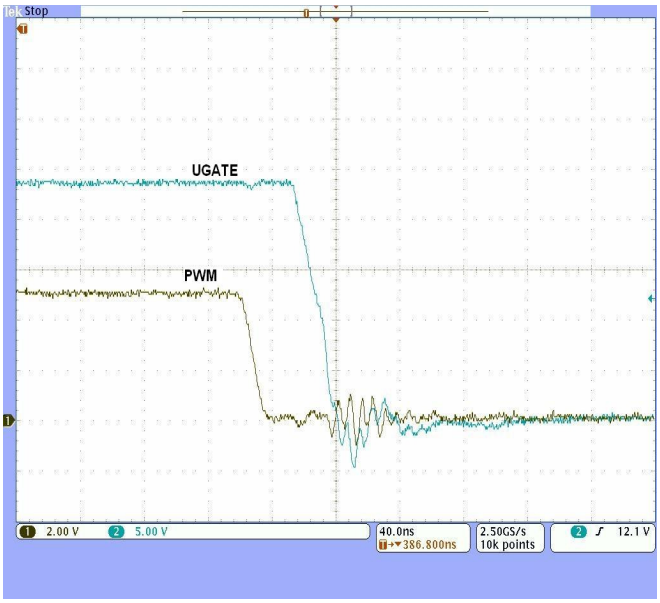
Dead Time LGATE to UGATE



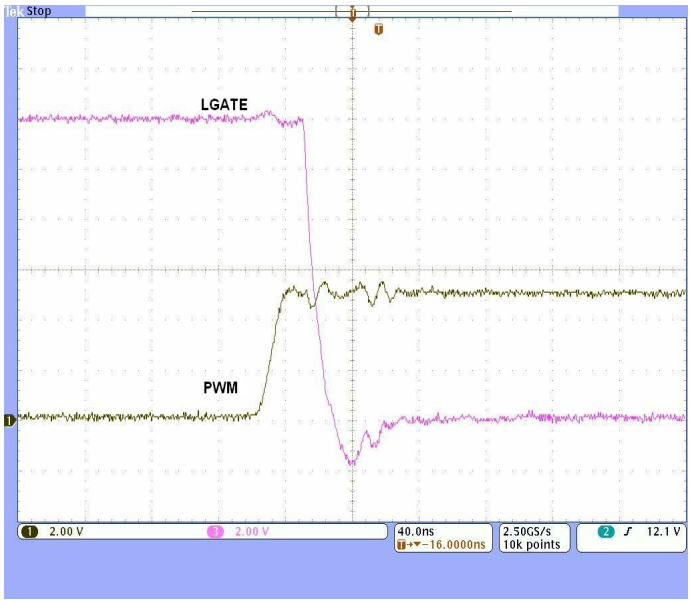
Dead Time UGATE to LGATE



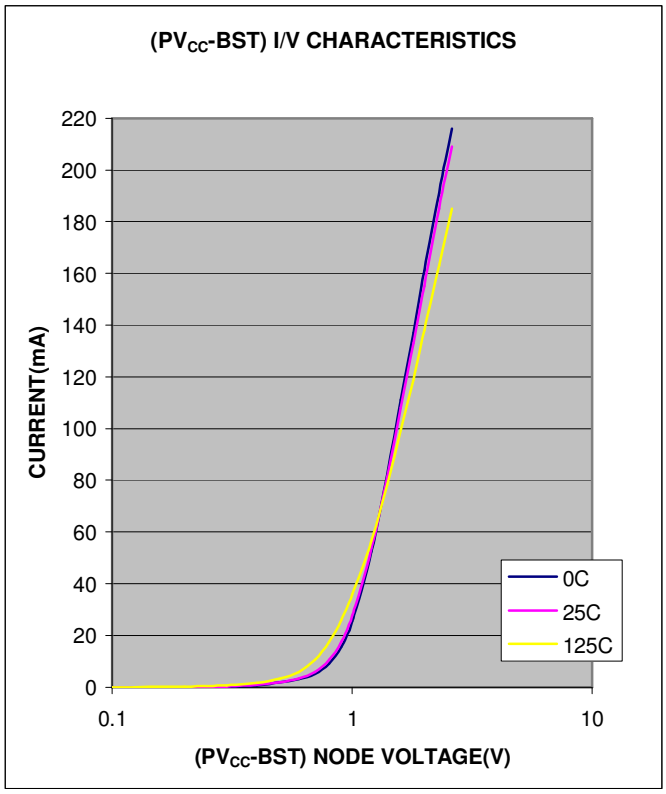
Propagation Delay PWM to UGATE



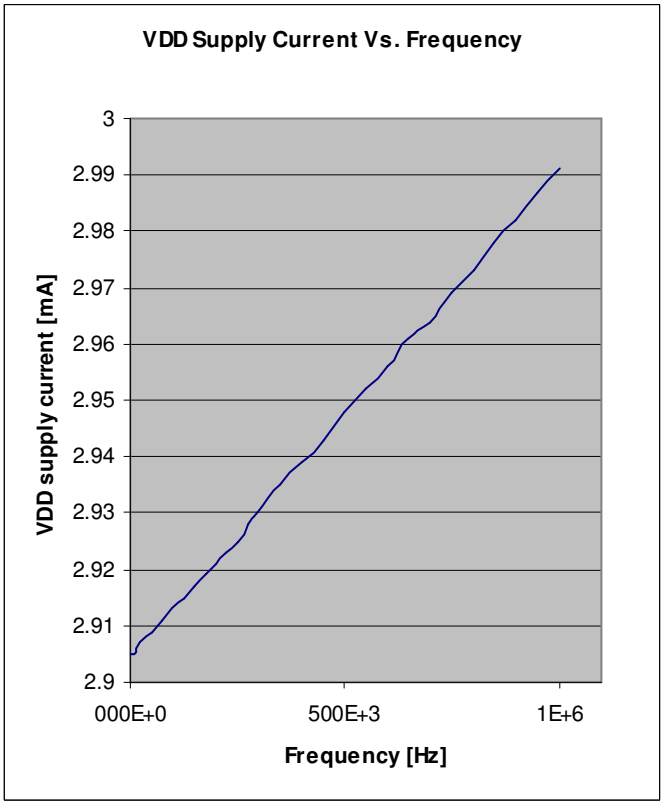
Propagation Delay PWM to LGATE



(PV_{CC}-BST) Node I-V Characteristics



I_{VDD} Vs Switching Frequency



Block Diagram

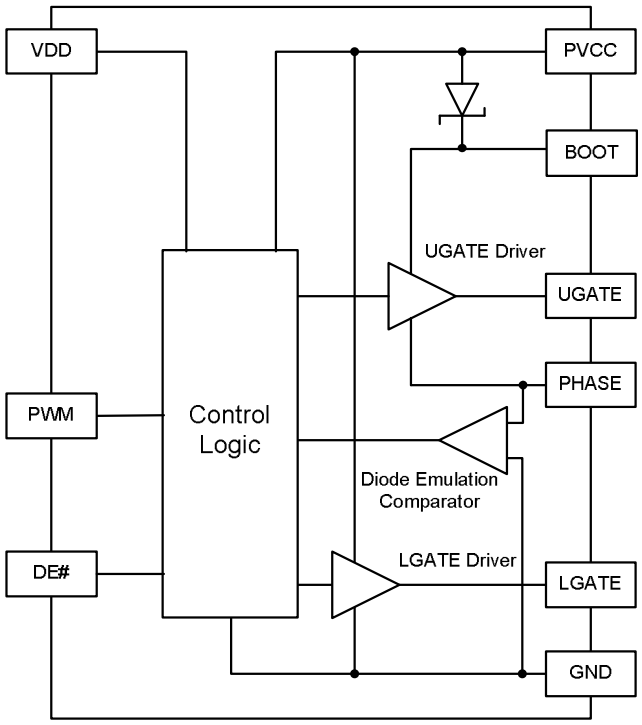


Figure 1. Block Diagram

Pin Descriptions

Pin #	Pin Name	Pin Type	Description
1	LGATE	Output	Lower Gate Drive Output. Connect to the lower power MOSFET gate.
2	PVCC	Power	Power Supply Input. Connect to+12 V supply. Bypass this pin to GND as close to the package as possible with1µF ceramic capacitor.
3	PWM	Input	PWM input control. Connect to the PWM output of the controller.
4	VDD	Power	5 V control supply to driver. Bypass this pin to GND as close to the package as possible with1µF ceramic capacitor.
5	DE#	Input	A low level on this pin enables Diode Emulation Mode. Leaving DE# open or tying it to VDD disables Diode Emulation mode and the driver operates in continuous conduction mode.
6	BOOT	Input	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin.
7	UGATE	Output	Upper Gate Drive Output. Connect to the upper power MOSFET gate.
8	PHASE	Input	Upper driver return and input to dead time control circuitry. Connected to the inductor switching node.
9	GND	Power	Device Ground at metal pad on package bottom. Must be connected to power GND and to large continuous copper area.

Typical Application Circuit

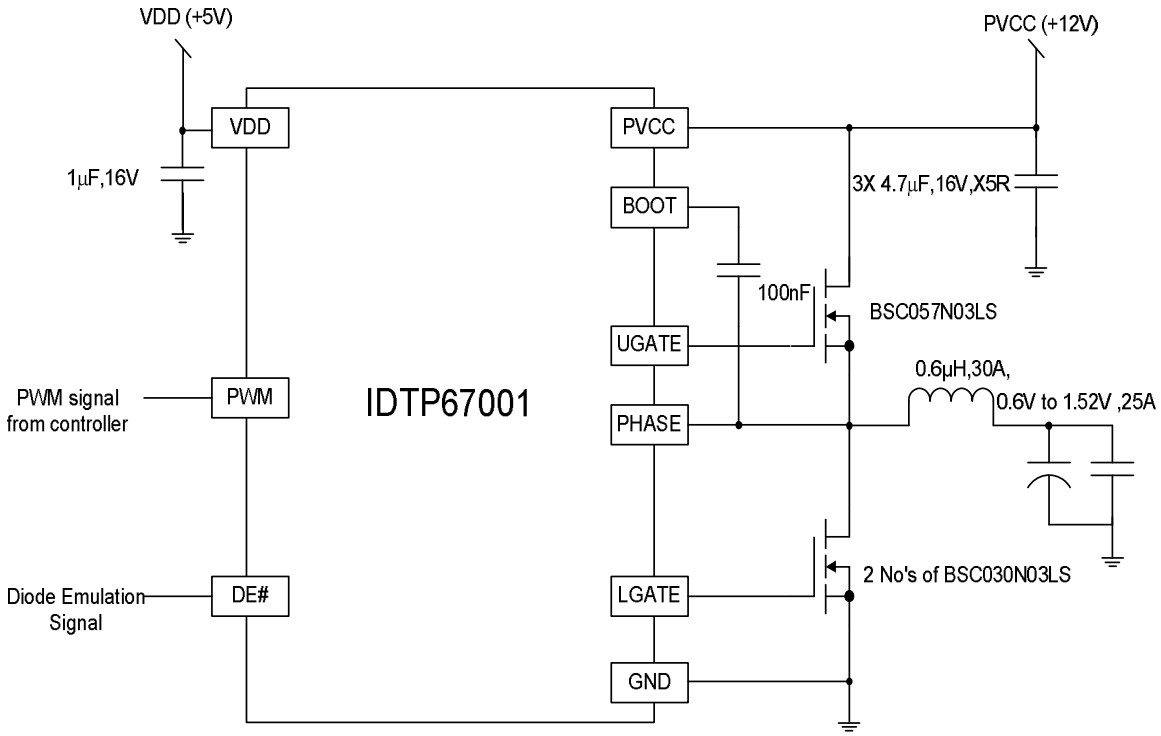


Figure 2. Typical Application Circuit

Timing Diagram

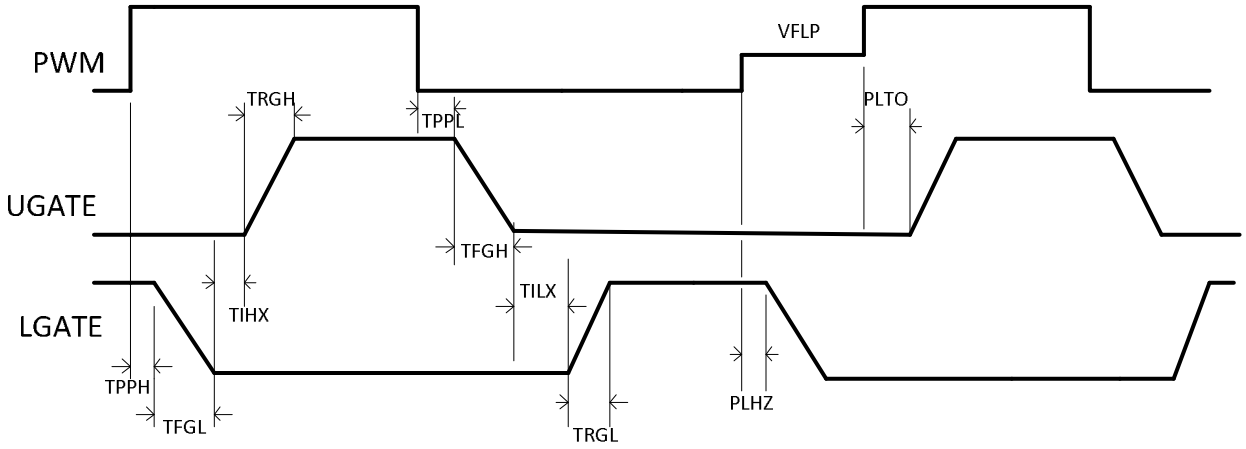


Figure 3. Timing diagram

Detailed Description

The IDTP67001 is designed to switch both the high side and low side N-channel MOSFETs totem pole configuration from a single PWM input. The PWM input pin has three states. Upon a low to high PWM transition, LGATE drives low, then UGATE drives high, to allow conduction in the high side control MOSFET(s). A high to low PWM transition will first drive UGATE low before driving LGATE high, allowing conduction in the low side synchronous rectifier MOSFET(s). A voltage on the PWM pin between the maximum input low voltage and the minimum input high voltage drives both LGATE and UGATE low, and puts all external MOSFETs into a high impedance drain-source OFF state.

Internal circuitry is included on the IDTP67001 PWM input pin to bias it between the upper and lower thresholds if the driving signal becomes high impedance indicating that tri-state operation is desired. This bias cicuit consumes almost no VDD current when the PWM input signal is high impedance to minimize standby current, yet allows fast (<130ns) transition to tri-state operation.

Shoot Through Protection

IDTP67001 prevents the high side and low side MOSFETs from conducting simultaneously with circuitry that adapts to the MOSFET characteristics, circuit configuration, and operating modes. Upon transition of the PWM input from a low to high threshold UGATE does not drive high until the LGATE voltage decreases to less than 1.0V (typical relative to GND). Upon transition of the PWM input from a high to low threshold LGATE does not drive high until the PHASE voltage decreases to less than 3V (typical) indicating that the high side control MOSFET is not conducting any significant current under normal operating conditions. However; since the voltage on the PHASE pin can exceed the 3V threshold for an extended period due to negative inductor current LGATE will drive high after a 115ns (typical) timeout period even if the voltage on the PHASE pin exceeds the 3V threshold.

Bootstrap circuit

IDTP67001 contains an internal boostrap diode between PVCC and BOOT. The drive voltage for UGATE is generated by charging a capacitor between BOOT and PHASE when PHASE is low. The capacitor between BOOT and PHASE should be a low ESR MLCC capacitor, X5R or X7R dielectric. A 100nF capacitor value is adequate for most applications. Larger values can be used but they can cause large diode current surges during start-up with pre-charged output voltages when the PHASE pin initially drives low. For low current applications with high gate charge MOSFETs, higher capacitance values up to 220nF are needed.

Pre Power On Output Overvoltage Protection

In fault conditions, it may be possible that input voltage 12V directly present at the converter output during 12V power-up due to a shorted high side power MOSFET or other problem. In this situation the PWM control IC may not have sufficient bias voltage to allow it to command the IDTP67001 to turn on the low side power MOSFET and attempt to save the load from damage due to over voltage and/or trip the over current protection in the 12V input supply. To address this situation the IDTP67001 monitors the voltage on the the PHASE pin, if PHASE voltage and the PVCC voltage are the same and exceed 4V (typical) with the PWM input in a high impedance tri-state condition it will drive LGATE high. This protection feature does not rely on any bias voltage being present at the VDD input.

PVCC + VDD Bypass Capacitors

PVCC is the supply pin for the LGATE driver and UGATE bootstrap circuit. PVCC should be bypassed with a low ESR X5R or X7R capacitor of 1.0uF as close to the the PVCC and GND pins as possible. VDD should also be bypassed with a low ESR X5R or X7R 1.0uFcapacitor of as close to the the VDD and GND pins as possible. Minimize the use of vias between the bypass caps and IC pins.

Diode Emulation

Upon assertion of the DE# input pin to a logic low by the PWM controller, the IDTP67001 monitors the drain-source voltage on the low side power MOSFET after its PWM input is driven below its low threshold. When the voltage across the MOSFET (between PHASE and GND) increases above 0V indicating a reverse inductor current, LGATE is turned off for the remainder of the PWM low time to reduce system conduction losses. A minimum LGATE on time of 250ns (typical) is provided to ensure the bootstrap capacitor doesn't discharge during diode emulation.

Power Dissipation

Power dissipation in the IDTP67001 is primarily caused by the charging and discharging of external MOSFETs and internal control circuitry.

The power loss is given by following equation.

$$P_D = ((Q_{GH} \times n_H + Q_{GL} \times n_L) \times f_{SW}) PV_{CC} + I_{VDD} \times V_{DD}$$

Where Q_{GH},Q_{GL} is total gate charge of high side and low side MOSFETs respectively. n_H,n_L is number of MOSFETs on high side and low side respectively.Use the following equation to estimate the operating temperature of the die.

$T_J = T_A + (P_D \times \theta_{J-A})$

Where T_A is maximum ambient temperature and θ_{J-A} is thermal resistance given in following table. Keep thermal dissipation such that it will not exceed the maximum operating junction temperature of 125 °C.

Thermal Characteristics

Parameter	Symbol	Typ.	Units
Thermal Resistance Junction to Ambient (JEDEC-51 STD conditions)	θ_{JA}	61.9	°C/W
Thermal Resistance Junction to Case	θ_{JC}	112.8	°C/W

Application Circuit

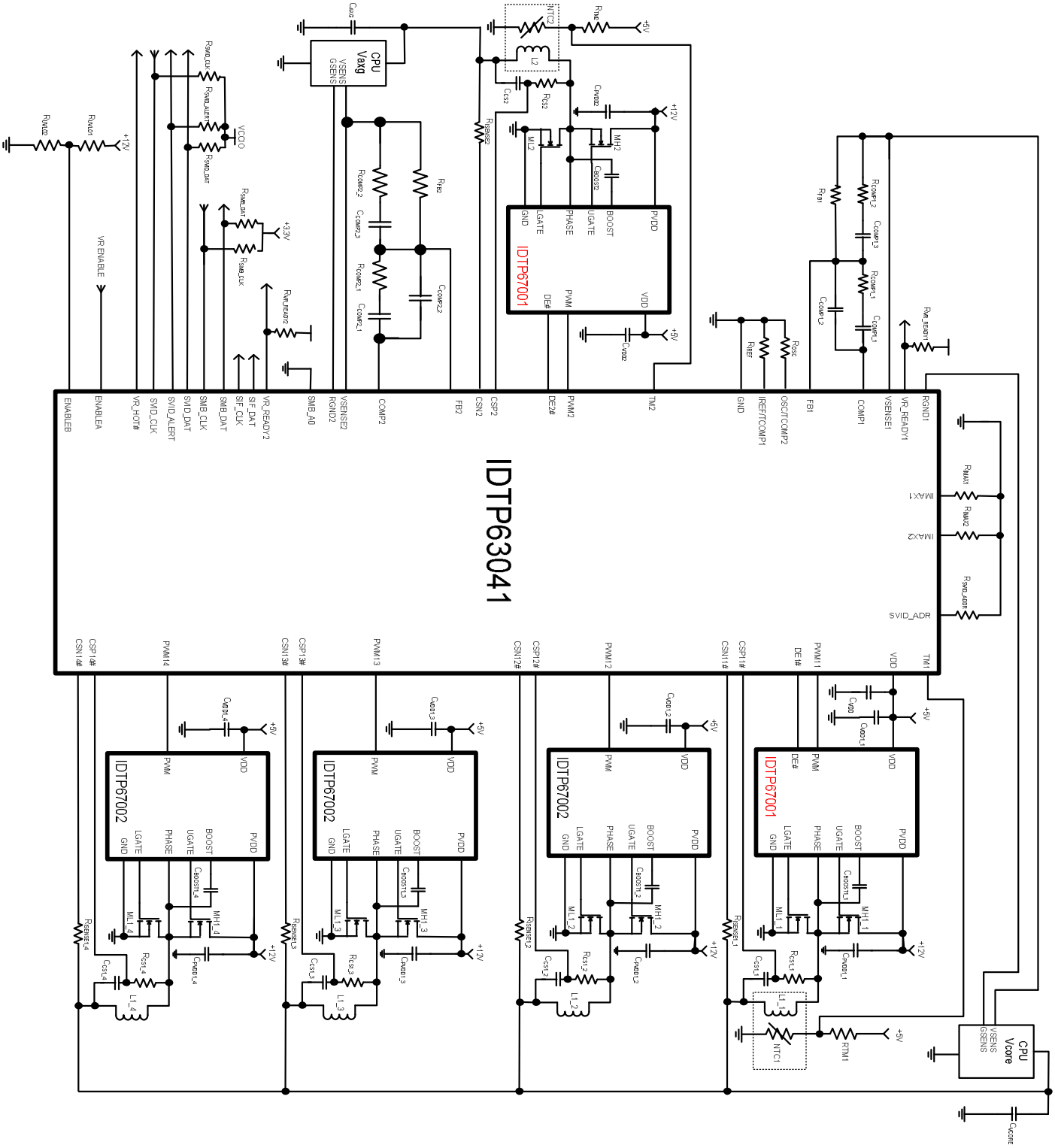
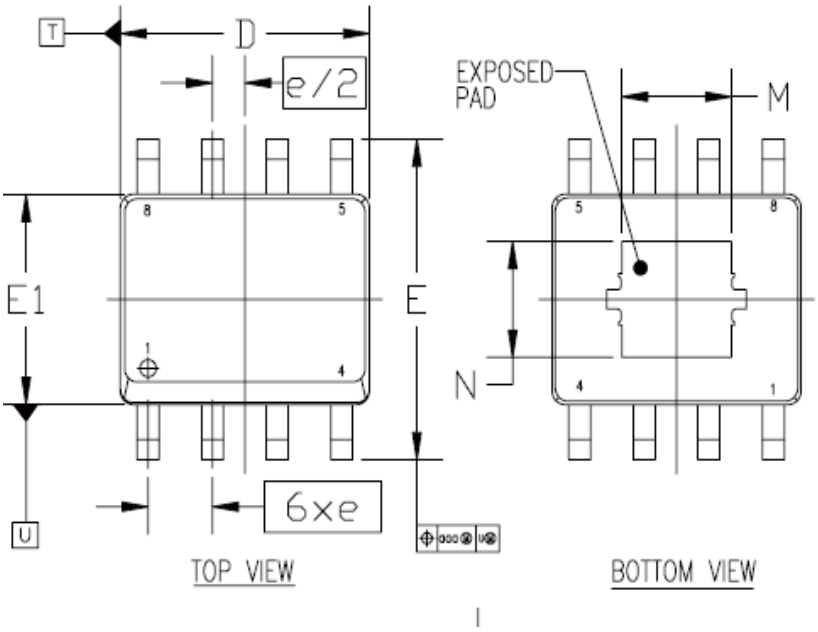


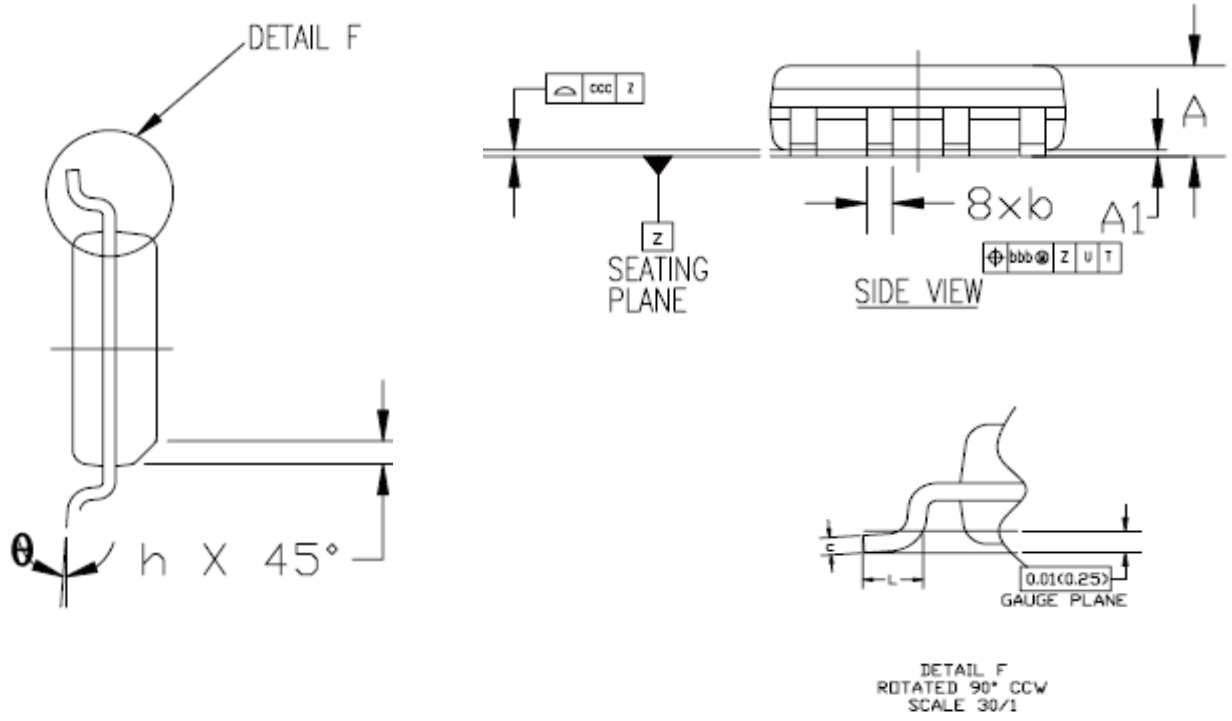
Figure 4. Typical Application Circuit for 4+1 operation

Package Outline and Package Dimensions (8-pin SO8 with exposed pad)

This part is compliant to JEDEC Standard MS-012



		INCHES			MM		
	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.051	---	.067	1.30	---	1.70
STAND OFF	A1	.002	---	.006	0.05	---	0.15
LEAD WIDTH	b	.014	---	.019	0.36	---	0.48
L/F THICKNESS	c	.007	---	.010	0.18	---	0.25
BODY SIZE	D	.189	---	.197	4.80	---	5.00
	E1	.150	---	.157	3.81	---	3.99
	E	.228	---	.224	5.79	---	6.20
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016	---	.050	0.41	---	1.27
	h	.010	---	.020	0.25	---	0.51
	θ	0°	---	8°	0°	---	8°
EP SIZE	M	.081	.085	.089	2.06	2.16	2.26
	N	.081	.085	.089	2.06	2.16	2.26
LEAD EDGE OFFSET	aaa	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	ccc	.004			0.10		



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package
P67001EXG	IDTP67001EXG	Tubes	8-pin SOIC

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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