

FCH125N65S3R0

Power MOSFET, N-Channel, SUPERFET® III, Easy Drive, 650 V, 24 A, 125 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 105 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 46 \text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(\text{eff.})} = 439 \text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

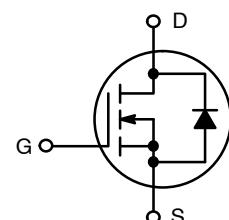
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar



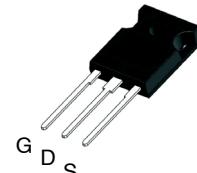
ON Semiconductor®

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V_{DSS}	$R_{DS(\text{ON}) \text{ MAX}}$	$I_D \text{ MAX}$
650 V	125 mΩ @ 10 V	24 A



N-Channel MOSFET



TO-247-3LD
CASE 340CH

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FCH125N65S3R0 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH125N65S3R0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		650	V
V _{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I _D	Drain Current	Continuous (T _C = 25°C)	24	A
		Continuous (T _C = 100°C)	15	
I _{DM}	Drain Current	Pulsed (Note 1)	60	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		115	mJ
I _{AS}	Avalanche Current (Note 2)		3.7	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		1.81	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P _D	Power Dissipation	(T _C = 25°C)	181	W
		Derate Above 25°C	1.45	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 3.7 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 12 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.69	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Quantity
FCH125N65S3R0-F155	FCH125N65S3R0	TO-247-3LD (Pb-Free)	30 Units / Tube

FCH125N65S3R0

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	0.68	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 520 V, T _C = 125°C	–	1.35	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 2.4 mA	2.5	–	4.5	V
R _{D(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A	–	105	125	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 12 A	–	16	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	1940	–	pF
C _{oss}	Output Capacitance		–	40	–	pF
C _{oss(ef)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	439	–	pF
C _{oss(er)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	62	–	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 12 A, V _{GS} = 10 V (Note 4)	–	46	–	nC
Q _{gs}	Gate to Source Gate Charge		–	12	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	19	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.5	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 12 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)	–	21	–	ns
t _r	Turn-On Rise Time		–	19	–	ns
t _{d(off)}	Turn-Off Delay Time		–	48	–	ns
t _f	Turn-Off Fall Time		–	4.6	–	ns

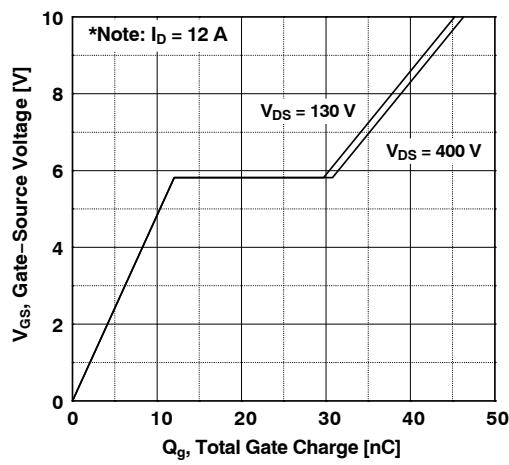
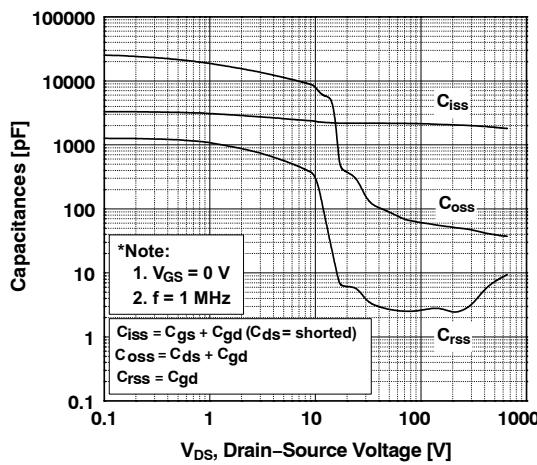
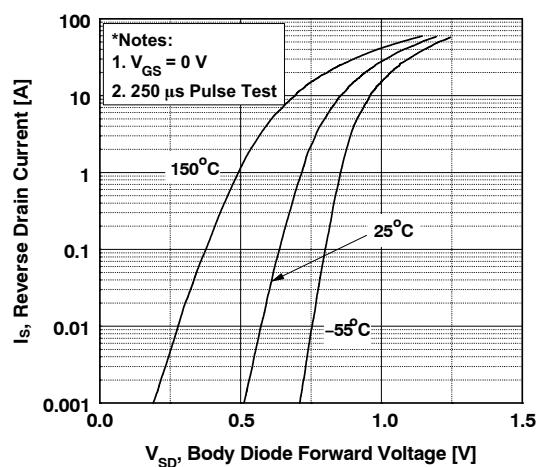
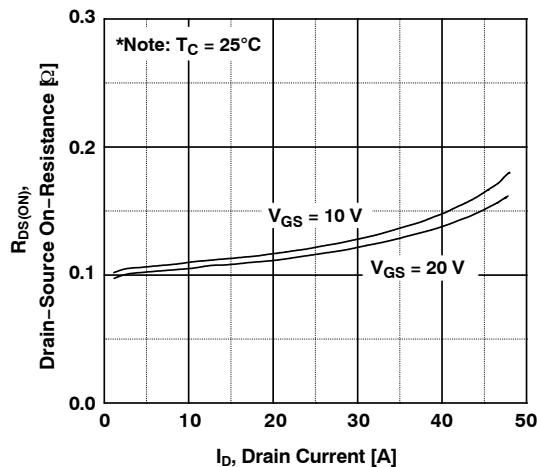
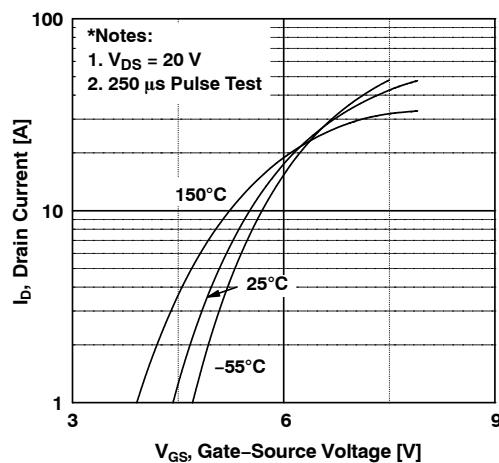
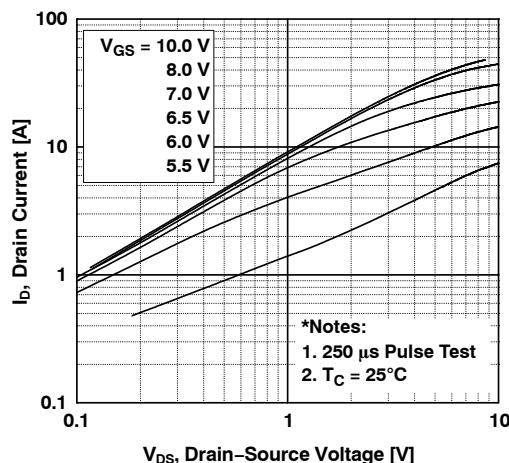
SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	24	A	
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current	–	–	60	A	
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 12 A, dI _F /dt = 100 A/μs	–	339	–	ns
Q _{rr}	Reverse Recovery Charge		–	5.7	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

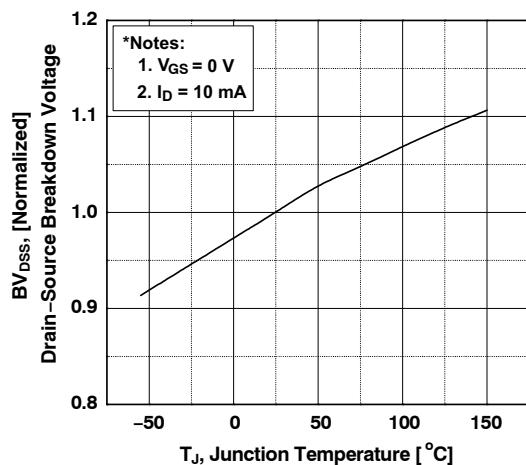


Figure 7. Breakdown Voltage Variation vs. Temperature

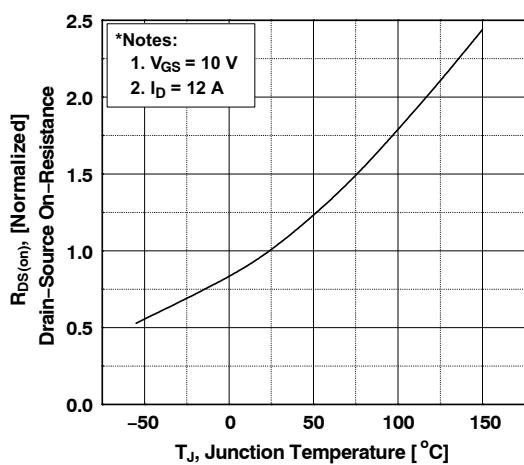


Figure 8. On-Resistance Variant vs. Temperature

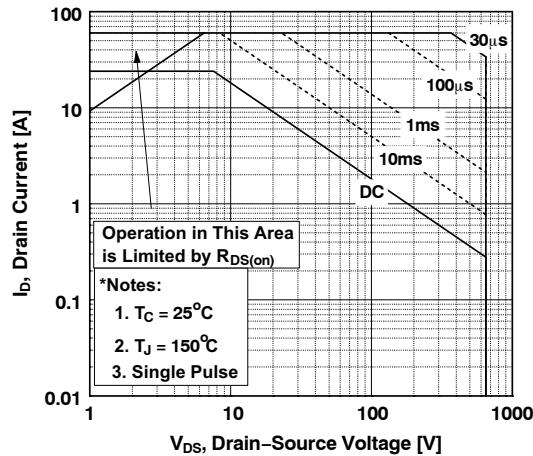


Figure 9. Maximum Safe Operation Area

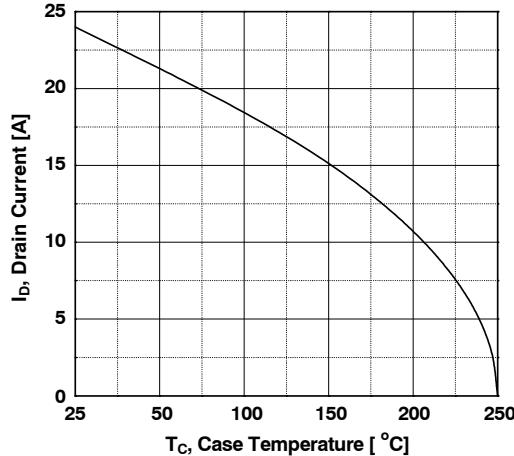


Figure 10. Maximum Drain Current vs. Case Temperature

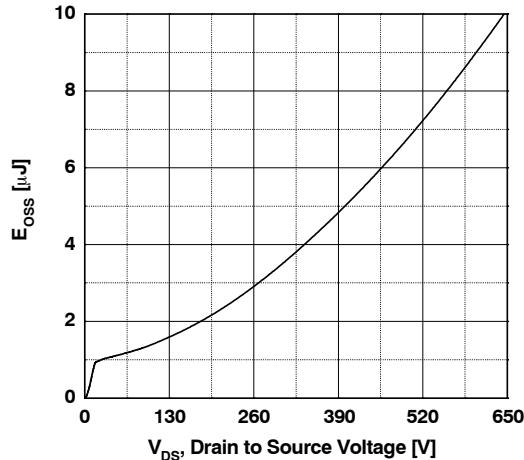


Figure 11. E_OSS vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

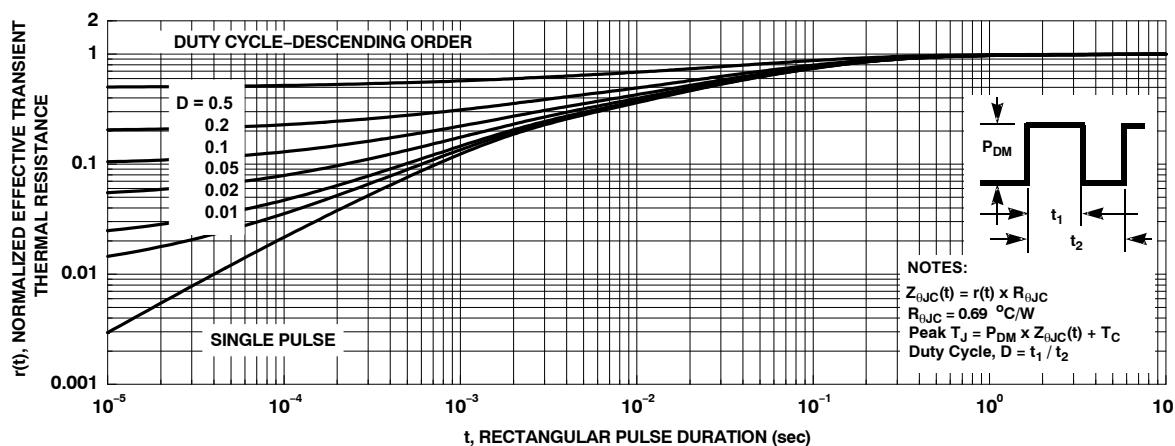


Figure 12. Transient Thermal Response Curve

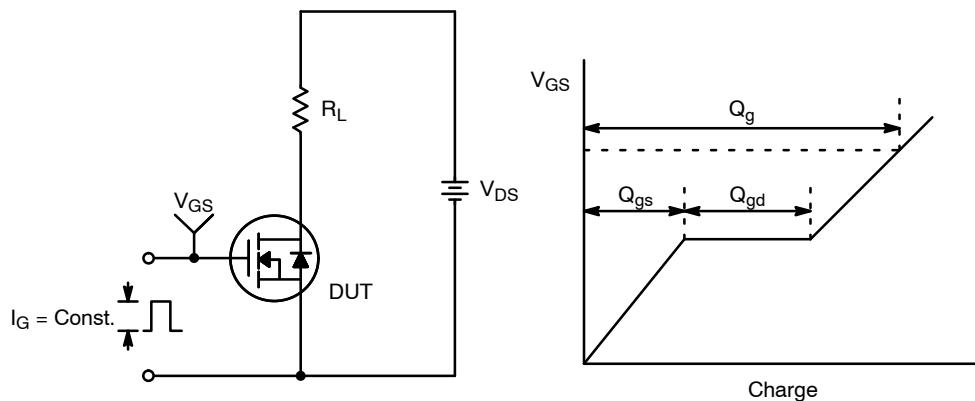


Figure 13. Gate Charge Test Circuit & Waveform

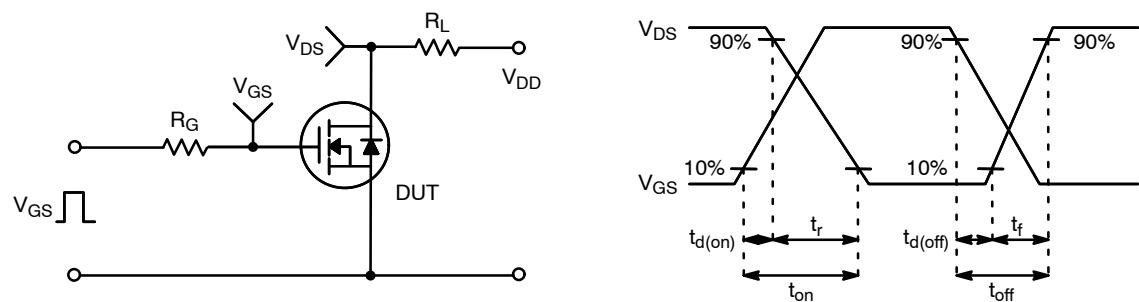


Figure 14. Resistive Switching Test Circuit & Waveforms

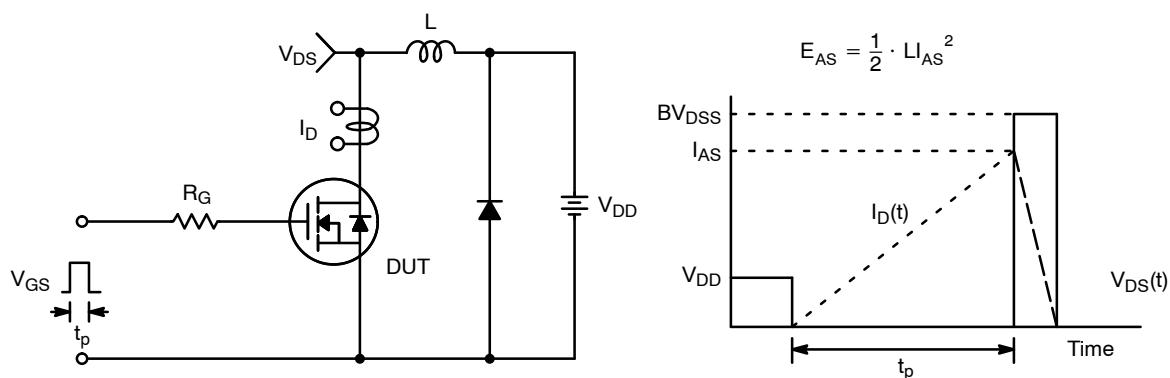


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

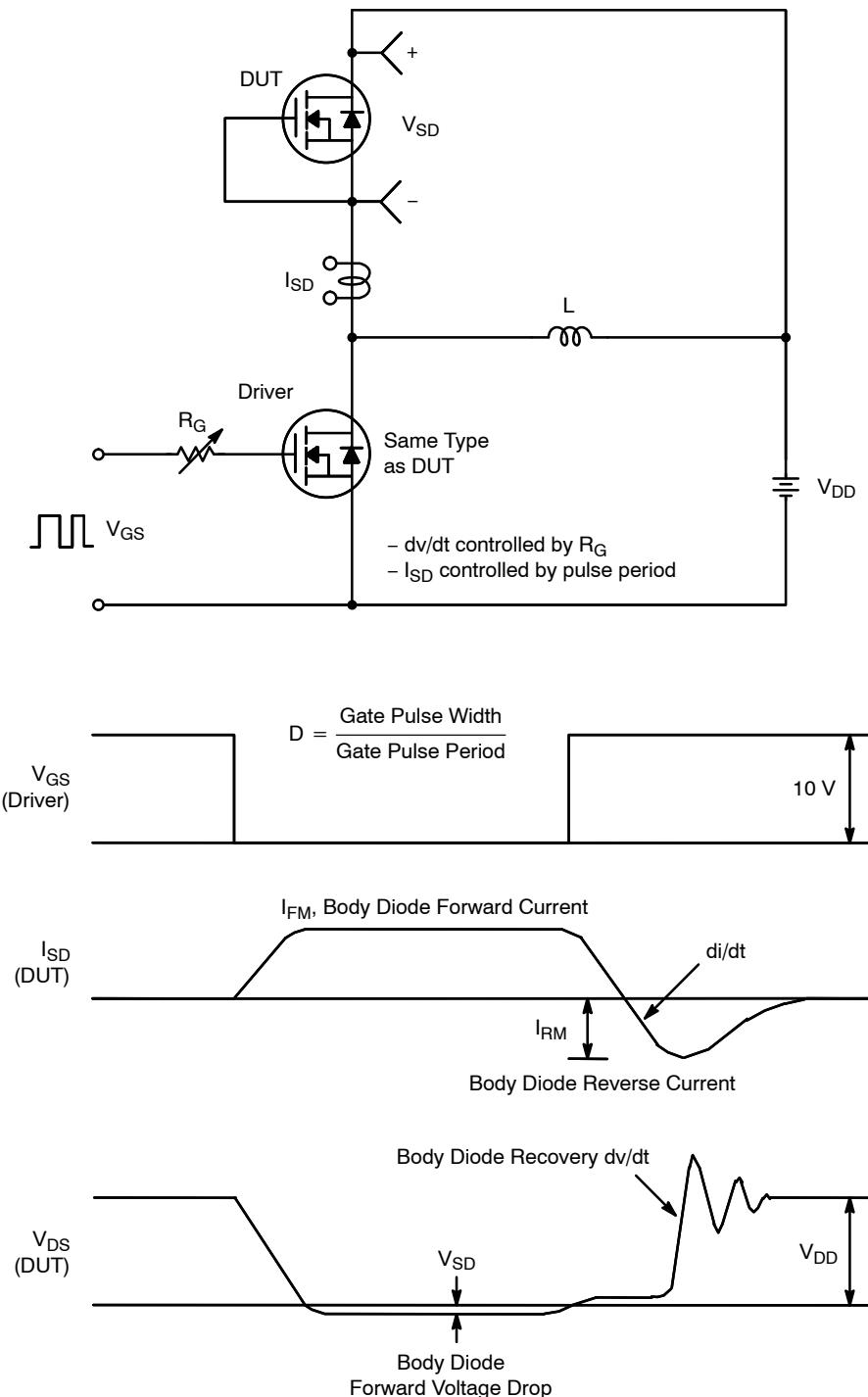
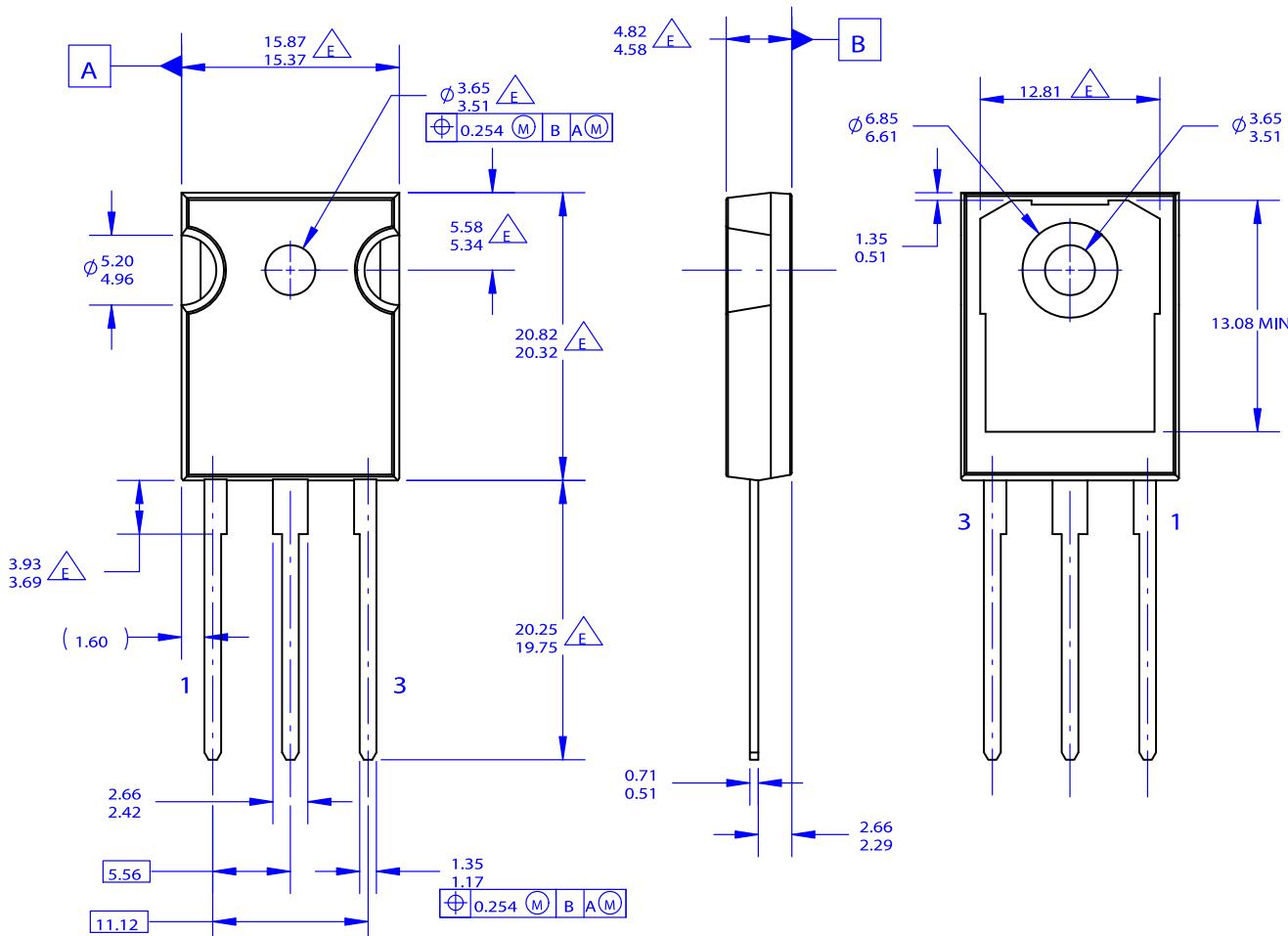


Figure 16. Peak Diode Recovery dt/dt Test Circuit & Waveforms

TO-247-3LD
CASE 340CH
ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED.

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- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

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