Brief Description

The ZSPM4141 is an ultra-low-power linear regulator optimized for minimal quiescent current losses via advanced, proprietary technology. It can improve energy efficiency and reduce heat due to power dissipation because it draws low nA-level quiescent current for light loads, yet it can regulate current loads as high as 200mA. The linear regulated output voltage is factory-configured to an option from 1.2V to 4.2V in 100mV steps. The ZSPM4141 also provides over-current protection.

Features

- Low operating voltage range: 2.5V to 5.5V
- Power-Down Mode for 100pA quiescent current
- Over-current protection: 250mA
- Output voltage options of 1.2V to 4.2V in 100mV steps (programmed at manufacturing)

Benefits

- Ultra-low 100pA quiescent current in power down mode
- Best-in-class quiescent current of 20nA at I_{LOAD}=0
- 0.5% DC line regulation (typical)
- Extends battery life
- Enables power harvesting applications
- High level of integration minimizes board space

Related IDT Smart Power Products

- ZSPM4121 Under-Voltage Load Switch for Smart Battery Management

Available Support

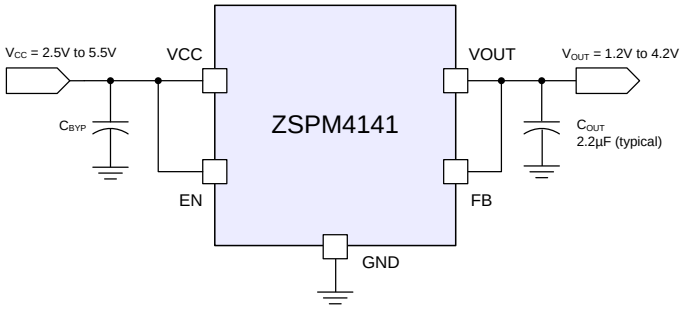
- ZSPM4141W12KIT Evaluation Kit
- Support Documentation

Physical Characteristics

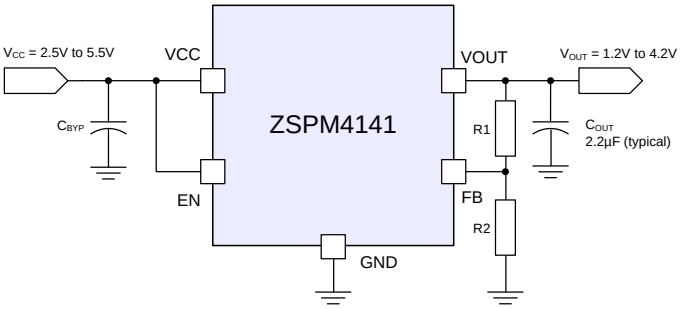
- Package: 8-pin DFN (2mm x2mm)

Typical ZSPM4141 Application Circuits

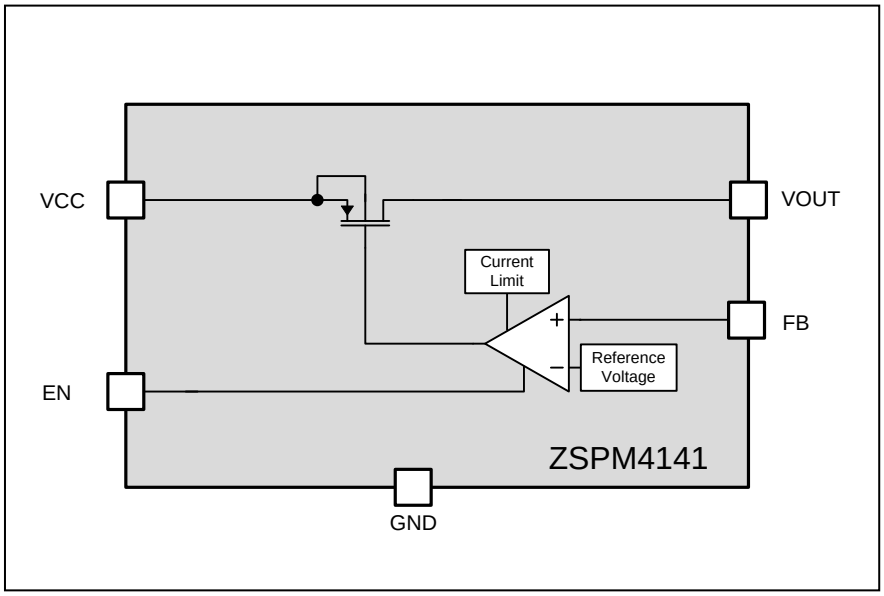
ZSPM4141 Basic (Fixed Output) Application



ZSPM4141AI1W12 Variable VOUT via Resistor Divider



ZSPM4141 Block Diagram



Typical Applications

- Portable Electronics
- Industrial
- Medical
- Smart Cards
- RFID
- Energy-Harvesting Systems

Ordering Information

Ordering Code*	Description	Package
ZSPM4141AI1*W*12	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 1.2V	8-pin DFN / Reel
ZSPM4141AI1*W*18	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 1.8V	8-pin DFN / Reel
ZSPM4141AI1*W*25	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 2.5V	8-pin DFN / Reel
ZSPM4141AI1*W*30	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 3.0V	8-pin DFN / Reel
ZSPM4141AI1*W*31	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 3.1V	8-pin DFN / Reel
ZSPM4141AI1*W*33	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 3.3V	8-pin DFN / Reel
ZSPM4141AI1*W*42	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 4.2V	8-pin DFN / Reel
ZSPM4141W12KIT	ZSPM4141 Evaluation Kit w/Vout adjusting resistors (default 1.2 Vout)	

* W for 7” reel with 2500 parts. Custom V_{OUT} values are also available: 1.2V to 4.2V (typical) in 100mV increments.

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1 ZSPM4141 Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” (section 1.3) is not implied. Exposure to absolute–maximum–rated conditions for extended periods could affect device reliability.

1.1. Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted. All voltage values are with respect to network ground terminal.

Table 1.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Maximum input/output on VCC, VOUT, EN, and FB pins		-0.3 to 6.0	V
Electrostatic Discharge – Human Body Model, according to the respective JESD22 JEDEC standard		2	kV
Electrostatic Discharge – Charged Device Model, according to the respective JESD22-C101 JEDEC standard		500	V
Operating Junction Temperature Range	T_J	-20 to 85	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Lead Temperature (soldering, 10 seconds)		260	°C

1.2. Thermal Characteristics

Table 1.2 Thermal Characteristics for 8-pin DFN (2x2) Package

θ_{JA} (°C/W) [1)]	θ_{JC} (°C/W) [2)]
73.1	10.7

1) This assumes a FR4 board only.

2) This assumes a 1oz. copper JEDEC standard board with thermal vias. See section 6.1 for more information.

1.3. Recommended Operating Conditions

Table 1.3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Unregulated Supply Input at VCC pin	V_{CC}	2.5		5.5	V
Enable Input (EN pin)	V_{EN}	0		5.0	V
Typical Regulated Supply Output Voltage	V_{OUT}	1.2		4.2	V
Operating Ambient Temperature [1)]	T_A	-20		55	°C
Operating Junction Temperature	T_J	-20		85	°C

1) Operating ambient temperature is only intended as a guideline. The operating junction temperature requirements must not be exceeded.

1.4. Electrical Characteristics

Electrical characteristics, V_{CC} = 2.5V to 5V (unless otherwise noted). Minimum and maximum characteristics tested at T_J = 25°C.

Table 1.4 Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Supply Voltage	V_{CC}		2.5		5.5	V
Input Low Logic Level	Vil_{EN}				0.3*V_{CC}	V
Input High Logic Level	Vih_{EN}		0.7*V_{CC}			V
Output Bypass Capacitor	C_{OUT}		1	2.2	4.7	µF
Input Bypass Capacitor	C_{BYP}			0.1		µF
Quiescent Current:	I_{QQ}	V_{CC} = 4.2V, I_{OUT}=0		20		nA
Quiescent Current: Power-Down Mode	I_{QQpd}	I_{OUT}=0, EN = 0		100		pA
Operating Current	I_{OP-GND}	V_{CC} = 2.5V, I_{OUT} = 200mA		200		µA
		V_{CC} = 3.3V, I_{OUT} = 200mA		200		µA
		V_{CC} = 5.5V, I_{OUT} = 200mA		200		µA
Load Capability	I_{OUT}		0		200	mA
DC Line Regulation	V_{LINE}	V_{CC} = 2.5V to 5V, V_{OUT} =1.8V, I_{OUT} = 50mA		0.5	1	%
DC Load Regulation	V_{LOAD}	V_{CC} = 4.2V, I_{OUT} = 0.02mA to 200mA, V_{OUT} = $V_{OUT,nominal}$+300mV		1	2	%
Current Limit	I_{LIMIT}	I_{OUT} measured at V_{OUT} = 0.9*$V_{OUT,nominal}$		250		mA

2 Typical Performance Characteristics

C_{IN} = 10µF and T = 25°C (unless otherwise noted)

Figure 2.1 I_{QQ} Performance vs. V_{CC}

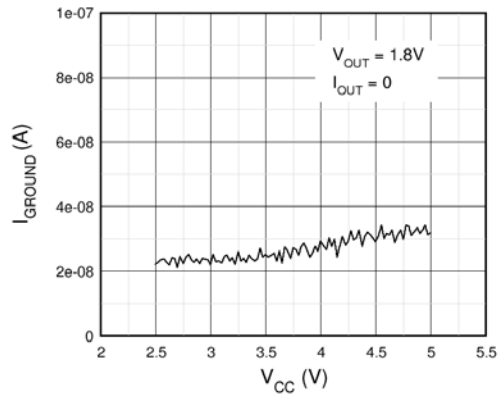


Figure 2.2 I_{QQ} Performance vs. Temperature

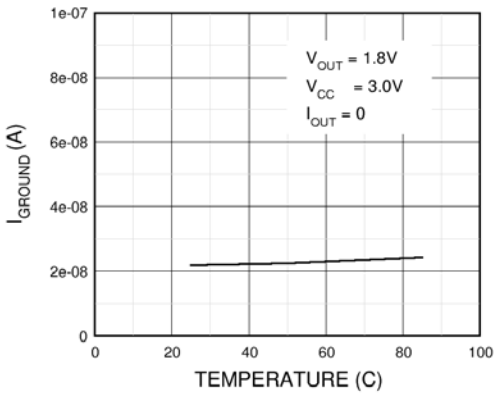


Figure 2.3 I_{QQ} Performance vs. Load Current

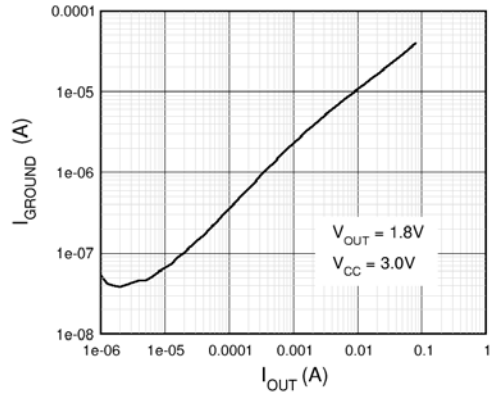


Figure 2.4 I_{QQ} Performance vs. Load Current in %

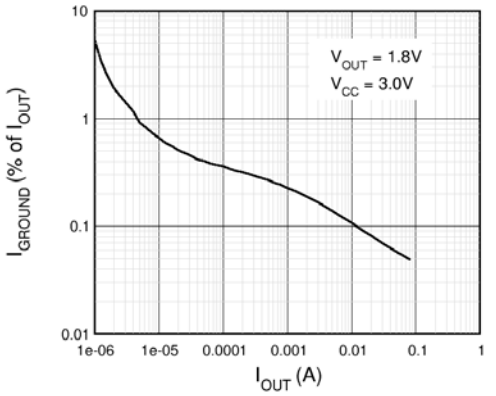


Figure 2.5 Line Regulation Performance

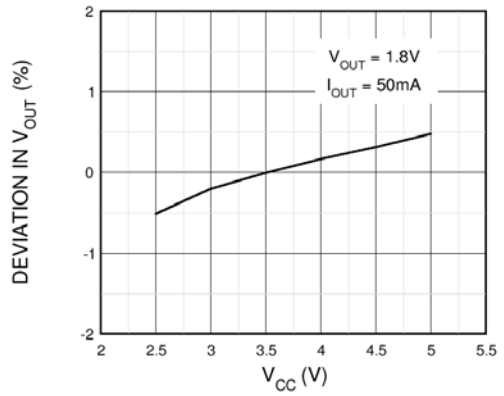


Figure 2.6 V_{OUT} Performance vs. Temperature

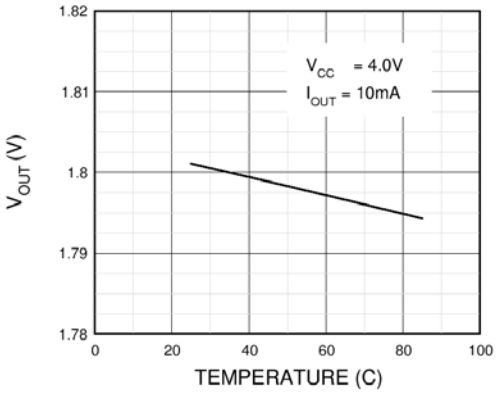
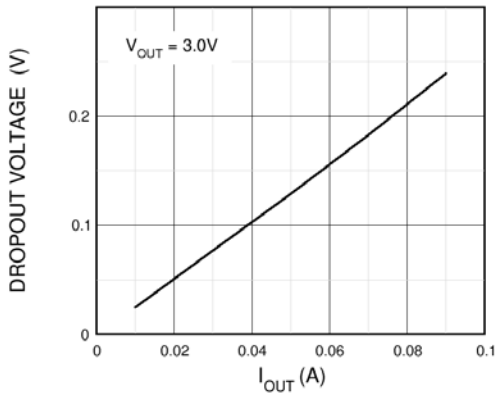


Figure 2.7 Dropout Voltage When V_{OUT} Drops By 3%



Note: Dropout voltage is defined as $V_{CC} – V_{OUT}$ when VOUT drops 3% below its nominal value.

Figure 2.8 Load Regulation Performance

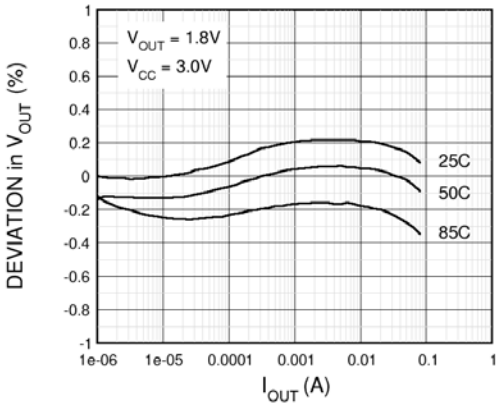


Figure 2.9 Load Step Response—I_{OUT} = 0 to 30mA

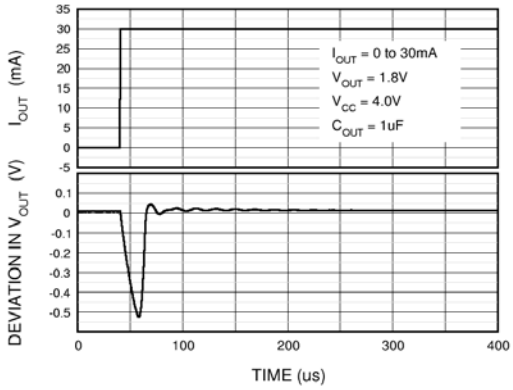


Figure 2.10 Load Step Response—I_{OUT} =30mA to 0

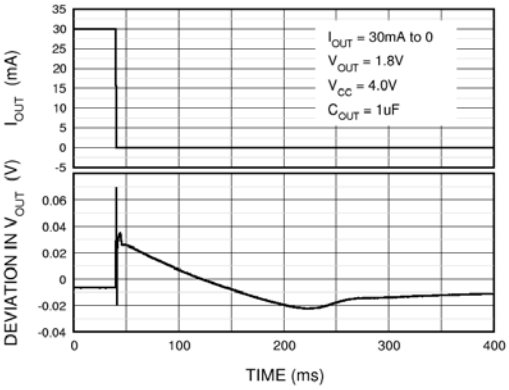


Figure 2.11 Load Step Response—I_{OUT} = 1mA to 30mA

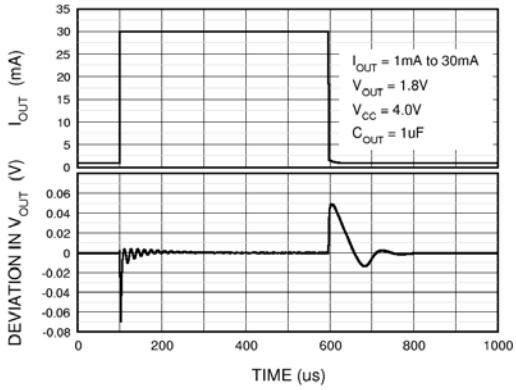


Figure 2.12 Line Step Response

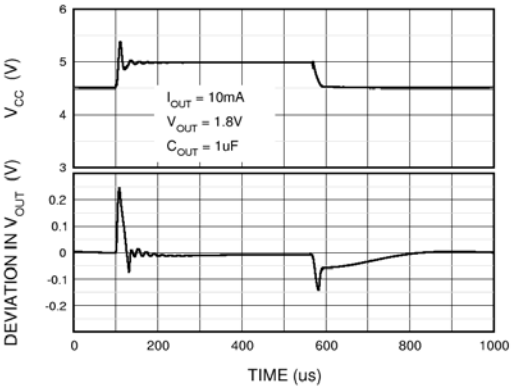
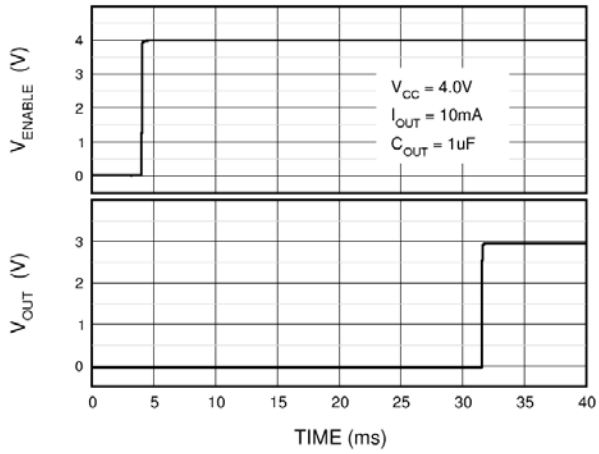


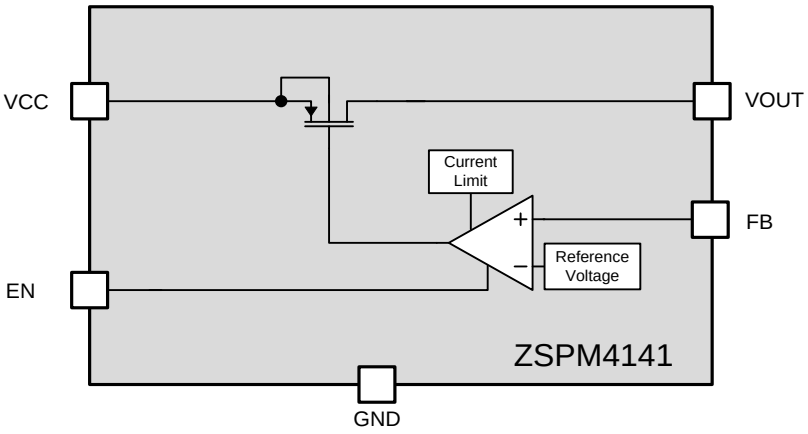
Figure 2.13 Output Enable Timing



3 Description of Circuit

The ZSPM4141 is an ultra-low-power linear regulator optimized for minimal quiescent current losses via advanced, proprietary technology. It draws low nA-level quiescent current for light loads, yet it can regulate current loads as high as 200mA. The linear regulated output voltage is factory-configured to an option from 1.2V to 4.2V in 100mV steps. The ZSPM4141 also provides over-current protection (see Table 1.4).

Figure 3.1 ZSPM4141 Block Diagram



4 Application Circuits

4.1. Selection of External Components

4.1.1. Output Bypass Capacitor C_{OUT}

Connect a bypass capacitor (C_{OUT}) from the VOUT pin to ground. The typical value for C_{OUT} is 2.2µF.

See Table 1.4 for further specifications.

4.1.2. Input Bypass Capacitor C_{BYP}

Connect a bypass capacitor (C_{BYP}) from the VCC pin to ground. The typical value for C_{OUT} is 0.1µF.

4.1.3. Output Voltage Adjustment Resistors R1 and R2

The ZSPM4141W12KIT includes a set of output adjustment resistors for R1 and R2 shown in the variable output circuit on page 2. Refer to Table 4.1 for the effect of different combinations of the resistors on the output voltage and the resulting increase in I_{QQ} current.

Table 4.1 Output Voltage Adjustment Resistors and Resulting I_{QQ} Increase

Vout	R1 (+/-0.1%)	R2 (+/-1%)	I_{QQ} increase
1.2	0		
1.5	1.00MΩ	4.02MΩ	0.30µA
1.8	1.00MΩ	2MΩ	0.60µA
3	1.00MΩ	665kΩ	1.80µA
3.3	1.00MΩ	576kΩ	2.10µA
4.2	1.00MΩ	402kΩ	3.00µA

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4.2. Typical Application Circuit

Figure 4.1 Basic ZSPM4141 Application Circuit—Fixed Output

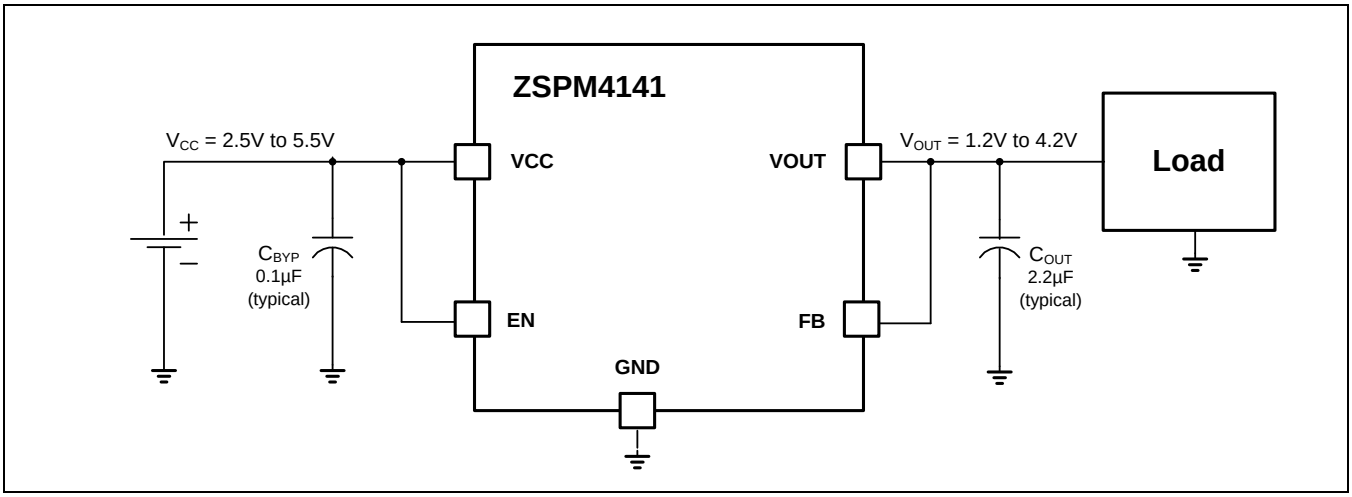
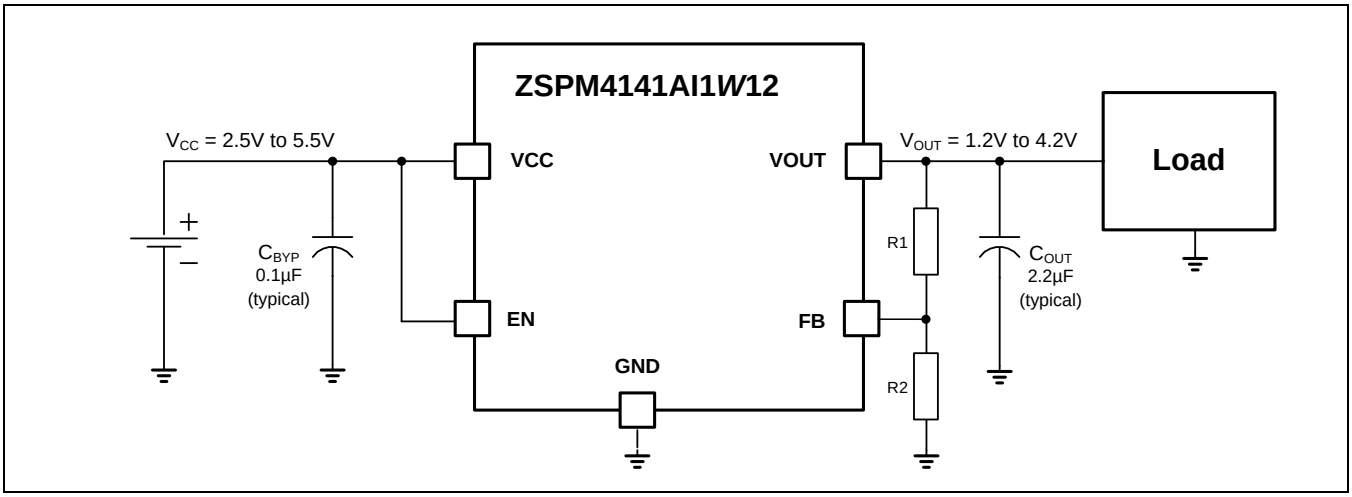


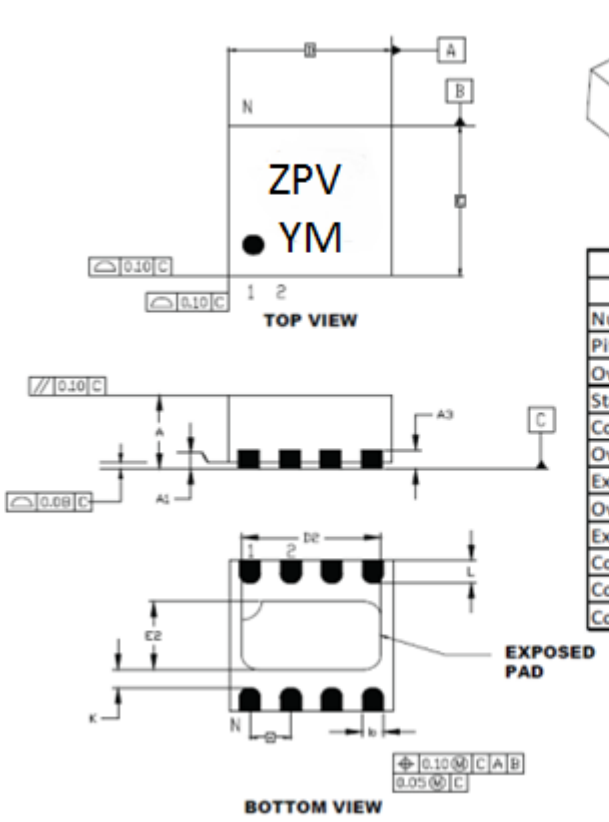
Figure 4.2 ZSPM4141AI1W12 Application Circuit—Variable Output

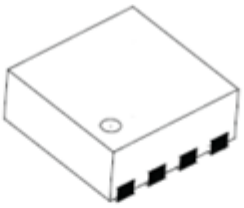


5 Pin Configuration and Package

5.1. ZSPM4141 Package Dimensions and Marking Diagram

Figure 5.1 ZSPM4141 Package Drawing





Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Width	E2	0.75	0.90	1.00
Overall Width	E		2.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
Dimensions and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

MARKING CODES:

Z: ZMDI
P: Product Code: 1 = ZSPM4141
V: Voltage levels: 0 = 1.2, 1 = 1.3, 2 = 1.4, 3 = 1.5, 4 = 1.6, 5 = 1.7, 6 = 1.8, 7 = 1.9, 8 = 2.0, 9 = 2.1, A = 2.2, B = 2.3, C = 2.4, D to U = 2.5 to 4.2
YM: Date Code (Year, Month)

The ZSPM4141 is packaged as an 8-pin DFN (2mm x2mm).

5.2. Pin Assignments

Figure 5.2 ZSPM4141 Pin Assignments (top view)

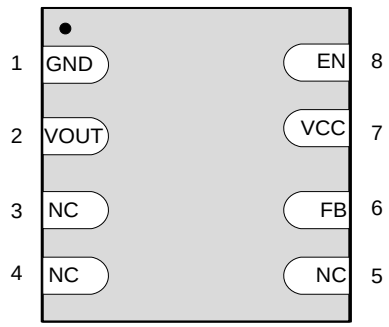


Table 5.1 Pin Description, 8-Pin DFN (2mmx2mm)

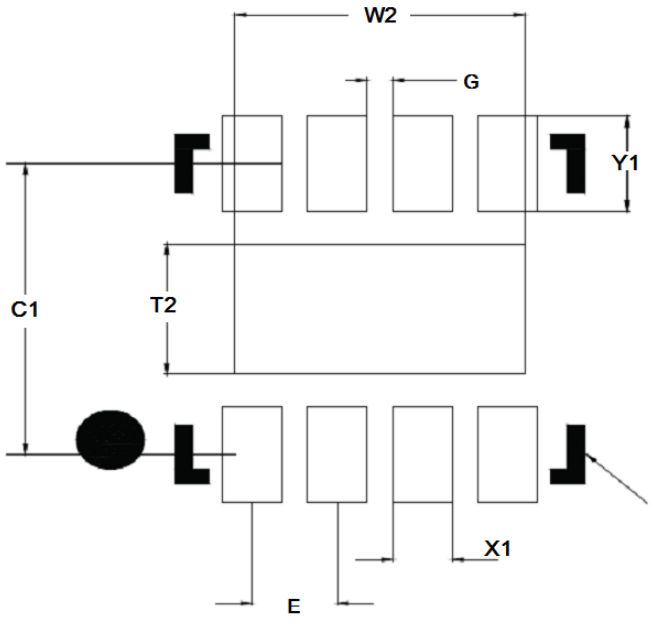
Pin #	Name	Function	Description
1	GND	Ground	GND
2	VOUT	Output	Regulated Output Voltage
3	NC		No Connection (connect to GND or float)
4	NC		No Connection (connect to GND or float)
5	NC		No Connection (connect to GND or float)
6	FB	Input	Feedback Input
7	VCC	Supply	Input Power
8	EN	Input	Enable Input

6 Layout and Soldering Requirements

To maximize the efficiency of this package for applications on a single layer or multi-layer printed circuit board (PCB), certain guidelines must be followed when laying out this part on the PCB.

6.1. Recommended Landing Pattern for PCBs

Figure 6.1 Recommended Landing Pattern for 8-Pin DFN



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	0.90
Contact Pad Spacing	C1	-	2.00	-
Contact Pad Width (X8)	X1	-	-	0.35
Contact Pad Length (X8)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

6.2. Multi-Layer PCB Layout

The following are guidelines for mounting the exposed pad ZSPM4141 on a multi-layer PCB with ground a plane. In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, and thickness of copper, etc.

Figure 6.2 Package and PCB Land Configuration for Multi-Layer PCB

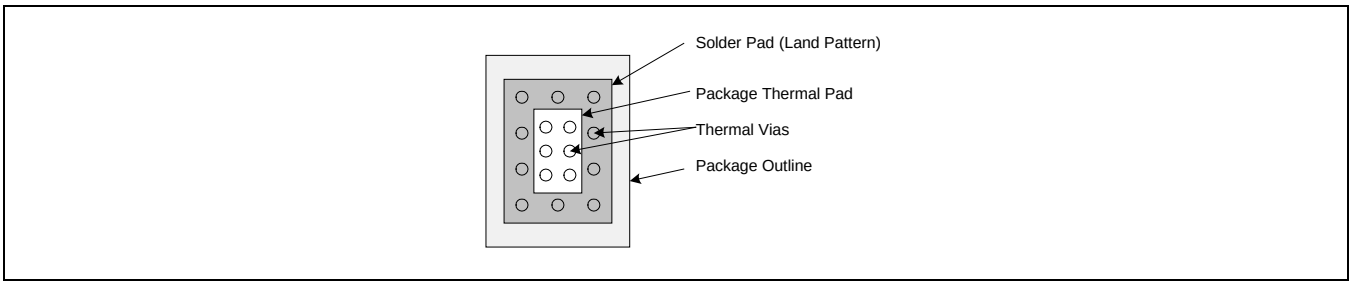


Figure 6.3 JEDEC Standard FR4 Multi-Layer Board – Cross-Sectional View

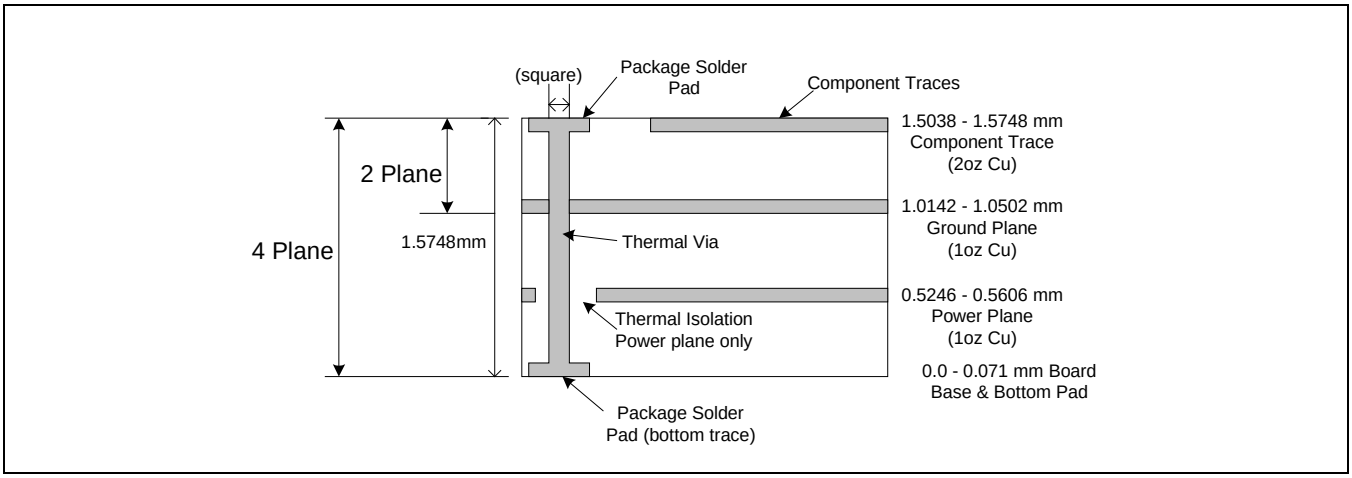
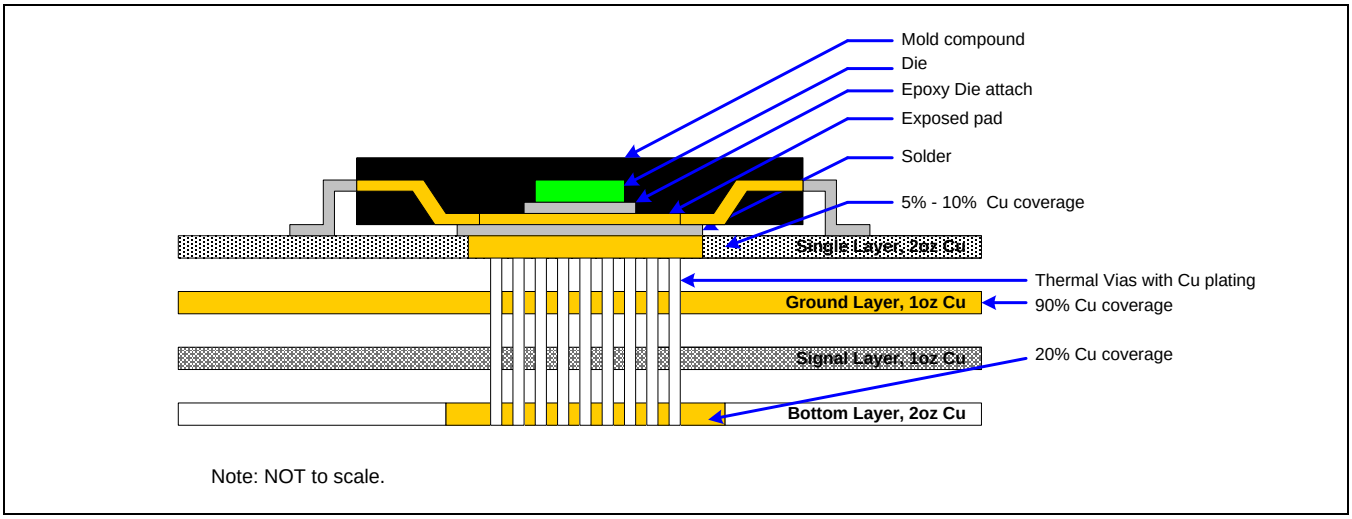


Figure 6.4 is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations, and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators might need to be de-rated for ambient temperatures above 85°C. The de-rated value will depend on calculated worst-case power dissipation and the thermal management implementation in the application.

Figure 6.4 Conducting Heat Away from the Die using an Exposed Pad Package

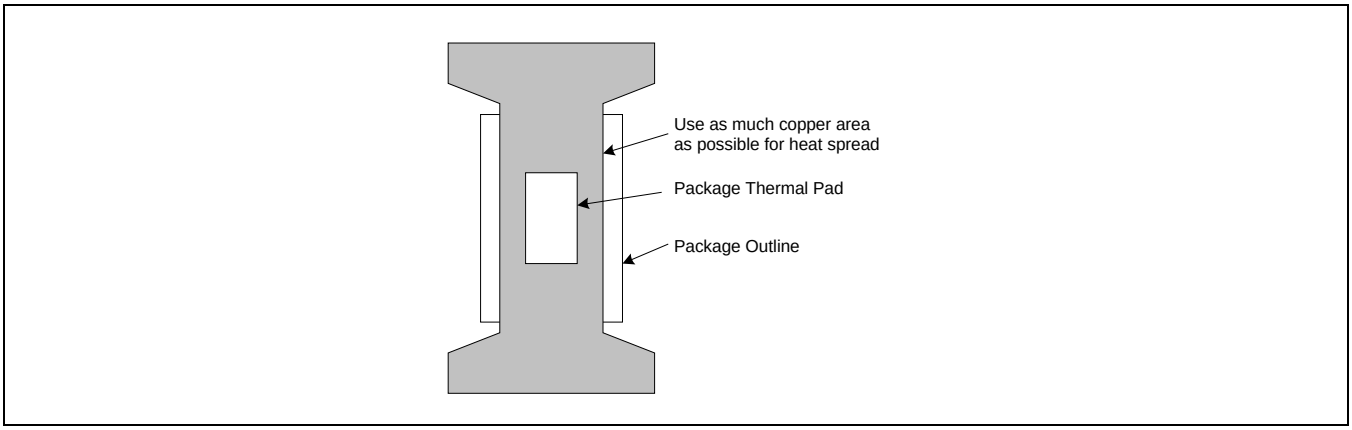


6.3. Single-Layer PCB Layout

Layout recommendation for a single-layer PCB: utilize as much copper area for power management as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above, it is advisable to use as much copper trace as possible to dissipate the heat.

Figure 6.5 Application Using a Single-Layer PCB



Important: If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

7 Ordering Information

Ordering Code*	Description	Package
ZSPM4141AI1*W*12	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 1.2V	8-pin DFN / Reel
ZSPM4141AI1*W*18	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 1.8V	8-pin DFN / Reel
ZSPM4141AI1*W*25	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 2.5V	8-pin DFN / Reel
ZSPM4141AI1*W*30	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 3.0V	8-pin DFN / Reel
ZSPM4141AI1*W*31	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 3.1V	8-pin DFN / Reel
ZSPM4141AI1*W*33	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 3.3V	8-pin DFN / Reel
ZSPM4141AI1*W*42	ZSPM4141 Ultra-Low Power Line Regulator —V_{OUT} factory set to 4.2V	8-pin DFN / Reel
ZSPM4141W12KIT	ZSPM4141 Evaluation Kit w/Vout adjusting resistors (default 1.2 Vout)	

Custom V_{OUT} values are also available: 1.2V to 4.2V (typical) in 100mV increments.

8 Related Documents

Document
ZSPM4141 Feature Sheet
ZSPM4141 Evaluation Kit Description
ZSPM4141 Application Note—Low Power Battery Control and Voltage Regulator Solutions for Remote Sensor Networks

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

9 Document Revision History

Revision	Date	Description
1.00	August 6, 2012	First release.
2.00	January 11, 2013	Addition of variable output illustration and Table 4.1. Update for ordering codes and contact information. Update for “Electrostatic Discharge” specification in Table 1.1.
	January 29, 2016	Changed to IDT branding.

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