AFBR-59E4APZ

Multimode Small Form Factor (SFF) Transceiver for Fast Ethernet with LC connector

Data Sheet

Description

The AFBR-59E4APZ is a new power saving Small Form Factor transceiver that gives the system designer a product to implement a range of solutions for multimode fiber Fast Ethernet.

This transceiver is supplied in the industry standard 2 x 5 DIP style with an LC fiber connector interface.

Transmitter

The transmitter section of the AFBR-59E4APZ transceiver utilizes a 1310 nm LED. This LED is packaged in the optical subassembly portion of the transmitter section. It is driven by an integrated circuit that converts differential LVPECL logical signals into an analog LED drive current.

Receiver

The receiver utilizes an InGaAs PIN photodiode coupled to a trans-impedance pre-amplifier IC. It is packaged in the optical subassembly of the receiver. The PIN/pre-amplifier combination is connected to a quantizer IC, which provides the final pulse shaping for data output. The data output is differential LVPECL. The Signal Detect output is single-ended. Both Data and Signal Detect outputs are LVPECL compatible.

Features

- Multisourced 2 x 5 package style
- Operates with 62.5/125 µm and 50/125 µm multimode fiber
- Single +3.3 V power supply
- Wave solder and aqueous wash process compatibility
- Manufactured in an ISO 9001 certified facility
- Compatible with the optical performance requirements of 100Base-FX version of IEEE 802.3u
- RoHS compliant
- LVPECL Signal Detect Output
- Temperature range: -40 °C to +85 °C

Application

- Fast Ethernet

Package

The package outline drawing and pinout are shown in Figure 1 and Figure 5. The details of this package outline and pinout are compliant with the multisource definition of the 2 x 5 DIP. The low profile of the Avago transceiver design complies with the maximum height allowed for the LC connector over the entire length of the package.

The optical subassemblies utilize a high-volume assembly process together with low-cost lens elements, which result in a cost-effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the ICs and various surface-mounted passive circuit elements are attached.

The receiver and transmitter sections include an internal shield for the electrical and optical subassemblies to ensure high immunity to external EMI fields.

The outer housing including the LC ports is molded of filled nonconductive plastic to provide mechanical strength. The solder posts of the Avago design are isolated from the internal circuit of the transceiver.

The transceiver is attached to a printed circuit board with the ten signal pins and the two solder posts, which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with the LC connector fiber cables.

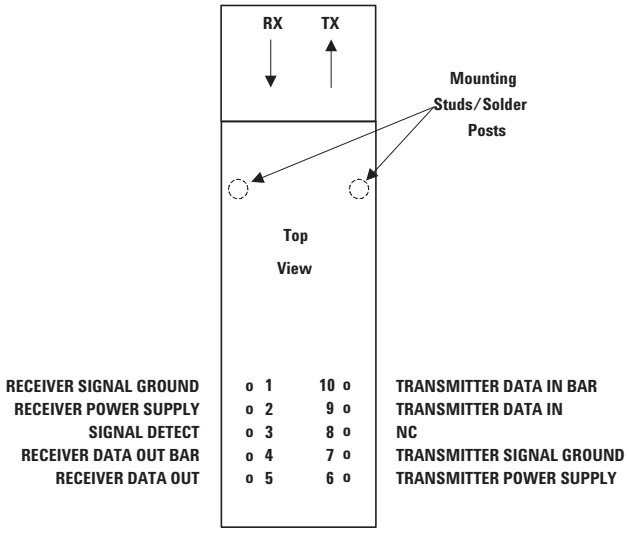


Figure 1. Pin Out Diagram

Pin Descriptions

Pin 1 Receiver Signal Ground V_{EE} RX:

Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply V_{CC} RX:

Provide +3.3 V DC via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} RX pin.

Pin 3 Signal Detect SD:

Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a logic "0" output.

Pin 4 Receiver Data Out Bar RD-:

Signal AC coupled LVPECL. See Figure 2.

Pin 5 Receiver Data Out RD+:

Signal AC coupled LVPECL. See Figure 2.

Pin 6 Transmitter Power Supply V_{CC} TX:

Provide +3.3 V DC via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pin 7 Transmitter Signal Ground V_{EE} TX:

Directly connect this pin to the transmitter ground plane.

Pin 8 NC:

Not connected.

Pin 9 Transmitter Data In TD+:

Signal AC coupled LVPECL. See Figure 2.

Pin 10 Transmitter Data In Bar TD-:

Signal AC coupled LVPECL. See Figure 2.

Mounting Studs/Solder Posts

The mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that you connect the holes in the circuit board to chassis ground.

Application Information

The Applications Engineering group is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Avago sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Avago LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The 1300 nm Avago LEDs are specified to experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Avago sales representative for additional details.

Recommended Handing Precautions

Avago recommends that normal status precautions be taken in the handling and assembly of these transceivers to prevent damage, which may be induced by electrostatic discharge (ESD). The AFBR-59E4APZ transceiver meets Jedec JESD22-A114 Class 2 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the LC receptacle.

This process plug protects the optical subassemblies during wave solder and aqueous wash processing, and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment of storage.

Board Layout - Decoupling Circuit, Ground Planes and Termination Circuits

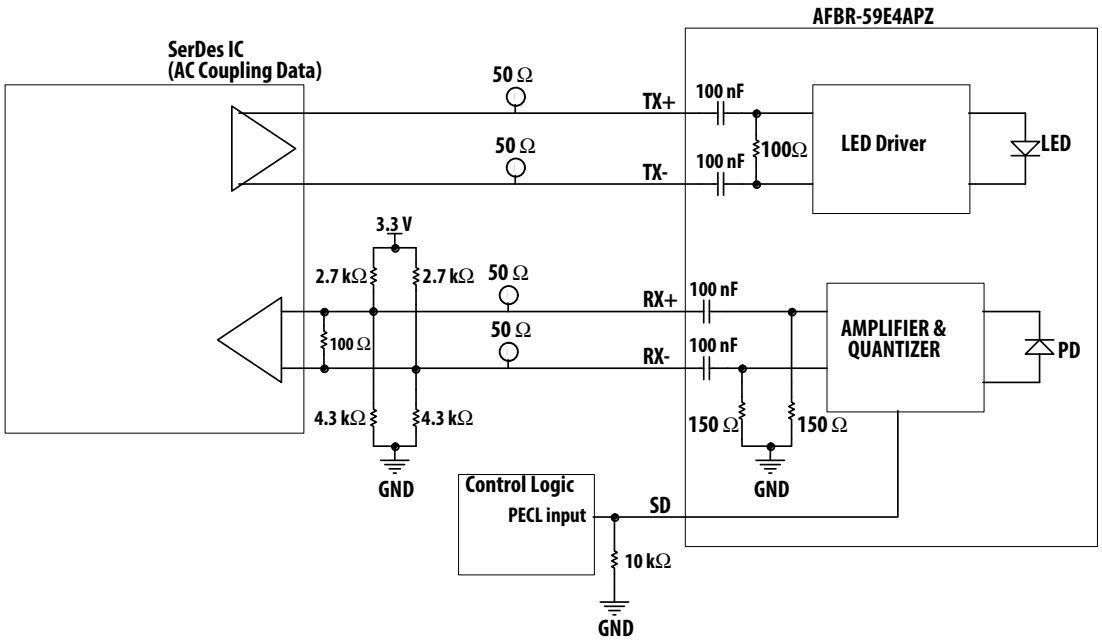
To achieve optimum performance from these transceivers, do take care in the layout of your circuit board. Figure 2 provides a schematic for a recommended termination circuit that works well with these parts, It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low-inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Figure 3 shows a recommended power supply filter.

Board Layout - Hole Pattern

The Avago transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement that defined the 2 x 5 package style. This drawing is reproduced in Figure 5 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board. Figure 5 illustrates the recommended panel opening and the position of the circuit board with respect to this panel.

Regulatory Compliance

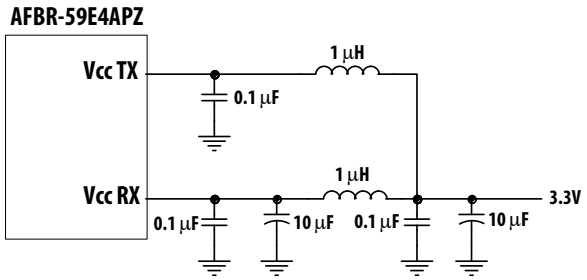
These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Avago sales representative.



Note:

Refer to SerDes supplier's recommendation regarding the interface between AFBR-59E4APZ and SerDes.
The proposed termination is recommended for LVPECL AC-coupled signals.
Other terminations could also be applicable, depending on the SerDes interface.

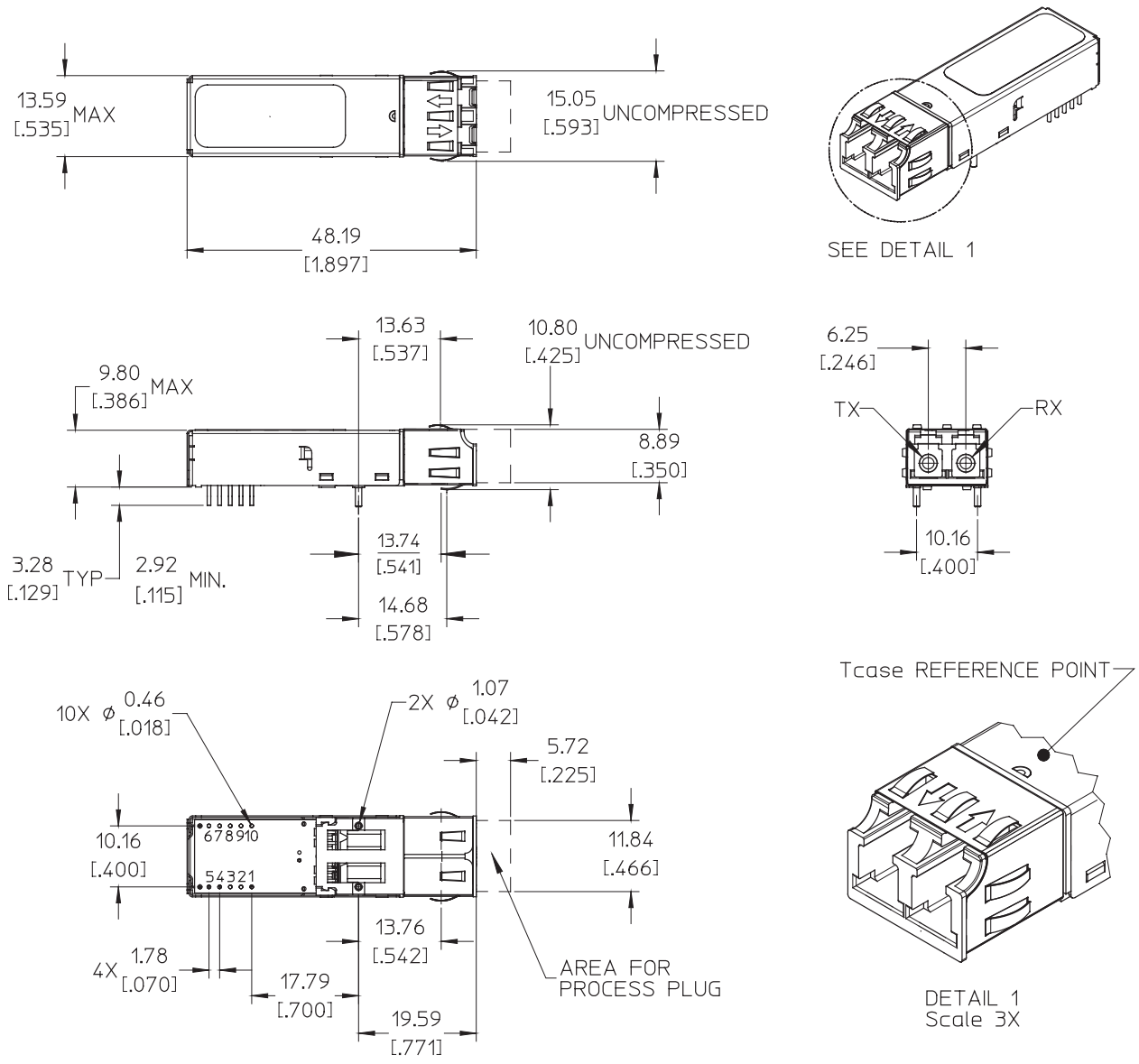
Figure 2. Recommended Termination Circuit



Note:

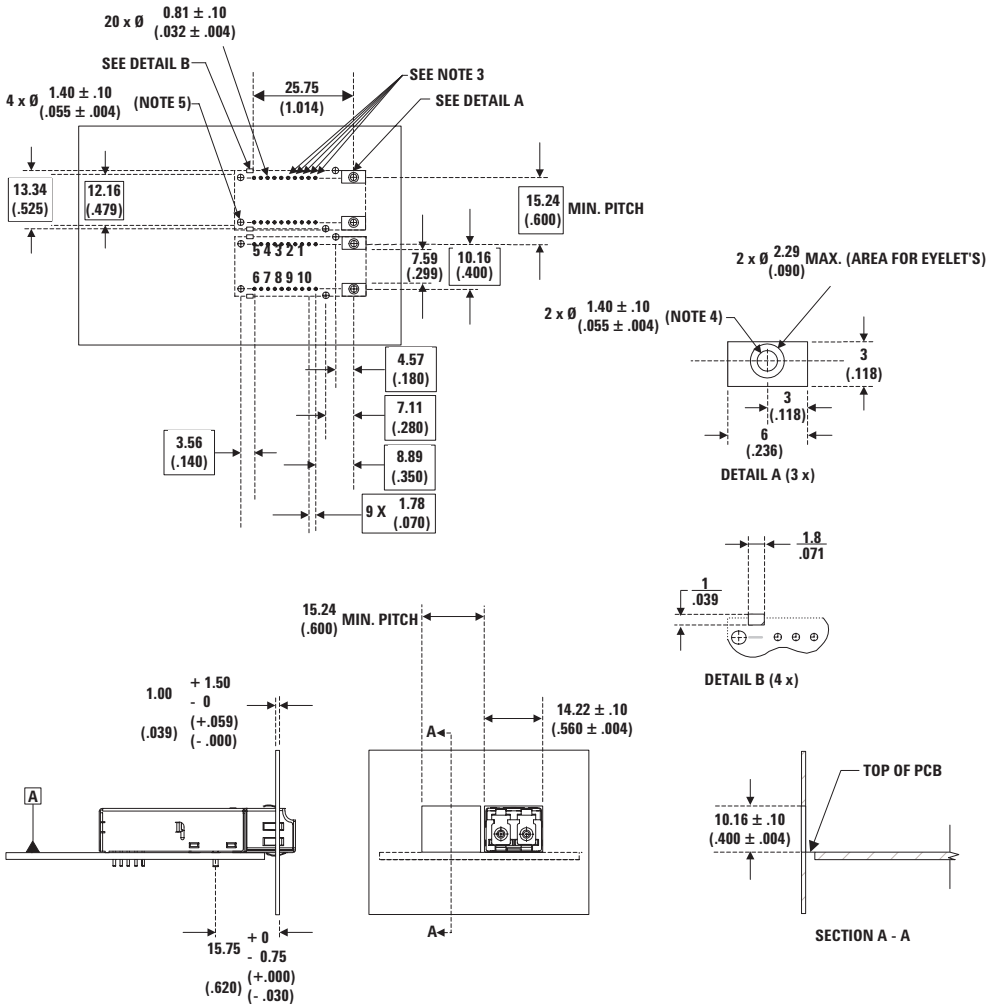
Inductors should have less than 1 Ω series resistor per MSA.

Figure 3. Recommended Power Supply Filter



All dimensions are in millimeters (inches).

Figure 4. Package Outline Drawing



Notes:

1. This page describes the recommended circuit board footprint and front panel openings for SFF transceivers.
2. The hatched areas are keep-out areas reserved for housing stand-offs. No metal traces are allowed in keep-out areas.
3. The drawing shows extra pin holes for 2x6 pin and 2x10 pin transceivers. These extra holes are not required for AFBR-59E4APZ and other 2x5 pin SFF modules.
4. Holes for mounting studs must not be tied to signal ground; they should be tied to chassis ground.
5. Holes for housing leads are not required for AFBR-59E4APZ.
6. All dimensions are in millimeters (inches).

Figure 5. Recommended Board Layout Hole Pattern

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is when the transceiver is handled before it is mounted on the circuit board. Note: Use normal ESD handling precautions for ESD-sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD-controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis that contains the transceiver parts. To the extent that the LC connector is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system-level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing this high speed transceiver from Avago will be required to meet the requirements of FCC in the United States, and CENELEC EN55022 (CISPR 22) in Europe.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

For additional information regarding EMI, susceptibility, ESD and conducted noise testing procedures and results, refer to Application Note 1166, *Minimizing Radiated Emissions of High-Speed Data Communications Systems*.

Transceiver Reliability and Performance Qualification Data

The 2 x 5 transceivers have passed Avago reliability and performance qualification testing and are undergoing ongoing quality and reliability monitoring. Details are available from your Avago sales representative.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	JEDEC JESD22-A114	Meets Class 2 (2000 to 3999 V).Withstand up to 2000 V applied between electrical pins.
Electrostatic Discharge (ESD) to the LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 9 kV without damage when the LC connector receptacle is contacted by a Human Body Model probe. Typically withstand 15 kV air discharge on LC-connector receptacle.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 Class B	Transceivers typically provide a 10 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the transceiver when mounted to a circuit card withouta chassis enclosure.
Eye Safety	EN 60950-1:2006+A11+A1+A12 EN 60825-1:2007 EN 60825-2:2004+A1+A2	Compliant per Avago testing under single fault conditions. TUV Certification - R 50236535 0003
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File #: E173874 , Vol. 1
RoHS Compliance		Reference to RoHS Directive 2011/65EU Annex II

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Storage Temperature	T_S	-40		+100	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	8
Lead Soldering Time	t_{SOLD}			10	sec	
Supply Voltage	V_{CC}	-0.5		3.63	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage (p-p)	V_D			1.9	V	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Operating Temperature	T_C	-40		+85	°C	
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Data Output Load	R_L		100		Ω	
Signaling Rate	B		125		MBd	1

Transmitter Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Supply Current	I_{CC}		80	120	mA	2
Power Dissipation	P_{DISS}		270	440	mW	
Differential Input Voltage	V_{DIFF}	0.8	1.0	1.6	V	3
Input Differential Impedance	R_{IN}		100		Ω	4

Receiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		65	85	mA	
Power Dissipation	P_{DISS}		215	310	mW	
Data Output: Differential Output Voltage (RD+/-)	$\|V_{OH} - V_{OL}\|$	0.4		2.0	V	5, 6
Data Output Rise Time (10%-90%)	t_r			2.2	ns	
Data Output Fall Time (10%-90%)	t_f			2.2	ns	
Signal Detect Output Voltage - Low	SDV_{OL}	V_{dd} - 1.81		V_{dd} - 1.62	V	7
Signal Detect Output Voltage - High	SDV_{OH}	V_{dd} - 1.02		V_{dd} - 0.88	V	7

Notes:

1. Fast Ethernet 4B/5B.
2. Typical Values are for room temperature at 3.3 V.
3. Peak to Peak.
4. Tx data inputs are AC coupled.
5. Differential output voltage is internally AC-coupled. The low and high voltages are measured using 100 Ω differential termination.
6. RD+ and RD- outputs are squelched at SD de-assert level.
7. Measured with an external 10 kΩ resistor to ground.
8. Moisture sensitivity level is MSL-1.

Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Output Optical Power 62.5/125 μm, NA = 0.275 Fiber	P_O	-20.0	-16.5	-14.0	dBm	2, 5
Output Optical Power 50/125 μm, NA = 0.20 Fiber	P_O	-23.5		-14.0	dBm	2, 5
Extinction Ratio	ER	10			dB	
Center Wavelength	λ_C	1270	1308	1380	nm	
Spectral Width - FWHM	$\Delta\lambda$		147		nm	
Optical Rise Time (10%-90%)	t_r	0.6	1.0	3.0	ns	
Optical Fall Time (10%-90%)	t_f	0.6	1.0	3.0	ns	
Duty Cycle Distortion Contributed by the Transmitter	DCD			0.6	ns	3
Data Dependent Jitter Contributed by the Transmitter	DDJ			0.6	ns	3
Random Jitter Contributed by the Transmitter	RJ			0.69	ns	1, 3

Receiver Optical and Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input Optical Power	P_{IN}	-31		-14	dBm	4, 5
Operating Wavelength	λ	1270		1380	nm	
Duty Cycle Distortion Contributed by the Receiver	DCD			0.4	ns	3, 6
Data Dependent Jitter Contributed by the Receiver	DDJ			1.0	ns	3
Random Jitter Contributed by the Receiver	RJ			2.14	ns	1, 3
Signal Detect - Assert	SD_A			-33.0	dBm	5
Signal Detect - Deassert	SD_D	-45.0			dBm	5
Signal Detect - Hysteresis	$SD_D - SD_A$	0.5	1.9		dB	
Signal Detect Assert Time (off to on)	SD_{on}	0		100	μs	7
Signal Detect Deassert Time (on to off)	SDoff	0		350	μs	8

Notes:

1. Peak to Peak.
2. Optical values are measured over the specified operating voltage and temperature ranges. The average power can be converted to a peak value by adding 3 dB.
3. Characterized with 125 MBd, $PRBS2^{7-1}$ pattern.
4. This specification is intended to indicate the performance of the receiver section of the transceiver when Optical Input Power signal characteristics are present per the following definitions
   - Over the specified operating temperature and voltage ranges
   - Bit Error Rate (BER) is better than or equal to $1x10^{-10}$
   - Transmitter is operating to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
5. Average
6. Duty Cycle Distortion contributed by the receiver is measured at 50% threshold of the electrical signal. The input optical power level is -20 dBm average.
7. Signal Detect output shall be asserted within the specified time after a step increase of the Optical Input Power.
8. Signal Detect output shall be de-asserted within the specified time after a step decrease of the Optical Input Power.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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