

# MAXIM

## CMOS 8 Bit Multiplying D/A Converter

MX7523

### General Description

The MX7523 is high performance multiplying 8 bit digital-to-analog converter (DAC). Low power CMOS technology and low cost make it suitable for a wide range of analog data acquisition and control applications.

Thin-film resistors assure 8 bit resolution with up to 10 bit linearity (L grade) over the full operating temperature range. In addition, all digital inputs are compatible with CMOS logic levels.

Maxim's MX7523 is electrically and pin compatible with the Analog Devices AD7523 and is available in a standard width 16-lead DIP as well as small outline package.

### Applications

Automatic Test Equipment  
Digital Calibration Systems  
Battery Powered Instruments  
Audio Gain Control  
Digitally Controlled Filters  
Programmable Power Supplies  
Motion Control Systems

### Features

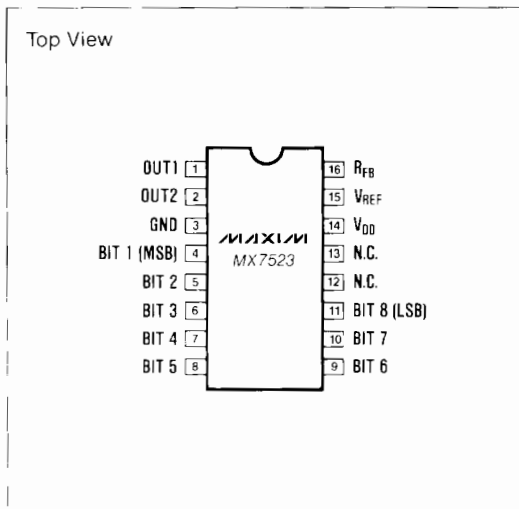
- ◆ 8, 9 and 10 Bit Linearity
- ◆  $\pm 1.5\%$  Untrimmed Gain Accuracy
- ◆ Guaranteed Monotonic
- ◆ Low Feedthrough 1/2LSB at 200kHz
- ◆ Low Power Consumption
- ◆ CMOS Compatible Logic Inputs
- ◆ Widely Second Sourced

### Ordering Information

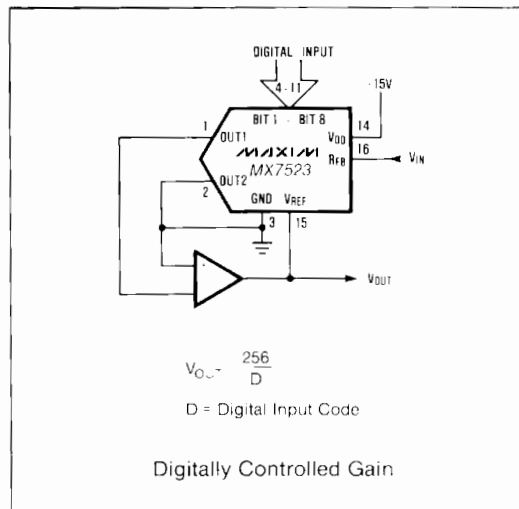
| PART       | TEMP RANGE   | PACKAGE*      | ERROR  |
|------------|--------------|---------------|--------|
| MX7523JN   | 0°C to +70°C | Plastic DIP   | 1/2LSB |
| MX7523KN   | 0°C to +70°C | Plastic DIP   | 1/4LSB |
| MX7523LN   | 0°C to +70°C | Plastic DIP   | 1/8LSB |
| MX7523JCWE | 0°C to +70°C | Small Outline | 1/2LSB |
| MX7523KCWE | 0°C to +70°C | Small Outline | 1/4LSB |
| MX7523LCWE | 0°C to +70°C | Small Outline | 1/8LSB |

\* All devices — 16 lead packages

### Pin Configuration



### Typical Operating Circuit



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## ABSOLUTE MAXIMUM RATINGS

|                                      |                 |                                      |                 |
|--------------------------------------|-----------------|--------------------------------------|-----------------|
| $V_{DD}$ to GND                      | -0.3V, +17V     | Storage Temperature                  | -65°C to +150°C |
| $V_{REF}$ to GND                     | ±25V            | Lead Temperature (Soldering 10 secs) | +300°C          |
| $R_{FB}$ to GND                      | ±25V            | Power Dissipation to +70°C           |                 |
| Digital Input Voltage to GND         | -0.3V, $V_{DD}$ | Plastic DIP                          | 670mW           |
| Output Voltage (OUT1, OUT2) (Note 1) | -0.3V, $V_{DD}$ | Small Outline                        | 450mW           |
| Operating Temperature                | 0°C to +70°C    |                                      |                 |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = +15V$ ,  $V_{REF} = +10V$ ,  $V_{OUT1} = V_{OUT2} = GND$ , unless otherwise specified)

| PARAMETER                                   | SYMBOL           | CONDITIONS                                                                                                            |                                                                | MIN.                    | TYP.       | MAX.              | UNITS              |
|---------------------------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|-------------------------|------------|-------------------|--------------------|
| DC ACCURACY                                 |                  |                                                                                                                       |                                                                |                         |            |                   |                    |
| Resolution                                  |                  |                                                                                                                       |                                                                | 8                       |            |                   | Bits               |
| Nonlinearity (Note 2)                       |                  | 0.2% FSR = 1/2LSB<br>0.1% FSR = 1/4LSB<br>0.05% FSR = 1/8LSB                                                          | J<br>K<br>L                                                    |                         |            | 1.5<br>1.0<br>0.5 | LSB                |
| Monotonicity                                |                  |                                                                                                                       |                                                                |                         | Guaranteed |                   |                    |
| Gain Error (Note 2, 3)                      |                  | Digital Inputs = V <sub>INH</sub>                                                                                     | T <sub>A</sub> = +25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub> |                         |            | 1.5<br>1.8        | % FSR              |
| Power Supply Rejection (Note 2)             | PSRR             | V <sub>DD</sub> = +14V to +15V                                                                                        | T <sub>A</sub> = +25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub> |                         |            | 0.02<br>0.03      | %/%V <sub>DD</sub> |
| Output Leakage Current                      |                  | OUT1, Digital Inputs = V <sub>INL</sub>                                                                               | T <sub>A</sub> = +25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub> |                         |            | 50<br>200         | nA                 |
|                                             |                  | OUT2, Digital Inputs = V <sub>INH</sub>                                                                               | T <sub>A</sub> = 25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub>  |                         |            | 50<br>200         |                    |
| V <sub>REF</sub> Input Resistance           | R <sub>REF</sub> | T <sub>A</sub> = +25°C                                                                                                |                                                                | 5                       | 10         | 20                | kΩ                 |
| V <sub>REF</sub> Resistance Tempco          |                  | (Note 4)                                                                                                              |                                                                |                         |            | -500              | ppm/°C             |
| AC PERFORMANCE (Note 4)                     |                  |                                                                                                                       |                                                                |                         |            |                   |                    |
| Output Current Settling Time to 0.2% of FSR |                  | R <sub>L</sub> = 100Ω, Digital Inputs = V <sub>INH</sub> to V <sub>INL</sub> and V <sub>INL</sub> to V <sub>INH</sub> | T <sub>A</sub> = +25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub> |                         |            | 150<br>200        | ns                 |
| Feedthrough Error                           |                  | Digital Inputs = V <sub>INL</sub> , V <sub>REF</sub> = 20V <sub>P-P</sub> , 200 KHz                                   | T <sub>A</sub> = +25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub> |                         |            | 1.5<br>1          | LSB                |
| Output Capacitance                          | C <sub>OUT</sub> | Digital Inputs = V <sub>INH</sub>                                                                                     | OUT1<br>OUT2                                                   |                         |            | 100<br>30         | pF                 |
|                                             |                  | Digital Inputs = V <sub>INL</sub>                                                                                     | OUT1<br>OUT2                                                   |                         |            | 30<br>100         |                    |
| DIGITAL INPUTS                              |                  |                                                                                                                       |                                                                |                         |            |                   |                    |
| Logic HIGH Threshold                        | V <sub>INH</sub> |                                                                                                                       |                                                                | +14.5                   |            |                   | V                  |
| Logic LOW Threshold                         | V <sub>INL</sub> |                                                                                                                       |                                                                |                         |            | -0.5              | V                  |
| Input Leakage Current                       |                  | Digital inputs = 0V or +15V                                                                                           |                                                                |                         |            | 1                 | μA                 |
| Input Capacitance, (Note 4)                 |                  |                                                                                                                       |                                                                |                         |            | 4                 | pF                 |
| Input Coding                                |                  | Unipolar Operation (Table 1)<br>Bipolar Operation (Table 2)                                                           |                                                                | Binary<br>Offset Binary |            |                   |                    |
| POWER REQUIREMENTS                          |                  |                                                                                                                       |                                                                |                         |            |                   |                    |
| Power Supply Range                          | V <sub>DD</sub>  | Accuracy not guaranteed over this range.                                                                              |                                                                | +5                      |            | +16               | V                  |
| Power Supply Current                        | I <sub>DD</sub>  | Digital inputs = V <sub>INH</sub> or V <sub>INL</sub>                                                                 |                                                                |                         |            | 100               | μA                 |

**Note 1:**  $V_{OUT1, 2}$  may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.

**Note 2:** Using internal feedback resistor ( $R_{FB}$ ). Full scale range (FSR) =  $-(V_{REF} - 1LSB)$  in unipolar mode.

**Note 3:** Maximum gain change from +25°C to  $T_{MIN}$  or  $T_{MAX}$  is  $\pm 0.3\%$  FSR.

**Note 4:** Guaranteed by design but not 100% tested.

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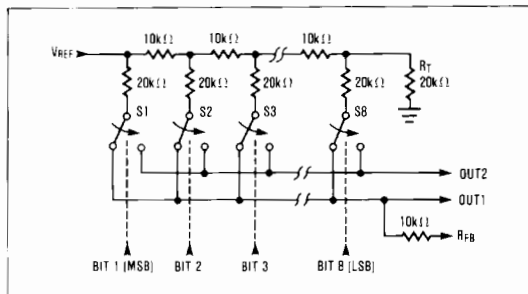


Figure 1. MX7523 Functional Diagram

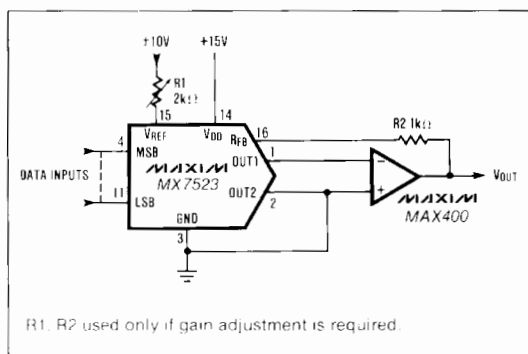


Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

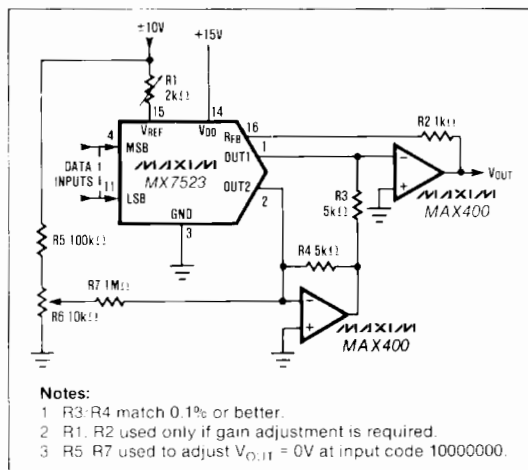


Figure 3. Bipolar (4-Quadrant) Operation

### Table 1. Unipolar Binary Code Table

| DIGITAL INPUT |   |   |   |     |   |   |   | ANALOG OUTPUT                                                  |
|---------------|---|---|---|-----|---|---|---|----------------------------------------------------------------|
| MSB           |   |   |   | LSB |   |   |   |                                                                |
| 1             | 1 | 1 | 1 | 1   | 1 | 1 | 1 | $-V_{REF} \left( \frac{225}{256} \right)$                      |
| 1             | 0 | 0 | 0 | 0   | 0 | 0 | 1 | $-V_{REF} \left( \frac{129}{256} \right)$                      |
| 1             | 0 | 0 | 0 | 0   | 0 | 0 | 0 | $-V_{REF} \left( \frac{128}{256} \right) = -\frac{V_{REF}}{2}$ |
| 0             | 1 | 1 | 1 | 1   | 1 | 1 | 1 | $-V_{REF} \left( \frac{127}{256} \right)$                      |
| 0             | 0 | 0 | 0 | 0   | 0 | 0 | 1 | $-V_{REF} \left( \frac{1}{256} \right)$                        |
| 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 | $-V_{REF} \left( \frac{0}{256} \right) = 0$                    |

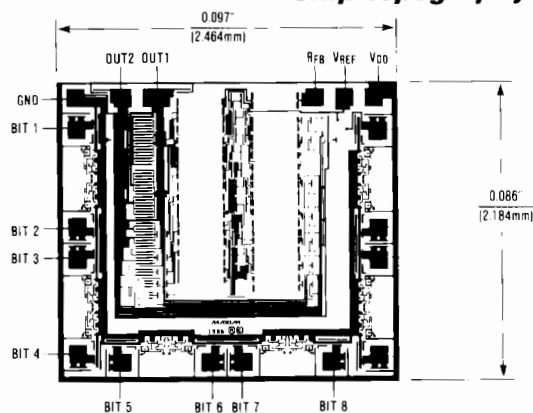
**Note:**  $1\text{LSB} = (2^{-8})(V_{\text{REF}}) = \left(\frac{1}{256}\right)(V_{\text{REF}})$

**Table 2. Bipolar (Offset Binary) Code Table**

| DIGITAL INPUT |   |   |   |     |   |   |   | ANALOG OUTPUT                             |
|---------------|---|---|---|-----|---|---|---|-------------------------------------------|
| MSB           |   |   |   | LSB |   |   |   |                                           |
| 1             | 1 | 1 | 1 | 1   | 1 | 1 | 1 | $-V_{REF} \left( \frac{127}{128} \right)$ |
| 1             | 0 | 0 | 0 | 0   | 0 | 0 | 1 | $-V_{REF} \left( \frac{1}{128} \right)$   |
| 1             | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0                                         |
| 0             | 1 | 1 | 1 | 1   | 1 | 1 | 1 | $+V_{REF} \left( -\frac{1}{128} \right)$  |
| 0             | 0 | 0 | 0 | 0   | 0 | 0 | 1 | $+V_{REF} \left( \frac{127}{128} \right)$ |
| 0             | 0 | 0 | 0 | 0   | 0 | 0 | 0 | $+V_{REF} \left( \frac{128}{128} \right)$ |

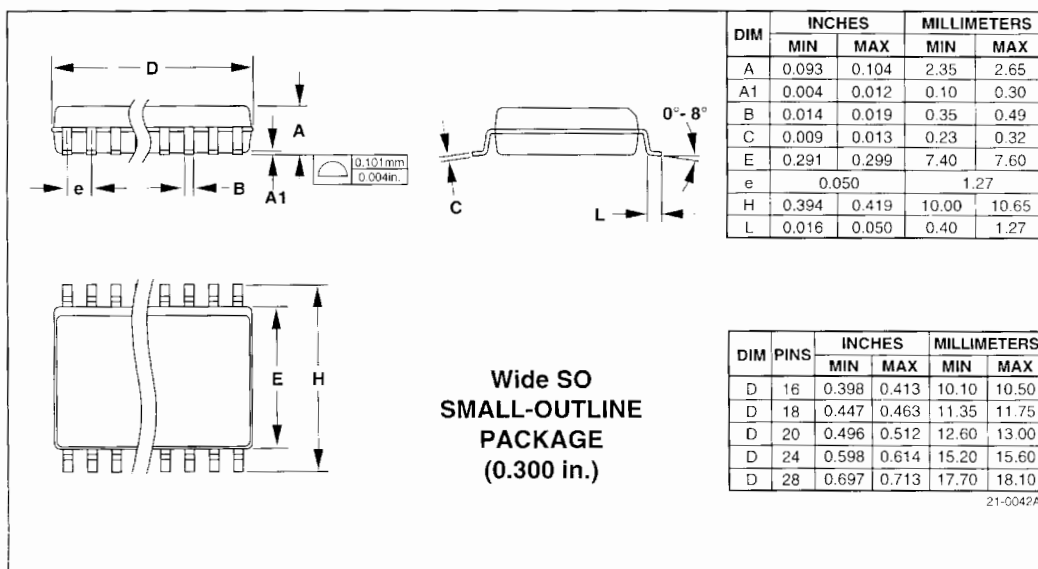
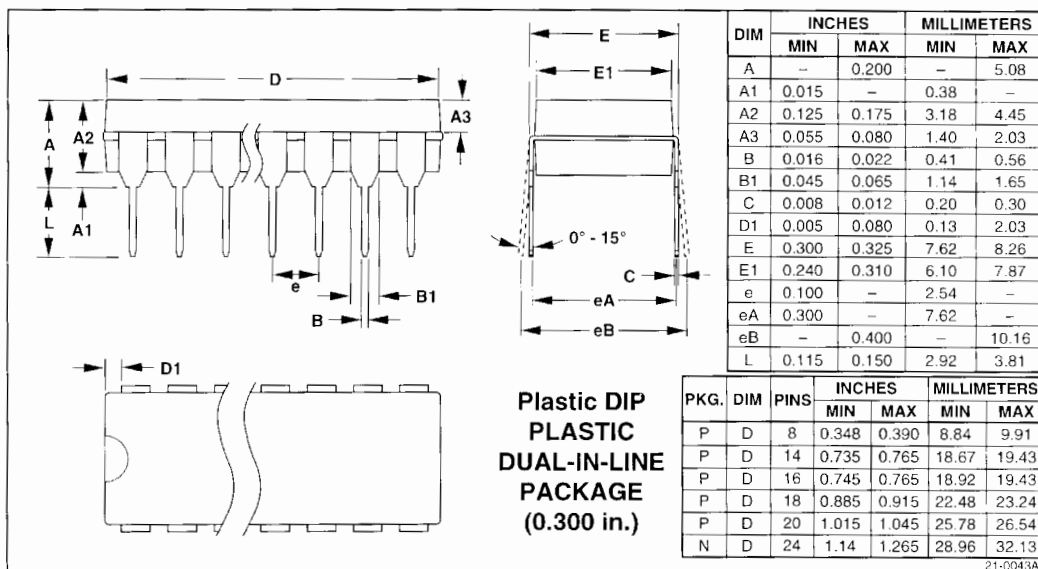
**Note:**  $1\text{LSB} = (2^{-7})(V_{\text{REF}}) = \left(\frac{1}{128}\right) (V_{\text{REF}})$

## Chip Topography



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## Package Information



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