GaAs, pHEMT, MMIC, Medium Power Amplifier, 24 GHz to 35 GHz

Data Sheet **HMC1131**

FEATURES

- High saturated output power (P_{SAT}): 25 dBm
- High output third-order intercept (IP3): 35 dBm
- High gain: 22 dB (24 GHz to 27 GHz)
- High output power for 1 dB compression (P1dB): 24 dBm
- DC supply: 5 V at 225 mA
- Compact 24-lead, 4 mm × 4 mm LCC package

APPLICATIONS

- Point-to-point radios
- Point-to-multipoint radios
- VSAT and SATCOM

FUNCTIONAL BLOCK DIAGRAM

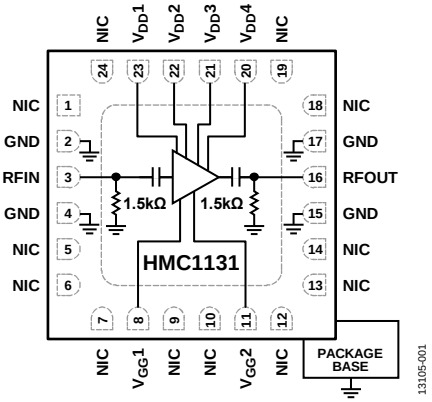

Figure 1.

GENERAL DESCRIPTION

The HMC1131 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), driver amplifier that operates from 24 GHz to 35 GHz. The HMC1131 provides 22 dB of gain at the 24 GHz to 27 GHz range, 35 dBm output IP3, and 24 dBm of output power at 1 dB gain compression, while requiring 225 mA from a 5 V supply.

The HMC1131 is capable of supplying 25 dBm of saturated output power and is housed in a compact, 4 mm × 4 mm ceramic leadless chip carrier (24-lead LCC). The HMC1131 is an ideal driver amplifier for a wide range of applications, including point-to-point radios, from 24 GHz to 35 GHz.

Rev. C
Document Feedback

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REVISION HISTORY

5/2019—Rev. B to Rev. C

Changes to Figure 32 and Table 5 13
Changes to Ordering Guide 15

6/2017—Rev. A to Rev. B

Changes to Table 5 12
Updated Outline Dimensions 14
Changes to Ordering Guide 14

9/2015—Rev. 0 to Rev. A

Changes to Features Section and General Description Section 1
Change to Gain Parameter, Table 1 3

7/2015—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

24 GHz TO 27 GHz FREQUENCY RANGE

T_A = 25°C, $V_{DD}1 = V_{DD}2 = V_{DD}3 = V_{DD}4$ = 5 V, I_{DD} = 225 mA, unless otherwise stated. Adjust $V_{GG}1$ and $V_{GG}2$ between −2 V to 0 V to achieve I_{DD} = 225 mA typical.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
FREQUENCY RANGE		24		27	GHz
GAIN		18	22		dB
Gain Variation Over Temperature			0.031		dB/°C
RETURN LOSS					
Input			8		dB
Output			7		dB
OUTPUT					
Output Power for 1 dB Compression	P1dB	20	23		dBm
Saturated Output Power	P_{SAT}		27		dBm
Output Third-Order Intercept[1]	IP3		34		dBm
SUPPLY CURRENT					
Total Supply Current	I_{DD}		225		mA
Total Supply Current vs. V_{DD}[2]			4		V
			5		V

[1] Measurement taken at P_{OUT}/tone = 10 dBm.
[2] The amplifier operates over the full voltage ranges shown. $V_{GG}1$ and $V_{GG}2$ are adjusted to achieve I_{DD} = 225 mA at 5 V.

27 GHz TO 35 GHz FREQUENCY RANGE

T_A = 25°C, $V_{DD}1 = V_{DD}2 = V_{DD}3 = V_{DD}4$ = 5 V, I_{DD} = 225 mA, unless otherwise stated. Adjust $V_{GG}1$ and $V_{GG}2$ between −2 V to 0 V to achieve I_{DD} = 225 mA typical.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
FREQUENCY RANGE		27		35	GHz
GAIN		18	20		dB
Gain Variation Over Temperature			0.031		dB/°C
RETURN LOSS					
Input			8		dB
Output			7		dB
OUTPUT					
Output Power for 1 dB Compression	P1dB	21	24		dBm
Saturated Output Power	P_{SAT}		25		dBm
Output Third-Order Intercept[1]	IP3		35		dBm
SUPPLY CURRENT					
Total Supply Current	I_{DD}		225		mA
Total Supply Current vs. V_{DD}[2]			4		V
			5		V

[1] Measurement taken at P_{OUT}/tone = 10 dBm.
[2] The amplifier operates over the full voltage ranges shown. $V_{GG}1$ and $V_{GG}2$ are adjusted to achieve I_{DD} = 225 mA at 5 V.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Bias Voltage (V_{DD})	5.5 V
RF Input Power (RFIN)	12 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 22 mW/°C)	1.97 W
Thermal Resistance, R_{TH} (Junction to Ground Paddle)	45.5°C/W
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
ESD Sensitivity, Human Body Model (HBM)	Class 0, passed 150 V
Maximum Peak Reflow Temperature	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

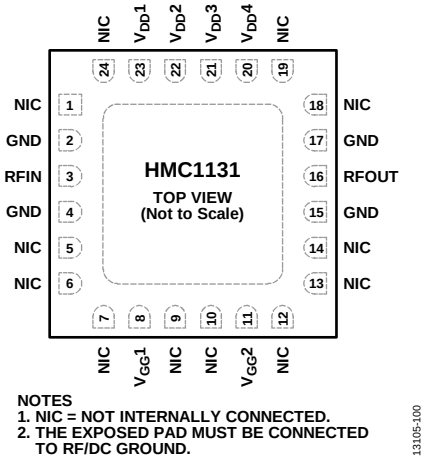

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5 to 7, 9, 10, 12 to 14, 18, 19, 24	NIC	Not Internally Connected. However, all data was measured with these pins connected to RF/dc ground externally.
2, 4, 15, 17	GND	Ground. These pins must be connected to RF/dc ground.
3	RFIN	RF Input. This pin is ac-coupled and matched to 50 Ω.
8	$V_{GG}1$	Gate Bias Pin for the First and Second Stages. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required for this pin.
11	$V_{GG}2$	Gate Bias Pin for the Third and Fourth Stages. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required for this pin.
16	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω.
20 to 23	$V_{DD}4$ to $V_{DD}1$	Drain Bias Voltage Pins. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required for these pins.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

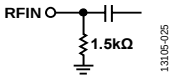

Figure 3. RFIN Interface Schematic

Figure 4. GND Interface Schematic

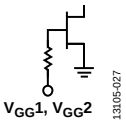

Figure 5. $V_{GG}1/V_{GG}2$ Interface Schematic

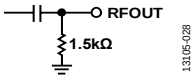

Figure 6. RFOUT Interface Schematic

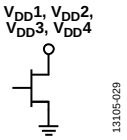

Figure 7. $V_{DD}1$ to $V_{DD}4$ Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

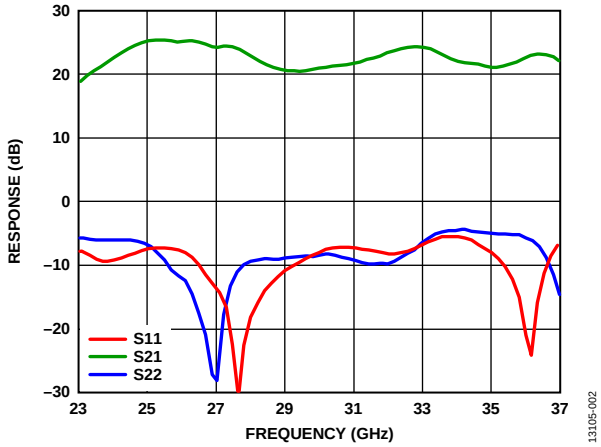

Figure 8. Response (Broadband Gain and Return Loss) vs. Frequency

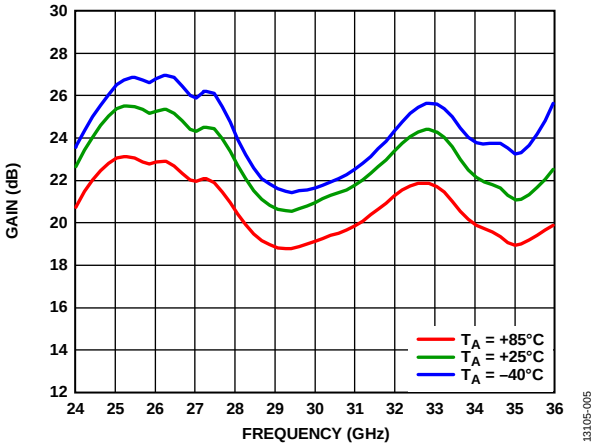

Figure 11. Gain vs. Frequency at Various Temperatures

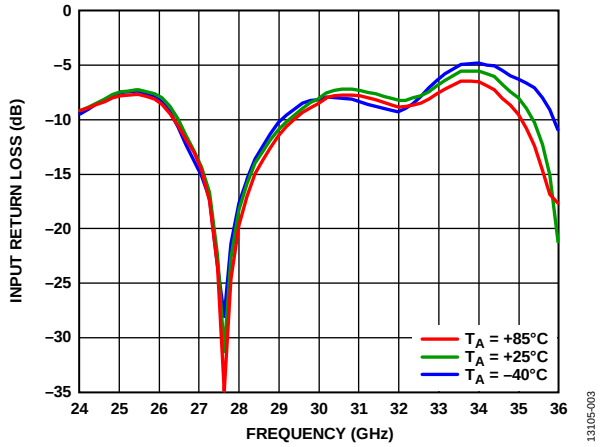

Figure 9. Input Return Loss vs. Frequency at Various Temperatures

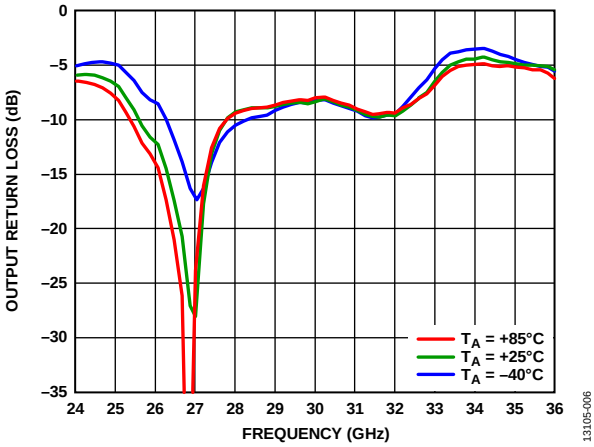

Figure 12. Output Return Loss vs. Frequency at Various Temperatures

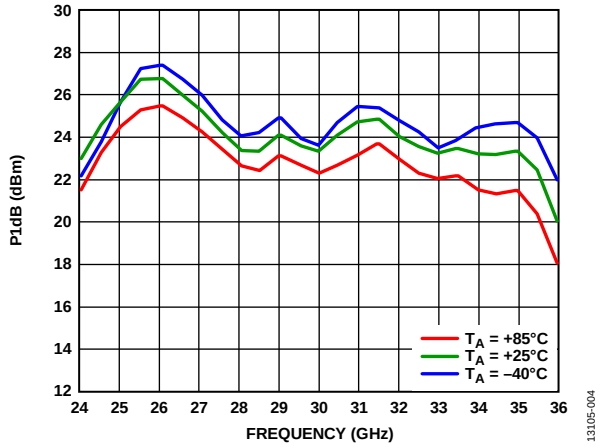

Figure 10. P1dB vs. Frequency at Various Temperatures

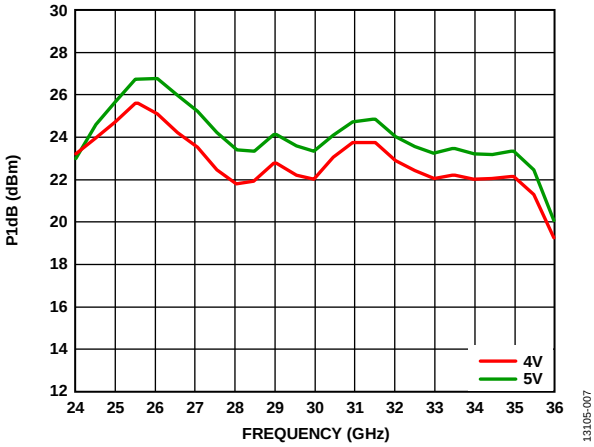

Figure 13. P1dB vs. Frequency at Various Supply Voltages

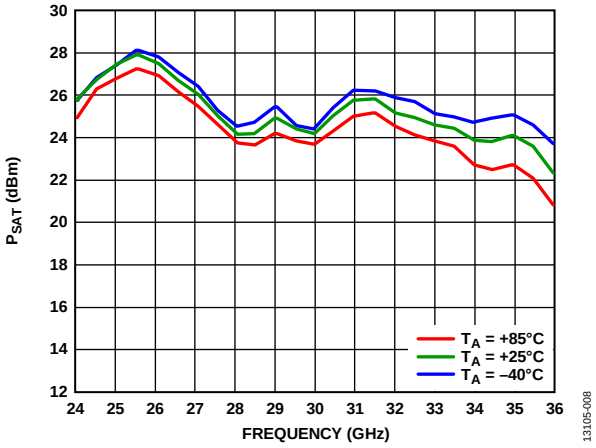

Figure 14. P_{SAT} vs. Frequency at Various Temperatures

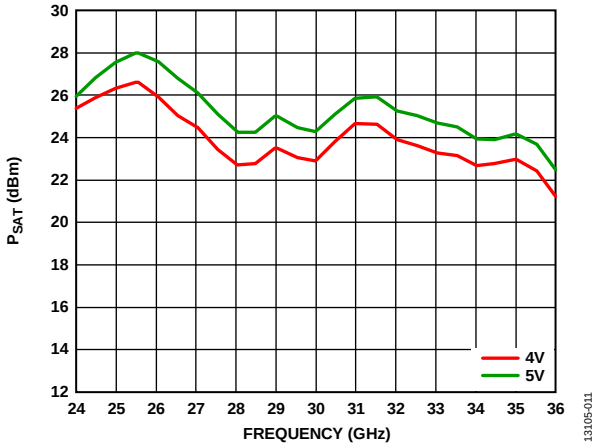

Figure 17. P_{SAT} vs. Frequency at Various Supply Voltages

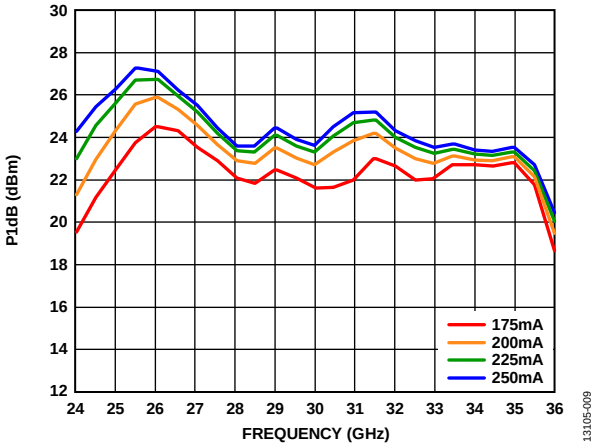

Figure 15. P1dB vs. Frequency at Various Supply Currents

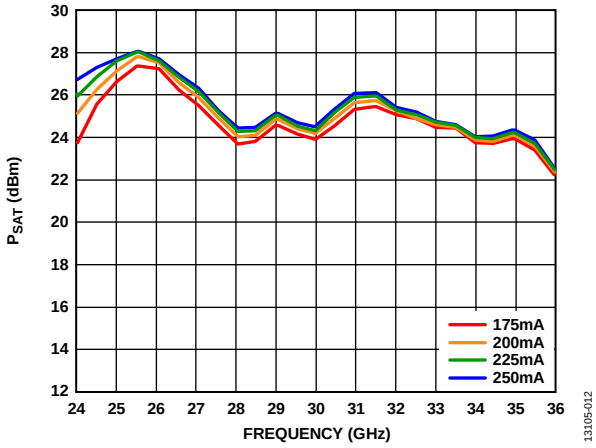

Figure 18. P_{SAT} vs. Frequency at Various Supply Currents

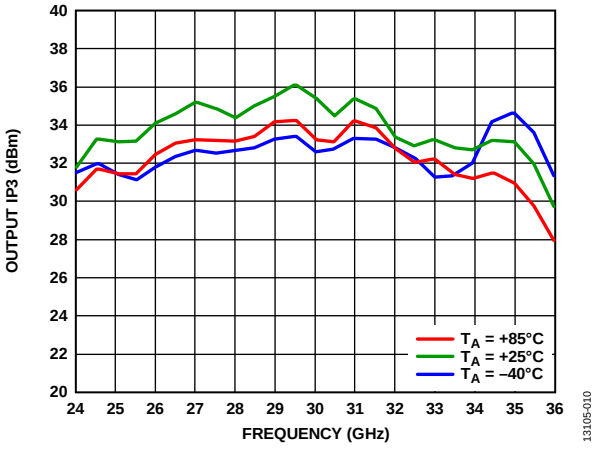

Figure 16. Output IP3 vs. Frequency at Various Temperatures, P_{OUT}/Tone = 10 dBm

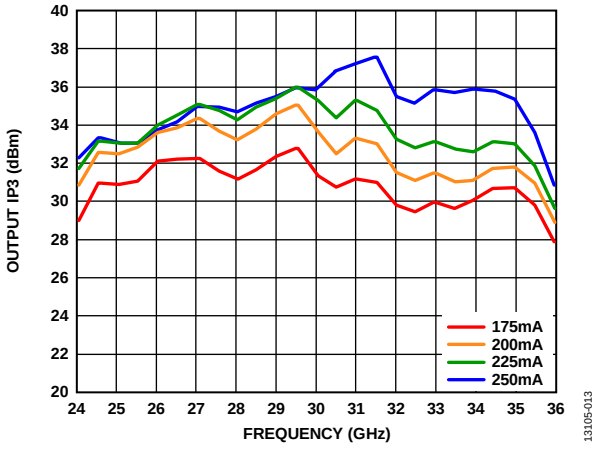

Figure 19. Output IP3 vs. Frequency at Various Supply Currents, P_{OUT}/Tone = 10 dBm

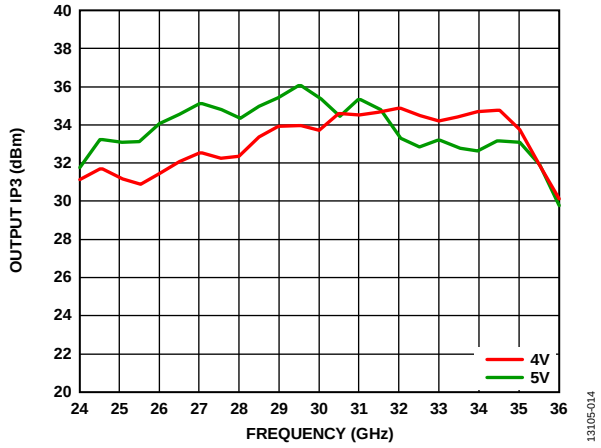

Figure 20. Output IP3 vs. Frequency for Various Supply Voltages, P_{OUT}/Tone = 10 dBm

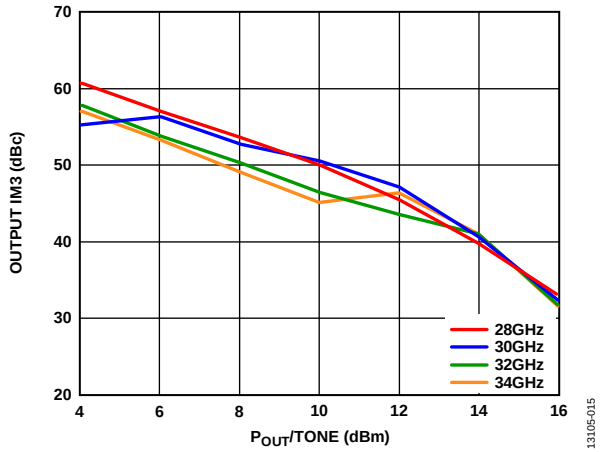

Figure 21. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 5 V

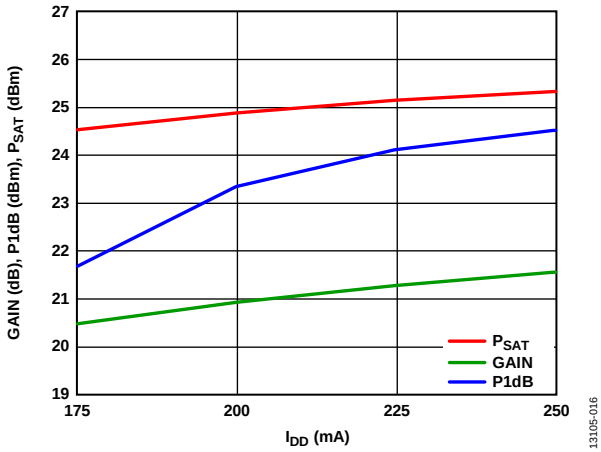

Figure 22. Gain, P1dB, and P_{SAT} vs. Supply Current (I_{DD}) at 30.5 GHz

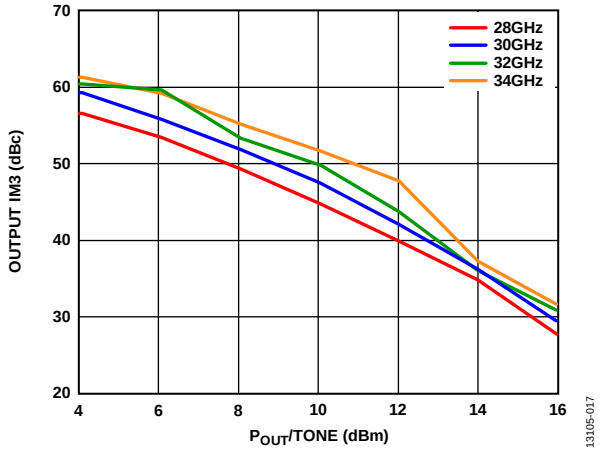

Figure 23. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 4 V

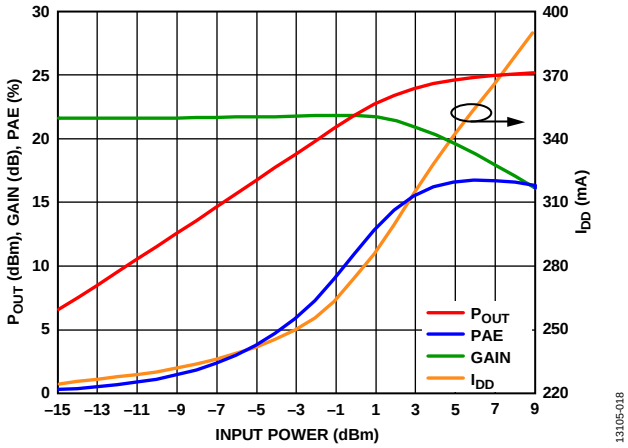

Figure 24. Power Compression at 30.5 GHz (PAE Is Power Added Efficiency)

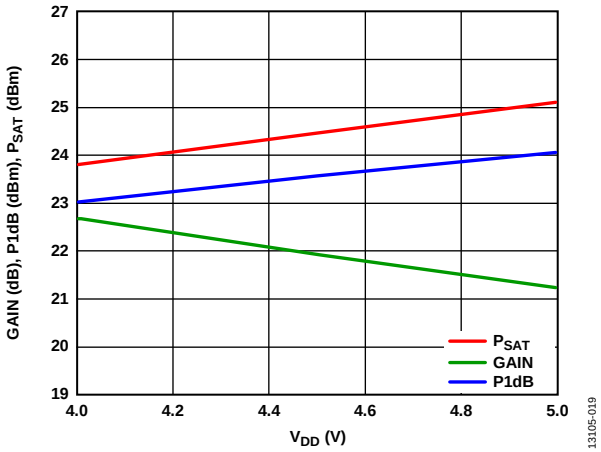

Figure 25. Gain, P1dB, and P_{SAT} vs. Supply Voltage (V_{DD}) at 30.5 GHz

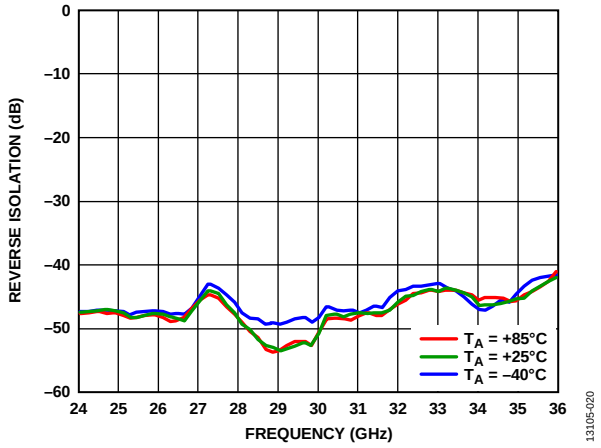

Figure 26. Reverse Isolation vs. Frequency at Various Temperatures

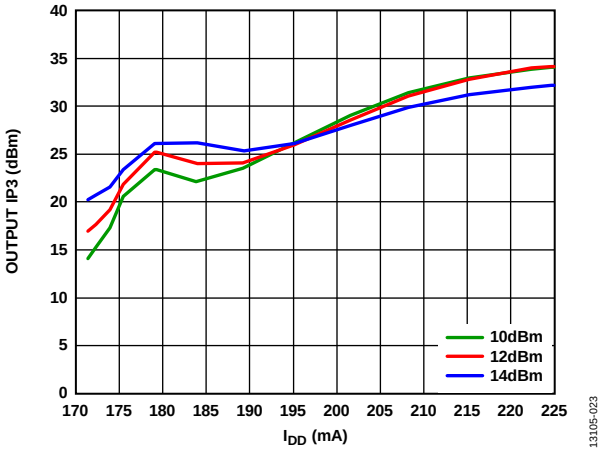

Figure 29. Output IP3 vs. I_{DD} over P_{OUT}/Tone at 30 GHz, V_{DD} = 5 V, I_{DD} = 225 mA, I_{DD2} = Fixed, and I_{DD1} Varied from 0 mA to 50 mA

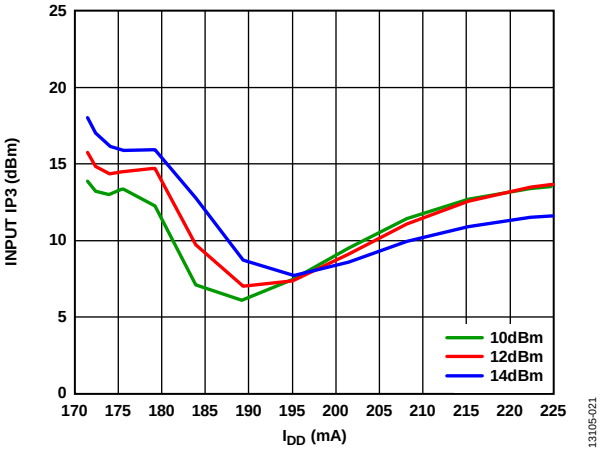

Figure 27. Input IP3 vs. I_{DD} over P_{OUT}/Tone at 30 GHz, V_{DD} = 5 V, I_{DD} = 225 mA, I_{DD2} = Fixed, and I_{DD1} Varied from 0 mA to 50 mA

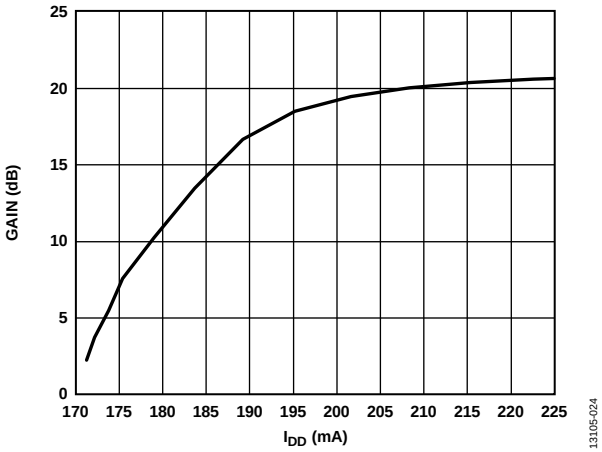

Figure 30. Gain vs. I_{DD} over P_{OUT}/Tone = 14 dBm at 30 GHz, V_{DD} = 5 V, I_{DD} = 225 mA, I_{DD2} = Fixed, and I_{DD1} Varied from 0 mA to50 mA

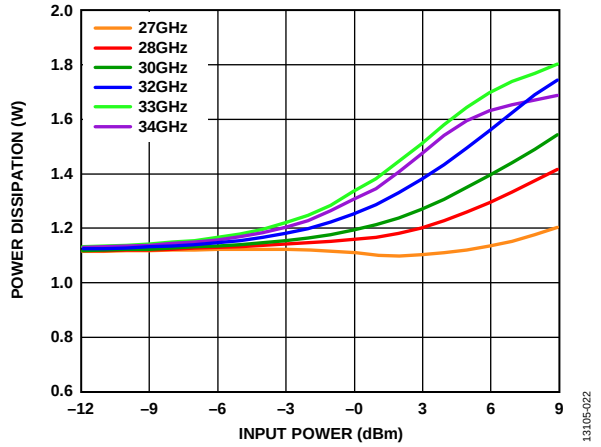

Figure 28. Power Dissipation (P_{DISS}) at 85°C vs. Input Power for Various Frequencies

APPLICATIONS INFORMATION

The HMC1131 is a GaAs, pHEMT, MMIC, medium power amplifier consisting of four gain stages in series. $V_{GG}1$ is the gate bias pin for the first and second stages, while $V_{GG}2$ is the gate bias pin for the third and fourth stages. A simplified block diagram is shown in Figure 31.

All measurements for this device were taken using the evaluation printed circuit board (PCB) in its default configuration. Unless otherwise noted, the $V_{GG}1$, $V_{GG}2$, and $V_{DD}1$ to $V_{DD}4$ pins were tied together during measurement, respectively.

The following is the recommended bias sequence during power-up:

1. Connect to ground.
2. Set $V_{GG}1$ and $V_{GG}2$ to −2 V.
3. Set $V_{DD}1$ through $V_{DD}4$ to 5 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to achieve a quiescent I_{DD} = 225 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:

1. Turn the RF signal off.
2. Decrease $V_{GG}1$ and $V_{GG}2$ to −2 V to achieve a quiescent I_{DD} = 0 mA (approximately).
3. Decrease $V_{DD}1$ through $V_{DD}4$ to 0 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to 0 V.

The $V_{DD}x$ = 5 V and I_{DD} = 225 mA bias conditions are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the HMC1131 at different bias conditions may result in performance that differs from that shown in Figure 27 and Figure 30. Biasing the HMC1131 for higher drain current typically results in higher P1dB, OIP3, and gain but at the expense of increased power consumption.

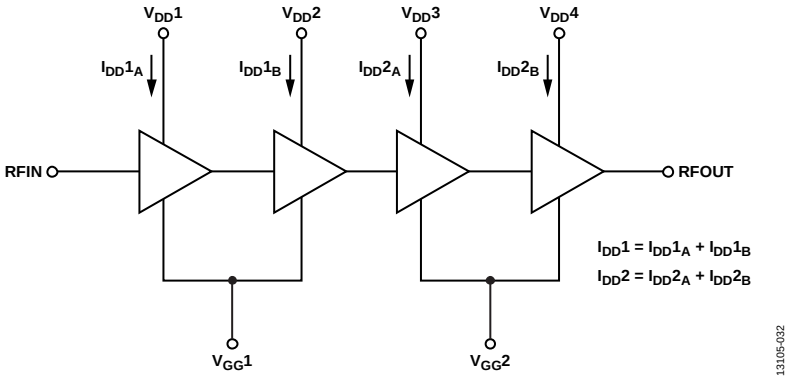

Figure 31. Simplified Block Diagram

EVALUATION PCB

Generate the evaluation PCB used in this application with proper RF circuit design techniques. Signal lines at the RF port must have 50 Ω impedance, and the package ground leads and exposed paddle must be connected directly to the ground plane similar to what is shown in Figure 32. Use a sufficient number of via holes to connect the top and bottom ground planes.

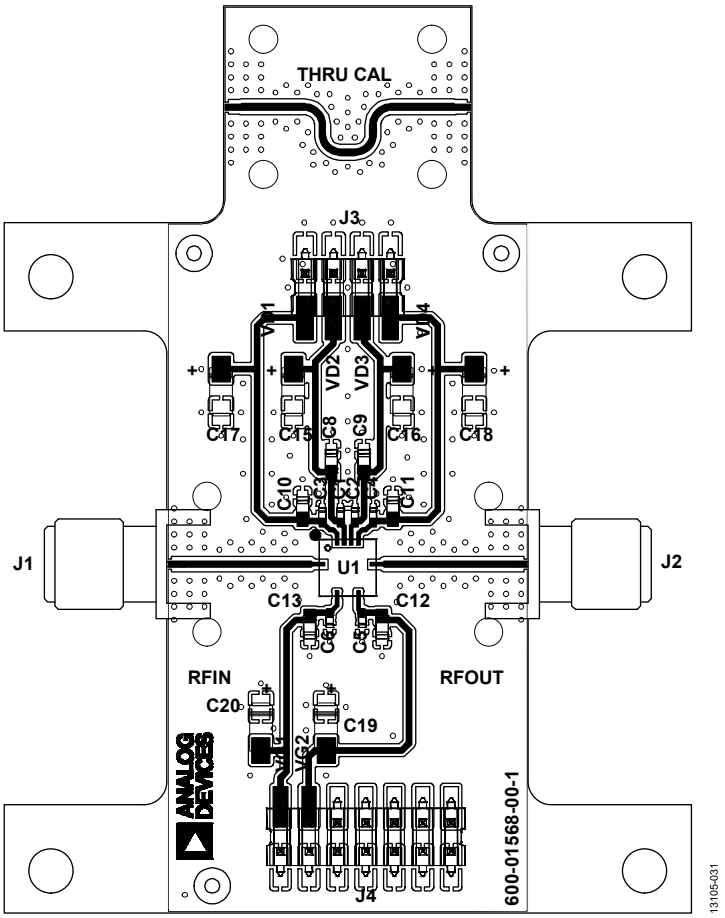

Figure 32. 600-01568-00-1 Evaluation PCB

Bill of Materials

Table 5. Evaluation Board (EV1HMC1131LC4) Bill of Materials

Item	Description	Manufacturer[1]
J1, J2	PCB mount, K connector	
J3, J4	DC pins	
C1 to C6	100 pF capacitors, 0402 package	
C8 to C13	0.01 µF capacitors, 0603 package	
C15 to C20	4.7 µF capacitors, Case A tantalum	
U1	HMC1131LC4	Analog Devices, Inc.
PCB	600-01568-00-1 evaluation board, Rogers 4350, or Arlon 25FR circuit board material	600-01568-00-1, Analog Devices, Inc.

[1] Blank cells in the manufacturer column left blank intentionally for they are user selectable.

TYPICAL APPLICATION CIRCUIT

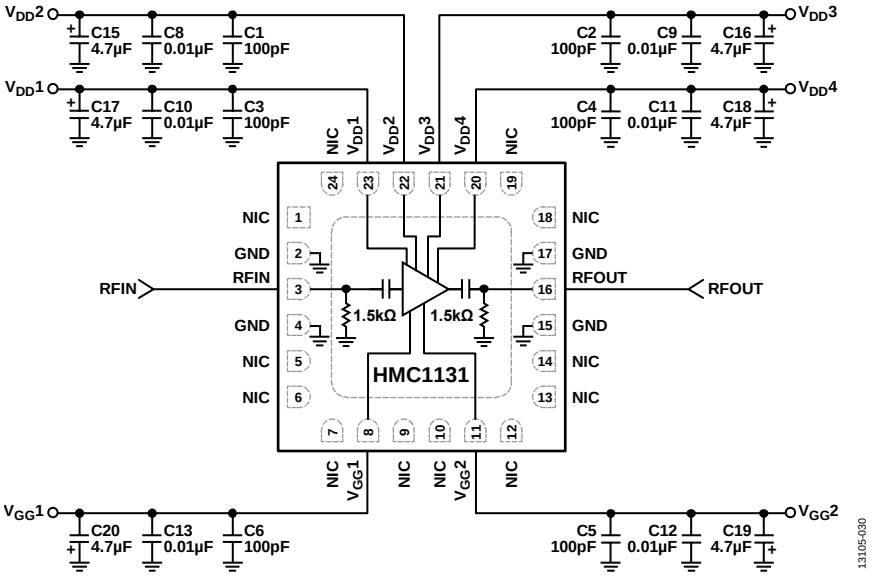

Figure 33. Typical Application Circuit

OUTLINE DIMENSIONS

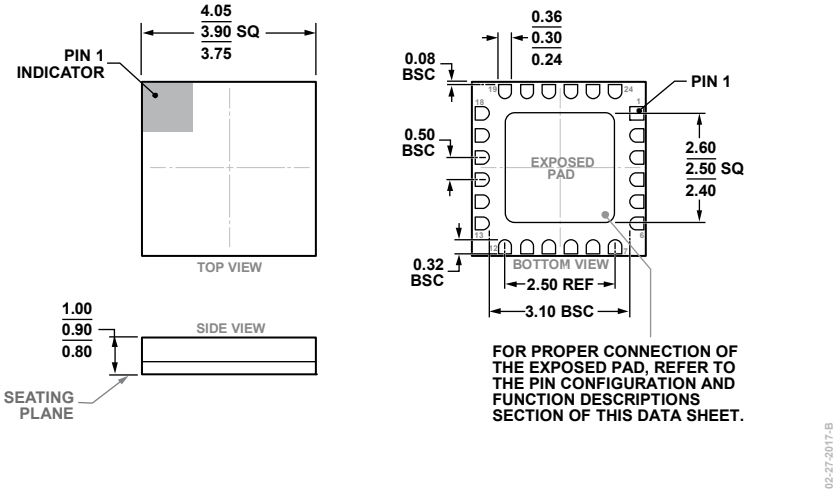

Figure 34. 24-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Moisture Sensitivity Level (MSL) Rating[2]	Lead Finish	Package Description	Package Option
HMC1131LC4	−40°C to +85°C	MSL3	Gold over Nickel	24-Terminal LCC	E-24-1
HMC1131LC4TR	−40°C to +85°C	MSL3	Gold over Nickel	24-Terminal LCC	E-24-1
EV1HMC1131LC4				Evaluation Board	

[1] All models are RoHS Compliant.
[2] See the Absolute Maximum Ratings section.

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D13105-0-5/19(C)

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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А