

# FPF2286UCX

## Product Preview

### 28 V / 4 A Rated OVP with Low On-resistance

FPF2286 is an OVP with integrated low on-resistance single channel switch. The device contains an N-MOSFET that can operate over an input voltage range of 2.8 V to 23 V and can support a maximum continuous current of 4 A.

When the input voltage exceeds the over-voltage threshold, the internal FET is turned off immediately to prevent damage to the protected downstream components.

FPF2286 is available in a small 6-bump WLCSP package and operate over the free-air temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

#### Features

- Over-voltage Protection Up to +28 V
- Internal Low  $R_{DS(on)}$  NMOS Transistors: Typical 25 m $\Omega$
- Programmable Over-voltage Lockout (OVLO)
  - ◆ Externally Adjustable via OVLO Pin
- Active-low Enable Pin (OVLO) for Device
- Super Fast OVLO Response Time: Typical 40 ns
- Short Circuit Protection and Auto-restart
- Over Temperature Protection (Thermal Shutdown)
- Robust ESD Performance
  - ◆ 2 kV Human Body Model (HBM)
  - ◆ 1 kV Charged Device Model (CDM)
  - ◆  $V_{IN}$  Tolerant to 35 V Residue-voltage during Surge Event
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- Mobile Phones
- PDAs
- GPS

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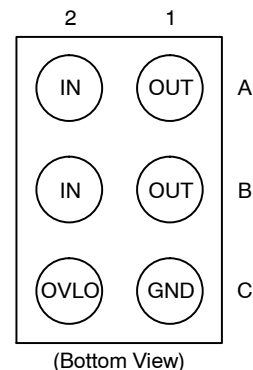
WLCSP6  
CASE 567UV

#### MARKING DIAGRAM



XX = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

#### PIN CONNECTIONS



#### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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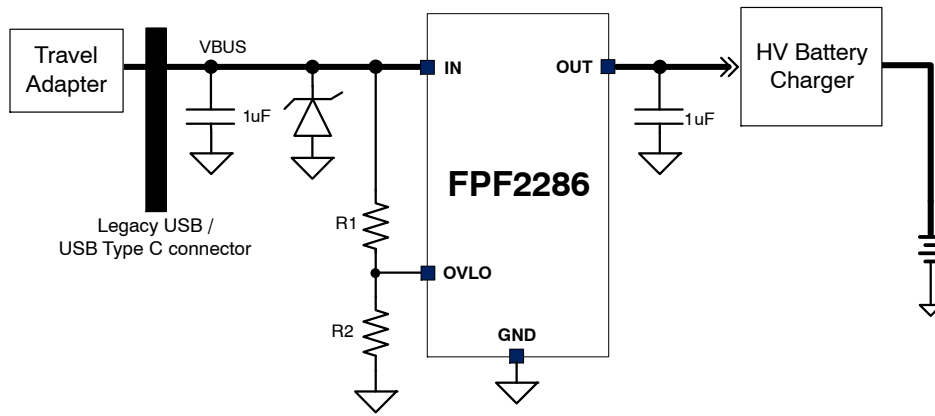


Figure 1. Application Schematic – Adjustable Option

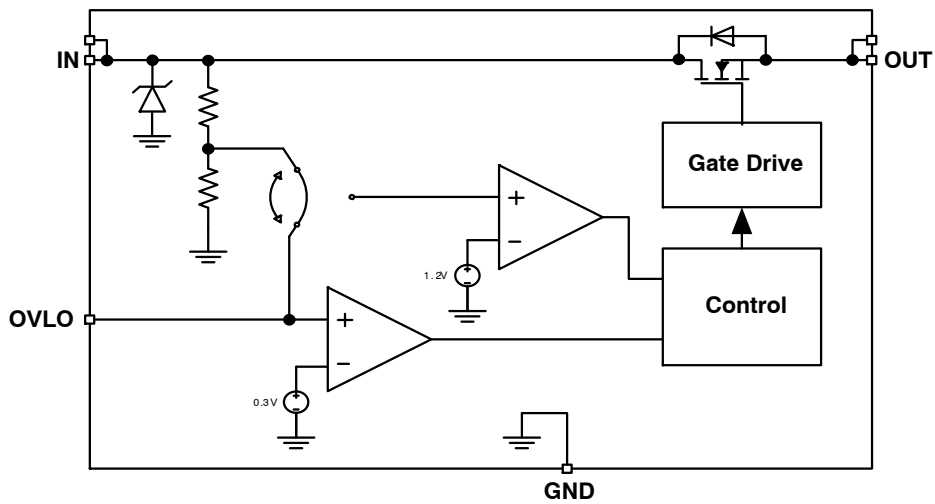


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description                                       |
|---------|----------|---|
| A2, B2  | IN       | Power Input: Switch Input and Device Supply       |
| A1, B1  | OUT      | Power Output: Switch Output to Load               |
| C2      | OVLO     | OVLO Input: Over Voltage Lockout Adjustment Input |
| C1      | GND      | Ground  |

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**Table 2. MAXIMUM RATINGS**

| Rating  | Symbol             | Value                      | Unit |
|---|--------------------|----------------------------|------|
| Input Voltage Range (Note 1)  | $V_{in}$           | -0.3 to 28                 | V    |
| Output Voltage Range  | $V_{out}$          | -0.3 to ( $V_{in} + 0.3$ ) | V    |
| Adjustable Input Range  | $V_{OVLO}$         | -0.3 to 23                 | V    |
| Internal FET continuous current   | $I_{OUT}$          | 0 to 4                     | A    |
| Maximum Junction Temperature  | $T_{J(max)}$       | 150                        | °C   |
| Storage Temperature Range   | $T_{STG}$          | -65 to 150                 | °C   |
| ESD Capability, Human Body Model (Note 2)   | ESD <sub>HBM</sub> | 2                          | kV   |
| ESD Capability, Charged Device Model (Note 2)                                     | ESD <sub>CDM</sub> | 1                          | kV   |
| Lead Temperature Soldering<br>Reflow (SMD Styles Only), Pb-Free Versions (Note 3) | $T_{SLD}$          | 260                        | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
ESD Charged Device Model tested per AEC-Q100-011 (EIA/JESD22-C101)  
Latch-up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**Table 3. THERMAL CHARACTERISTICS**

| Rating  | Symbol          | Value | Unit |
|---|-----------------|-------|------|
| Thermal Characteristics, WLCSP-6 (Note 4)<br>Thermal Resistance, Junction-to-Air (Note 5) | $R_{\theta JA}$ | 121.7 | °C/W |

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. Values based on 2S2P JEDEC std. PCB.

**Table 4. RECOMMENDED OPERATING RANGES**

| Rating                | Symbol     | Min | Max | Unit |
|-----------------------|------------|-----|-----|------|
| Supply Voltage on VIN | $V_{in}$   | 2.8 | 23  | V    |
| I/O pins              | $V_{OVLO}$ | 0   | 5.5 | V    |
| Output Current        | $I_{out}$  | 0   | 3.5 | A    |
| IN Capacitor          | $C_{in}$   | 0.1 |     | μF   |
| OUT Capacitor         | $C_{out}$  | 0.1 |     | μF   |
| Ambient Temperature   | $T_A$      | -40 | 85  | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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**Table 5. ELECTRICAL CHARACTERISTICS**

$V_{IN} = 2.8$  to  $23$  V,  $C_{IN} = 0.1$   $\mu$ F,  $C_{OUT} = 0.1$   $\mu$ F,  $T_A = -40$  to  $85^\circ$ C; For typical values  $V_{IN} = 5.0$  V,  $I_{IN} \leq 3$  A,  $C_{IN} = 0.1$   $\mu$ F,  $T_A = 25^\circ$ C, for min/max values  $T_A = -40^\circ$ C to  $85^\circ$ C; unless otherwise noted. (Note 6)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

## LEAKAGE AND QUIESCENT CURRENTS

|                                    |  |             |      |     |     |         |
|------------------------------------|--|-------------|------|-----|-----|---------|
| Input Quiescent Current on VIN     | $V_{IN} = 5$ V, $V_{OVLO} = 0.6$ V                   | $I_Q$       |      | 85  |     | $\mu$ A |
|                                    | $V_{IN} = 20$ V, $V_{OVLO} = 0.6$ V                  |             |      | 200 |     |         |
| Supply Current during Over Voltage | $V_{IN} = 23$ V, $V_{OVLO} = 3.0$ V, $V_{OUT} = 0$ V | $I_{IN\_Q}$ |      | 215 |     | $\mu$ A |
| OVLO Input Leakage Current         | $V_{OVLO} = V_{OVLO\_TH}$                            | $I_{OVLO}$  | -100 |     | 100 | nA      |

## OVER VOLTAGE AND UNDER VOLTAGE LOCKOUT

|  |  |                 |      |      |      |   |
|--|--|-----------------|------|------|------|---|
| Under-Voltage Rising Trip Level for VIN  | $V_{IN}$ rising, $T_A = -40$ to $85^\circ$ C   | $V_{IN\_UV\_R}$ | 2.3  | 2.5  | 2.7  | V |
| Under-Voltage Falling Trip Level for VIN | $V_{IN}$ falling, $T_A = -40$ to $85^\circ$ C  | $V_{IN\_UV\_F}$ |      | 2.4  |      | V |
| Default Over-Voltage Trip Level          | $V_{IN}$ rising, $T_A = -40$ to $85^\circ$ C   | $V_{IN\_OVLO}$  | 6.6  | 6.8  | 7.0  | V |
| OVLO set threshold                       | $V_{OVLO} = 1.1$ V to $1.3$ V, the voltage of OVLO to trigger Over Voltage condition | $V_{OVLO\_TH}$  | 1.16 | 1.19 | 1.22 | V |
| OVLO threshold hysteresis                |  | $V_{HYS\_OVLO}$ |      | 2    |      | % |
| Adjustable OVLO range                    | $OV\_MODE = 0$ , $V_{OVLO} > 0.5$ V  | $V_{OV\_RNG}$   | 4    |      | 23   | V |

## I/O THRESHOLDS

|                                |      |                |     |   |      |   |
|--------------------------------|------|----------------|-----|---|------|---|
| OVLO Input Threshold Voltage   |      |                |     |   |      | V |
| Voltage Increasing, Logic High | High | $V_{IH\_OVLO}$ | 0.3 | - | -    |   |
| Voltage Decreasing, Logic Low  | Low  | $V_{IL\_OVLO}$ | -   | - | 0.15 |   |

## RESISTANCE

|                            |  |          |  |    |    |            |
|----------------------------|--|----------|--|----|----|------------|
| On-resistance of Power FET | $V_{IN} = 5$ V, $I_{OUT} = 500$ mA, $T_A = 25^\circ$ C | $r_{ON}$ |  | 25 | 35 | m $\Omega$ |
|----------------------------|--|----------|--|----|----|------------|

## TIMING

|                                       |  |               |  |           |  |    |
|---------------------------------------|--|---------------|--|-----------|--|----|
| De-bounce Time of Power FET turned on | Time from $2.5$ V $< V_{IN} < V_{IN\_OVLO}$ to $V_{OUT} = 0.1 \times V_{IN}$   | $t_{SW\_DEB}$ |  | 15        |  | ms |
| Switch Turn-On rising Time (Note 8)   | $V_{IN} = 5$ V, $R_L = 100$ $\Omega$ , $C_L = 22$ $\mu$ F, $V_{OUT}$ from $0.1 \times V_{IN}$ to $0.9 \times V_{IN}$   | $t_R$         |  | 1         |  | ms |
| Switch Turn-Off Time (Note 8)         | $R_L = 10$ $\Omega$ , $C_L = 0$ $\mu$ F, time from $V_{IN} > V_{OVLO}$ to $V_{OUT} = 0.9 \times V_{IN}$<br>Internal OVP level<br>External OVP level (Note 9) |               |  | 40<br>100 |  | ns |

## THERMAL SHUTDOWN

|                                       |  |          |   |     |   |            |
|---------------------------------------|--|----------|---|-----|---|------------|
| Thermal Shutdown Temperature (Note 8) |  | $T_{SD}$ | - | 130 | - | $^\circ$ C |
| Thermal Shutdown Hysteresis (Note 8)  |  | $T_{SH}$ | - | 20  | - | $^\circ$ C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ$ C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
- Refer to the APPLICATION INFORMATION section.
- Values based on design and/or characterization.
- Depends on the capacitance on OVLO pin.

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## Function Description

### General

FPF2286 is an OVP power switch to protect next stage system which is optimized to lower voltage working condition. The device includes ultra low on-resistance power FET (25 mΩ) and super fast OVP response time (40 ns).

### Power MOSFET

The FPF2286 integrates an N-type MOSFET with 25 mΩ resistance. The power FET can work under 2.8 V ~ 23 V and up to 4 A DC current capability.

### Power Supply

The FPF2286 is supplied by IN. IN will be firstly supplied by OUT when the device is working under USB On-The-Go (OTG) condition.

### Enable Control

There is no specified enable pin for FPF2286. However, the OVLO can be used as an active LOW enable pin to be controlled by a GPIO. When OVLO pin is connected to a high level (higher than 1.2 V), the internal FET will be turned off. When OVLO pin is connected to 0 V, the FET will be turned on as long as V<sub>IN</sub> is not higher than 6.8 V.

### Under Voltage Lockout

FPF2286 power switch will be turned off when the voltage on IN is lower than the UVLO threshold V<sub>IN\_UV\_F</sub>. Whenever V<sub>IN</sub> voltage ramps up to higher than V<sub>IN\_UV\_R</sub>, the power FET will be turned on automatically after t<sub>DEB</sub> de-bounce time if there is no OV or OT condition.

### Over Voltage Lockout

The power FET will be turned off whenever V<sub>IN</sub> voltage higher than V<sub>IN\_OVLO</sub>. The value of V<sub>IN\_OVLO</sub> can be set by external resistor ladder or just be default value V<sub>IN\_OVLO</sub>.

When V<sub>OVLO</sub> is smaller than V<sub>IL\_OVLO</sub>, V<sub>OVLO</sub> will be decided by default value. When V<sub>OVLO</sub> is larger than V<sub>IH\_OVLO</sub>, the power switch will be turned off once V<sub>OVLO</sub> > V<sub>OVLO\_TH</sub>. The external resistor ladder can be decided according to the following equation:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times (1 + R1/R2) \quad (\text{eq. 1})$$

where R1 and R2 are the resistors in Figure 1.

### Thermal Shutdown

When the device is in the switch mode, to protect the device from over temperature, the power switch will be turned off when the junction temperature exceeds T<sub>SD</sub>. The switch will be turned on again when temperature drop below T<sub>SD</sub> - T<sub>SH</sub>.

## APPLICATIONS INFORMATION

### Input Decoupling (C<sub>in</sub>)

A ceramic or tantalum at least 0.1 μF capacitor is recommended and should be connected close to the FPF2286 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

### Output Decoupling (C<sub>out</sub>)

The FPF2286 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements.

### Thermal Considerations

As power in the FPF2286 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When

the FPF2286 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the FPF2286 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (\text{eq. 2})$$

Since T<sub>J</sub> is not recommended to exceed 125°C, then the FPF2286 soldered on 645 mm<sup>2</sup>, 1 oz copper area, and the ambient temperature (T<sub>A</sub>) is 25°C. The power dissipated by the FPF2286 can be calculated from the following equations:

$$P_D \approx V_{in} \cdot (I_Q @ I_{out}) + I_{out}^2 \cdot r_{ON} \quad (\text{eq. 3})$$

### Hints

V<sub>in</sub> and V<sub>out</sub> printed circuit board traces should be as wide as possible. Place external components, especially the input capacitor and TVS, as close as possible to the FPF2286, and make traces as short as possible.

## ORDERING INFORMATION

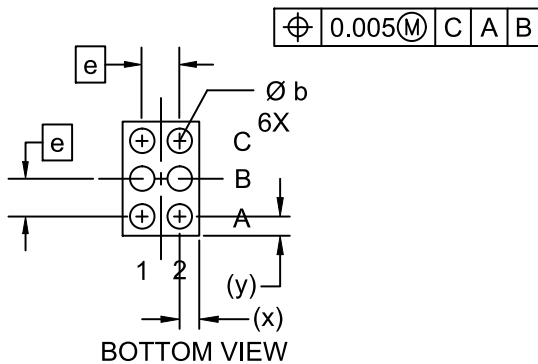
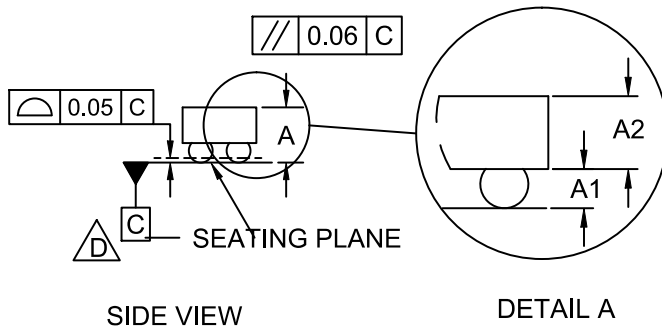
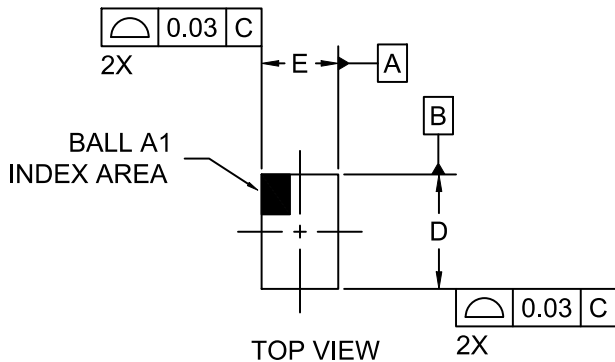
| Device     | Default OV Level | Marking | Package  | Shipping†          |
|------------|------------------|---------|----------|--------------------|
| FPF2286UCX | 6.8 V            | 3F      | WLCSP-6L | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

# FPF2286UCX

## PACKAGE DIMENSIONS

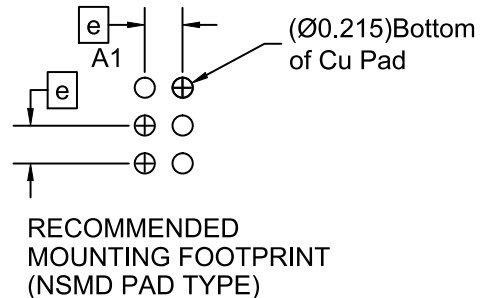
WLCSP6 1.3x0.9x0.574  
CASE 567UV  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 0.536       | 0.574 | 0.612 |
| A1  | 0.176       | 0.196 | 0.216 |
| A2  | 0.360       | 0.378 | 0.396 |
| b   | 0.240       | 0.260 | 0.280 |
| D   | 1.270       | 1.300 | 1.330 |
| E   | 0.870       | 0.900 | 0.930 |
| e   | 0.40 BSC    |       |       |
| x   | 0.235       | 0.250 | 0.265 |
| y   | 0.235       | 0.250 | 0.265 |



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