QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1243 HOT SWAP CONTROLLER WITH CURRENT AND VOLTAGE MONITOR

LTC4215-1

DESCRIPTION

Demonstration Circuit 1243A showcases the LTC®4215--1IUF positive low voltage Hot Swap controller with I2C compatible monitoring in a 60W, 10.2 to 13.6V application. Included on board is an input clamp, input and output voltage dividers for UV, OV, and PWRGD, LEDs to indicate the presence of various voltages and signals and turret terminals for critical signals to facilitate evaluation in a working system. Input and output connections are made by 93 mil turrets which if removed, accommodate insertion of up to 12 gauge wires for in-situ testing. An I2C port designed to interface with DC590A allows control of DC874 with LTC's QuickEval software.

The DC1243A permits evaluating the LTC4215-1 during turn-on and turn-off transients as well as during steady state conditions.

Design files for this circuit board are available. Call the LTC factory.

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Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Rated operating limits	2.9V ≤ VCC ≤ 15V
Under Voltage Lockout	Transition to operating mode	2.75V ≤ $V_{DD(UVL)}$ ≤ 2.89V
UV, OV, FB,EN\ Pin Threshold Voltage		1.215V ≤ V_{TH} ≤ 1.255V
Gate to Source Voltage	V_{DD} = 2.9V to 15V	4.7V ≤ V_{GS} ≤6.5V
Gate Pull-Up current	Charge Pump On, V_{GATE} 0.2V	15µA ≤ I_{GATE} ≤ 30µA
Normal Gate Pull-Down Current	ON Pin Signal Low	0.8mA ≤ I_{GATE} ≤ 1.6mA
Circuit Breaker Threshold	After Startup Timer Expired	22.5mV ≤ ΔV_{SENSE} ≤ 27.5mV
Current Limit Voltage	V_{FB}=1.3V	22mV ≤ ΔV_{SENSE} ≤ 29mV
	V_{FB}=0V	6.5mV ≤ ΔV_{SENSE} ≤ 13mV
	Start-Up Timer Expired	65mV ≤ ΔV_{SENSE} ≤ 90mV
ADC Resolution (No missing codes)		8
ADC Offset	VDD-Sense	+/- 2.0 LSB
	SOURCE	+/- 1 LSB
	ADIN	+/- 1 LSB
ADC Full-Scale Voltage (255 * V_{LSB})	VDD-Sense	37.625mV ≤ V_{FS} ≤ 39.275mV
	SOURCE	15.14 ≤ V_{FS} ≤ 15.74
	ADIN	1.205 ≤ V_{FS} ≤ 1.255
ADC Total Unadjusted Error	VDD-Sense	+/- 5.5 LSB
	SOURCE	+/- 5 LSB
	ADIN	+/- 5 LSB

OPERATING PRINCIPLES

The LTC4215-1 is a low voltage hot swap controller that has a 2.9V to 15V operating range and a 24V absolute maximum operating voltage for the VDD pin. This demo circuit is populated for +12V operation, but it can easily be readjusted for any voltage between 2.9V and 15V by replacing R1, R2 and R7 (top resistors in the UV/OV divider and the FB divider). The DC1243A as supplied by the factory is populated with a Si4864DP MOSFET in an SO-8 package and a 4mΩ, 1/2W, current sense resistor, providing a minimum of 5.4A load current. The current limit and circuit breaker thresholds can be adjusted by changing the sense resistor, RS. To enable demonstration of higher current applications up to 20A, provisions have been made to replace RS with a 1W, 2512 size sense resistor and replace Q1 with a MOSFET in a PowerPAK SO-8, such as the Si7880ADP. The large turrets may be removed to permit installation of up to 12 gauge wire for direct, low resistance connections to the board. None of the turrets are swaged.

QUICK START PROCEDURE

Demonstration circuit 1243A is easy to set up to evaluate the performance of the LTC4215-1. Refer to Figure 4 for proper measurement equipment setup and follow the procedure below:

1. The DC1243A is factory setup to operate in a 12 volt system at current levels up to 5 amps. If the LTC4215-1 is to be evaluated at a different operating condition, follow 2-6 below, otherwise skip to 6.
2. If evaluating at a voltage other than 12V, R1 and R2 must be adjusted for proper UV and OV PIN response. Select $R2=V_{MAX}/V_{MIN}•13.7K*1.235/1.205-13.7K$, and $R1=V_{MIN}*(13.7k+R2)/1.235-13.7-R2$, where V_{MIN} and V_{MAX} are the minimum and maximum output voltages expected for normal operation.
3. If evaluating at a voltage other than 12V, R7 must be adjusted for proper foldback and power-good detection. Select $R7=V_{MIN}*3.01k/1.235-3.01k$, where V_{MIN} is the minimum output voltage value for which power is determined to be good.
4. If the DC1243A will operate at other than 5Amps max, change the value of $R_{SENSE}=0.99•22mV/I_{LOAD(MAX)}$ for a 1% tolerance current sense resistor.
5. If the DC1243A will be operating above 10Amps, replace Q1 with a suitable PowerPAK SO-8 package MOSFET such as the Si7880ADP suitable for up to 20Amps. The SO-8 pads on the front of the board include the extra heat-sinking this package requires. Alternately, for low power applications, Q1 may be replaced with a MOSFET in a SSOT-6 package using alternate pads on the back of the board.
6. The 'TIMER SELECT' jumper can be used to choose between the external timer capacitor, CT, and the built in internal startup time of 100ms. CT is stuffed with a 0.68uF capacitor at the factory, which provides an 8ms startup time. To customize the startup time, select $CT=T_{START}/12.3(ms/uF)+10*CSS$.
7. The soft start capacitor, CSS, sets the ramp rate at which the inrush current will increase when turning on. CSS is stuffed with a 68nF capacitor at the factory, which provides a 5mV/ms inrush sense voltage ramp. CSS has a minimum value of 1nF. CT must be at least 10 times CSS to avoid a condition where the startup timer expires before the inrush ramp allows the MOSFET to turn on.
8. The LTC4215-1 does not require an RC network on the GATE pin for compensation. However, an RC network may be used to limit the rate at which the GATE rises to provide an inrush current below the internal current limit. Pads R6 and CG on the back of the board are available for this purpose. R6 and CG may be stuffed with a 15k resistor, and $CG=C_{LOAD} * 20uA/I_{INRUSH}$ for this purpose.
9. The ADIN pin may be used to take 8 bit measurements of any voltage. Jumper 'ADIN SELECT' selects between measuring the input voltage or measuring the voltage on the ADIN turret. The input voltage is measured through a resistor divider, which defaults to a 15.4V full scale range to match the range of the SOURCE pin measurement. To change the full scale of the input measurement, select $R11=V_{RANGE}*12.4k/1.23-12.4k$. The ADIN turret is also measured through a voltage divider, but the bottom resistor is not stuffed at the factory, defaulting to a 1.23V full scale voltage. To select a larger full scale voltage, choose $R17=1.23*10k/(V_{RANGE}-1.23)$.
10. If your system uses a short pin to sense board insertion, move the EN# jumper to SHORT PIN and, using the SHORT PIN turret, connect the aforementioned short pin. This is a direct connection to the LTC4215's EN# pin; if deleterious voltages are anticipated, add a series resistor and clamping. EN# is good for -0.3 to +12V on its own. EN# is also logic compatible, with a 1.235V threshold and 130mV hysteresis.
11. The I2C address is selected on the board by using **JP4 (ADR0)** and **JP5 (ADR1)** to pull the address

pins high, low, or allowing them to float. An address table is shown in the data sheet. The evaluation software automatically scans and identifies the I2C address, regardless of the setting.

12. After any necessary component changes have been made, connect a suitable load between VOUT and GND. This may be a passive resistive load or an active electronic load box. If long leads are present between the DC1243A and load bypassing, install 10µF or more bypassing at COUT to eliminate the chance of MOSFET oscillation and large negative excursions at +12V/5A OUTPUT.

13. Connect a power supply capable of supplying $1.5 \bullet I_{LOAD}$ between the +12V input and GND turrets. The minimum current capability of the supply must accommodate the tolerance of the circuit breaker threshold of ±12%. With the 4mΩ, 1%, factory installed sense resistor, the overload circuit breaker will trip at between 5.4A to 7.1Amp (6.25Amp nominal).

14. Connect the ribbon cable from a DC590 to the I2C PORT on the 874. LTC's QuickEval software will automatically recognize the 1243 and load software to read and write to the LTC4215-1's registers. During an I2C transaction, D5-7 will flicker faintly. If the I2C port (JP7) is disconnected, the turret terminals SDAO, SDAI, and SCL can be connected directly to an I2C bus. Power for D4-7 is supplied by JP7**, pin 2**, so in this mode the LEDs will not light unless 5V is connected to this pin. Resistor R24 shorts SDAO and SDAI together for communication to a non-isolated bus. Removing R24 splits SDAO and SDAI to facilitate optically isolated applications (see the LTC4215-1 data sheet).

15. The following experiments can be run. Turn on into a nominal load. Turn on into an overload. Turn on into a short circuit. Turn on into a nominal load and increase the load until the LTC4215 trips off. A digital storage scope provides a convenient means of observing the turn on and overload events. Observe the input or output current using a current probe. A probe ground turret is provided to provide a low current connection to the LTC4215-1's ground.

USING THE I2C PORT WITH QUICKEVAL

1) Register Display Options

The bits of registers A, B, C, or D, are shown in detail depending on the option selected (Figure 2A, 2B 2C, and 2D). Checking a box to the left of each bit of the Read/Write registers sets the respective bit, while unchecking a box clears the bit. The bit status is shown to the right of each bit after every refresh of the interface. The Clear button for register D clears out the bits in this register.

In the Register List option (Figure 2E) a display of a status bit map of the all the registers is shown and is updated with each refresh of the interface.

The Reg Send option (Figure 2F) allows for the user to enter and send data to a particular register. Select the register to be written to in the drop down menu. Enter the data in hex and click on Send Data to send the data or Send/Refresh so send and refresh the interface.

2) START/Refresh Buttons

Click on the START button to enable a timer that continuously updates the interface with the latest data from the LTC4215 approximately every 500ms. This button will display STOP when the timer is enabled. Click on STOP to stop the timer. Click on Refresh for a single update.

3) FET Control

The status of the FET is shown with a color display. When the FET On bit (C3) is read as high and the FET On Control bit (A3) is set, the FET is On, the shape dis-

play will be green and the FET control button will read .Turn FET Off.. If C3 is low and A3 is set, the FET is off, the shape display will be the color red and the FET control button will read .Clear Faults.. In all other cases, the FET is off, the shape display is rd and the FET control button will read .Turn FET On. The .Turn FET On. control button sets bits A3 logic high. .Turn FET Off. or .Clear Faults. clears bit A3 to logic low.

4) Address Selection

Select in the drop down list box the Write address byte of the LTC4215-1 that is to be communicated with. If multiple LTC4215-1s are on the bus lines, the Mass Write address BEh can be selected to communicate with all LTC4215-1s at the same time. The Auto find button will scan through the 9 individual LTC421-15 addresses and list which addresses responded with an acknowledge. The ARA button sends the Alert Response protocol and displays the address of the device that replies with its address.

5) Data Display Option

The Fixed option (Figure 3A) shows the data byte in hex for registers E, F, and G and displays the calculated Vdd sense, Source voltage, and ADIN values using the following equations:

Vdd sense = Sense(data) * SenseScale mV

Source voltage = Source(data) * SourceScale V

ADIN voltage = ADIN(data) * ADINScale V

The Adjusted option allows the user to enter Rs, R14 and R17. The calculated values are shown using the following equations:

Idd sense = Vdd sense / Rs mA

ADIN full = ADIN voltage * (R14 + R17) / R17 V

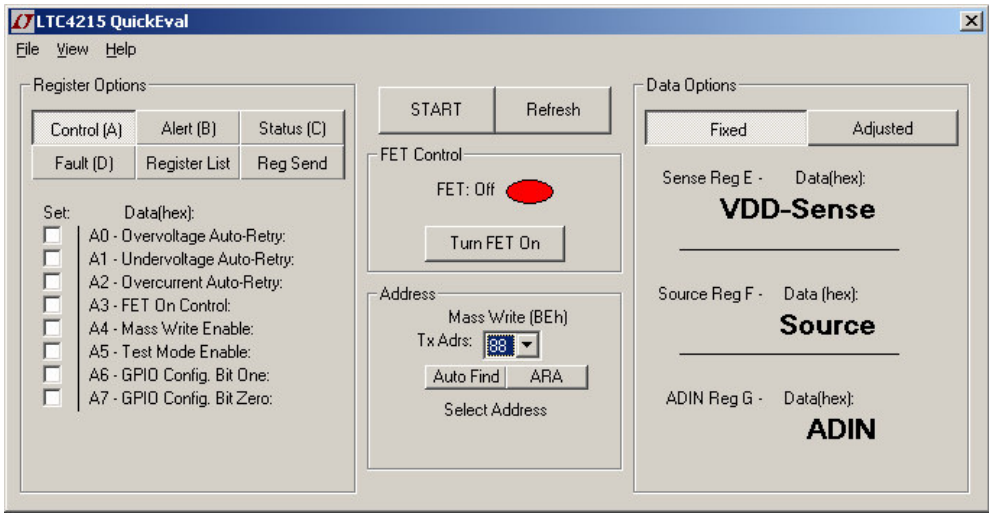


Figure 1. Default LTC4215-1 QuickEval Interface

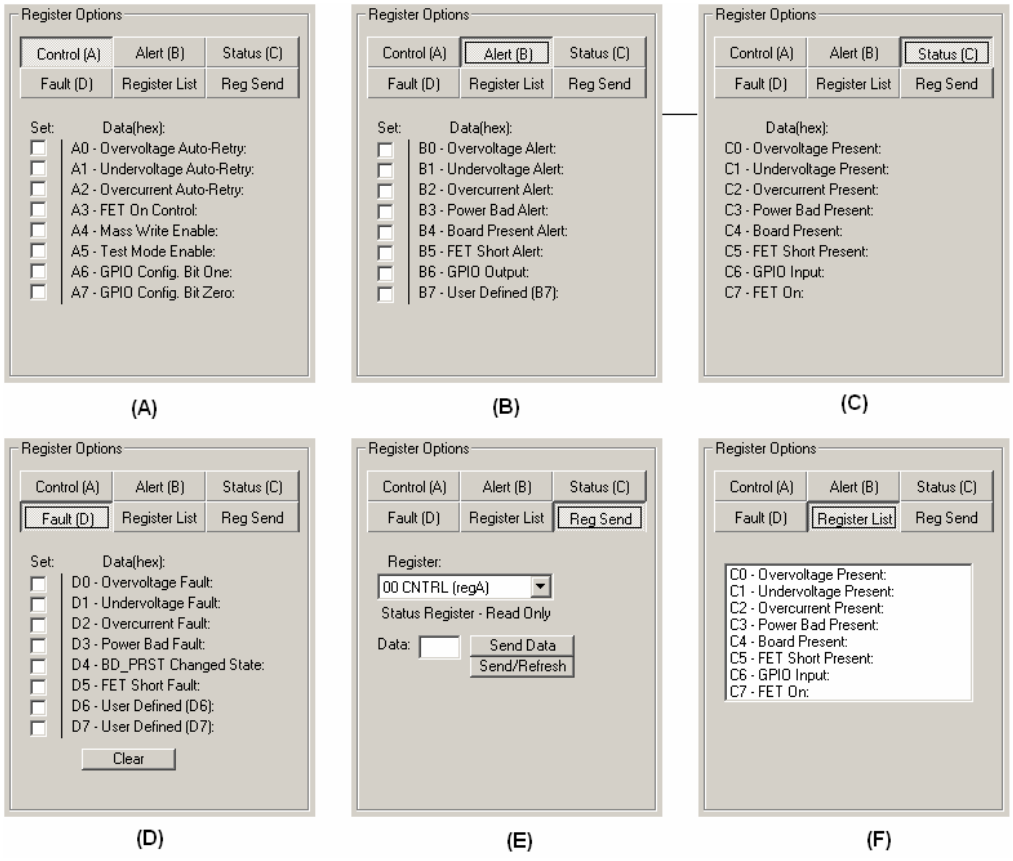


Figure 2. Register Display Options

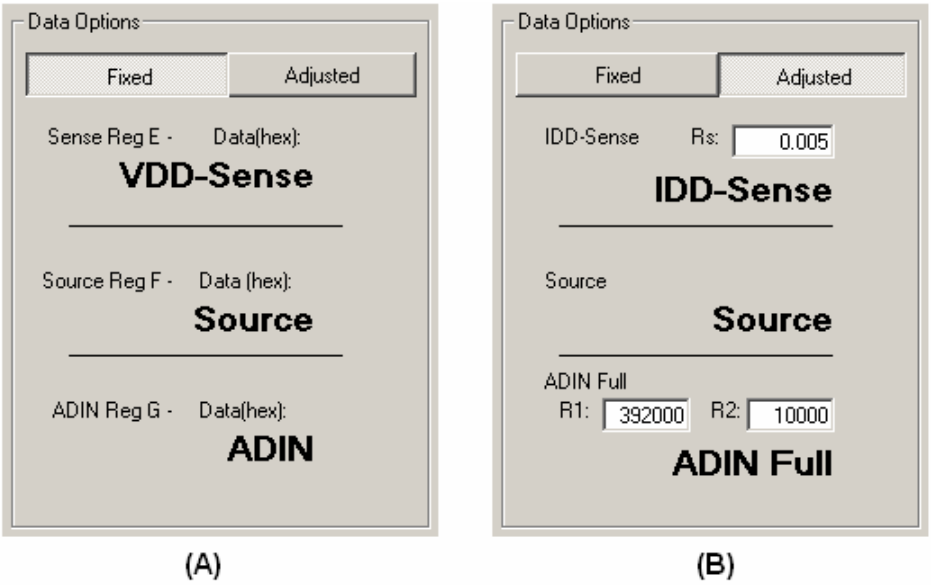


Figure 3. Data Display Options

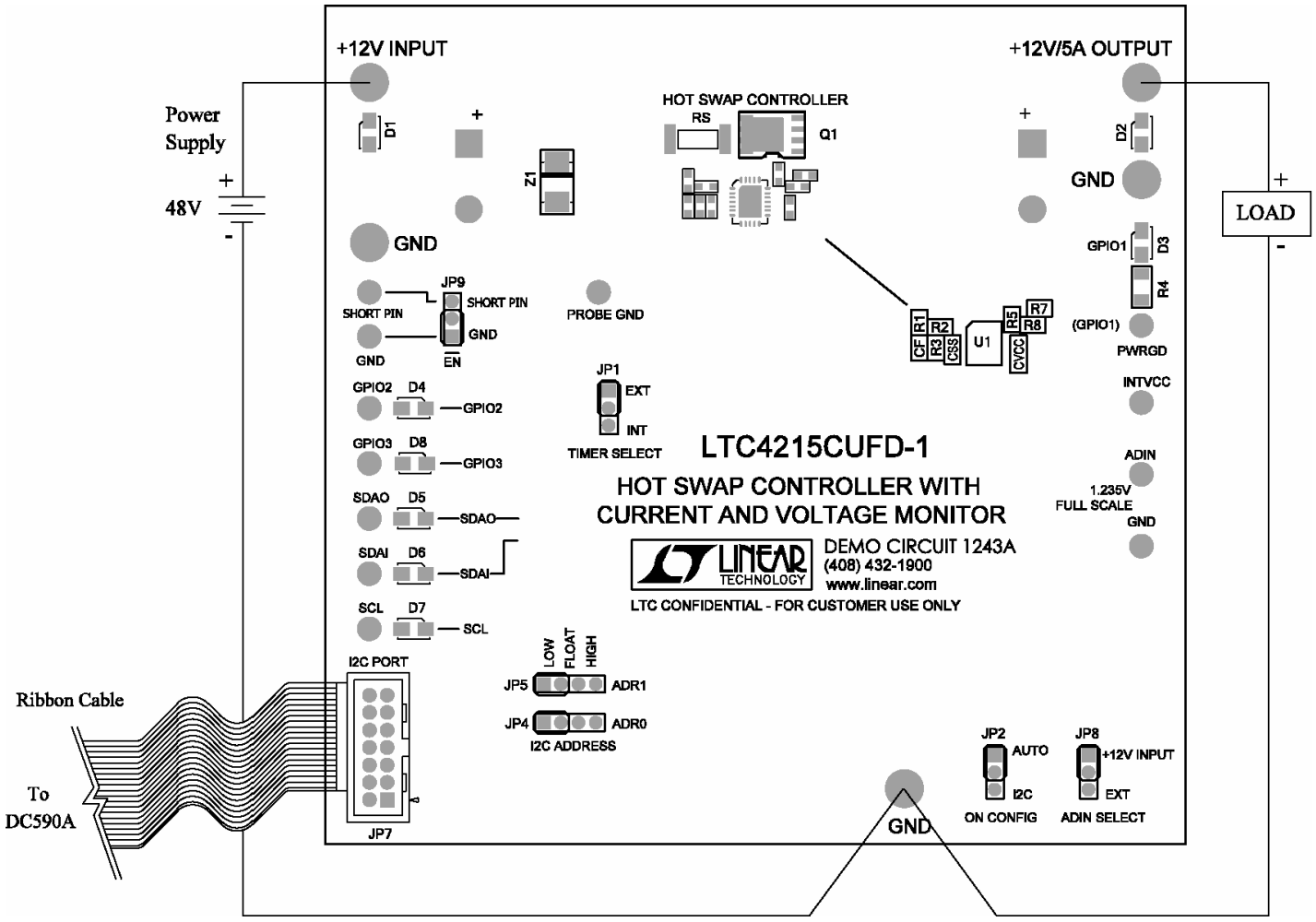
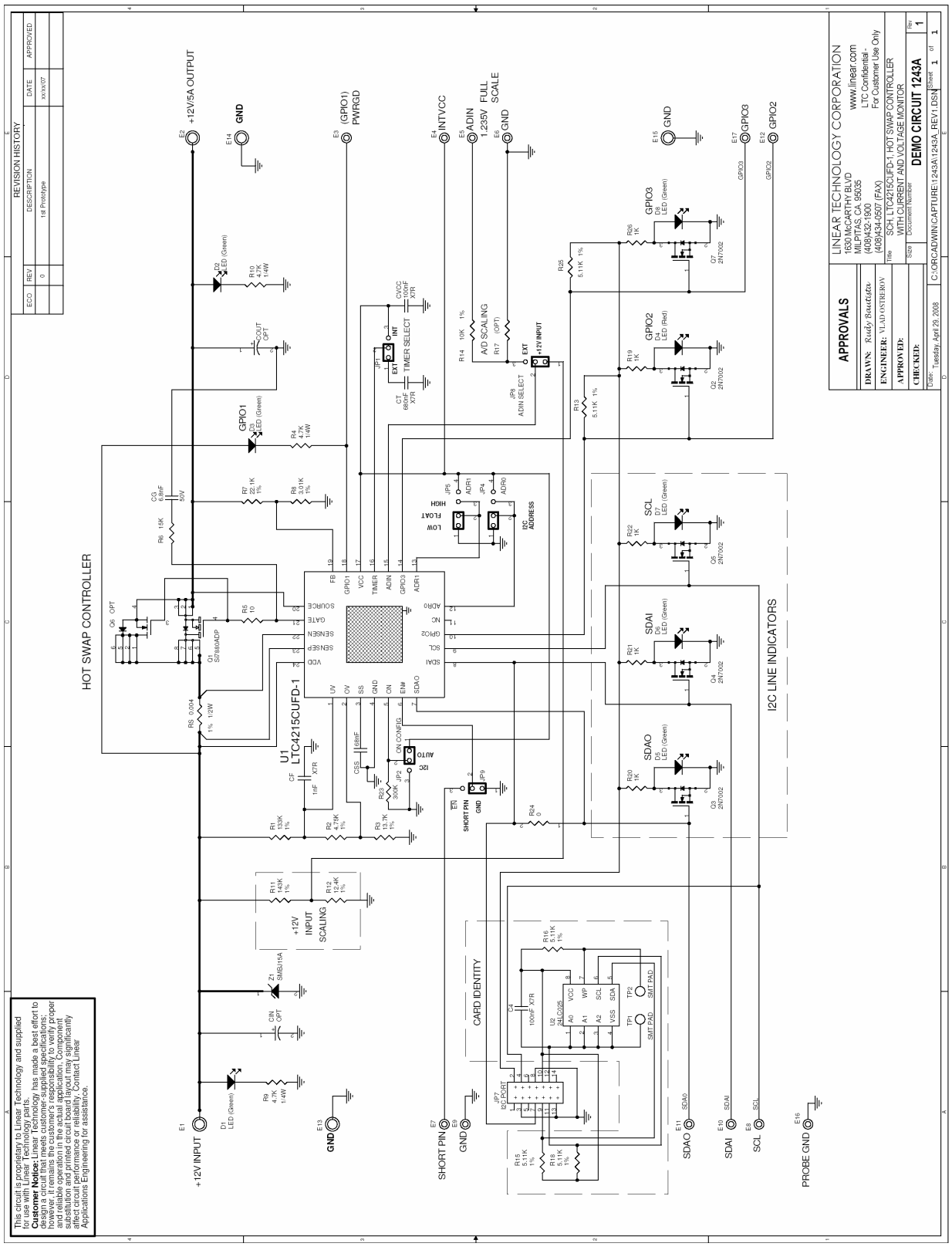


Figure 4. Proper Measurement Equipment Setup


REVISION HISTORY
ECO
REV
DESCRIPTION
DATE
APPROVED
0
1st Prototype
xx/xx/07
HOT SWAP CONTROLLER
U1
LTC4215CUFD-1
I2C LINE INDICATORS
CARD IDENTITY
+12V INPUT SCALING
+12V/5A OUTPUT
GND
(GPIO1) PWRGD
INTVCC
ADIN 1.235V
FULL SCALE
GPIO3
GPIO2
SCL
SDAI
SDAO
SHORT PIN
PROBE GND
+12V INPUT
TIMER SELECT
A/D SCALING
I2C ADDRESS
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CHECKED:
Title: SCH, LTC4215CUFD-1, HOT SWAP CONTROLLER WITH CURRENT AND VOLTAGE MONITOR
Size
Document Number
DEMO CIRCUIT 1243A
Rev 1
Date: Tuesday, April 29, 2008
C:\ORCADWIN\CAPTURE\1243A\1243A_REV1.DSN
Sheet 1 of 1
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