

# 74ABT125

Quad buffer; 3-state

Rev. 7 — 25 November 2015

Product data sheet

## 1. General description

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ( $\overline{1OE}$ ,  $\overline{2OE}$ ,  $\overline{3OE}$ ,  $\overline{4OE}$ ), each controlling one of the 3-state outputs.

## 2. Features and benefits

- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH  $-32$  mA; LOW  $+64$  mA
- Power-up 3-state
- Inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT125D	$-40$ °C to $+85$ °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT125DB	$-40$ °C to $+85$ °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74ABT125PW	$-40$ °C to $+85$ °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ABT125BQ	$-40$ °C to $+85$ °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$ to $\overline{4OE}$	1, 4, 10, 13	output enable input (active LOW)
1A to 4A	2, 5, 9, 12	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
$V_{CC}$	14	supply voltage

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Inputs		Output
$\overline{nOE}$	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values<sup>[1]</sup>

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	-0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
$T_j$	junction temperature		-	150	°C
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] SO14 packages: above 70 °C  $P_{tot}$  derate linearly with 8 mW/K  
 SSOP14 and TSSOP14 packages: above 60 °C  $P_{tot}$  derate linearly with 5.5 mW/K  
 DHVQFN14 packages: above 60 °C  $P_{tot}$  derate linearly with 4.5 mW/K

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		4.5	5.5	V
$V_I$	input voltage		0	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	V
$V_{IL}$	LOW-level Input voltage		-	0.8	V
$I_{OH}$	HIGH-level output current		-32	-	mA
$I_{OL}$	LOW-level output current		-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_{IK} = -18\text{ mA}$	-	-0.9	-1.2	-	-1.2	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IL}$ or $V_{IH}$						
		$V_{CC} = 4.5\text{ V}; I_{OH} = -3\text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0\text{ V}; I_{OH} = -3\text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5\text{ V}; I_{OH} = -32\text{ mA}$	2.0	2.4	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5\text{ V}; I_{OL} = 64\text{ mA}; V_I = V_{IL}$ or $V_{IH}$	-	0.35	0.55	-	0.55	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or $5.5\text{ V}$	-	$\pm 0.01$	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0.0\text{ V}; V_I$ or $V_O \leq 4.5\text{ V}$	-	$\pm 5.0$	$\pm 100$	-	$\pm 100$	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.1\text{ V}; V_O = 0.5\text{ V}; V_I = \text{GND}$ or $V_{CC}; \overline{OE} = \text{don't care}$ <a href="#">[1]</a>	-	$\pm 5.0$	$\pm 50$	-	$\pm 50$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5\text{ V}; V_I = V_{IL}$ or $V_{IH}$						
		$V_O = 2.7\text{ V}$	-	1.0	50	-	50	$\mu\text{A}$
		$V_O = 0.5\text{ V}$	-	-1.0	-50	-	-50	$\mu\text{A}$
$I_{CEX}$	output high leakage current	HIGH-state; $V_O = 5.5\text{ V}; V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or $V_{CC}$	-	5.0	50	-	50	$\mu\text{A}$
$I_O$	output current	$V_{CC} = 5.5\text{ V}; V_O = 2.5\text{ V}$ <a href="#">[2]</a>	-50	-100	-180	-50	-180	mA
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or $V_{CC}$						
		outputs HIGH-state	-	65	250	-	250	$\mu\text{A}$
		outputs LOW-state	-	12	15	-	30	mA
		outputs disabled	-	65	250	-	50	$\mu\text{A}$

Table 6. Static characteristics ...continued

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per control pin; $V_{CC} = 5.5$ V; one control input at 3.4 V, other inputs at $V_{CC}$ or GND <sup>[3]</sup>						
		outputs enabled	-	0.5	1.5	-	1.5	mA
		outputs disabled	-	50	250	-	250	mA
		one enable input at 3.4 V and other inputs at $V_{CC}$ or GND; outputs disabled	-	0.5	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = 0$ V or $V_{CC}$	-	4	-	-	-	pF
$C_O$	output capacitance	outputs disabled; $V_O = 0$ V or $V_{CC}$	-	7	-	-	-	pF

[1] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V, with a transition time of up to 10 ms. From  $V_{CC} = 2.1$  V to  $V_{CC} = 5$  V  $\pm 10$  %, a transition time of up to 100  $\mu$ s is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

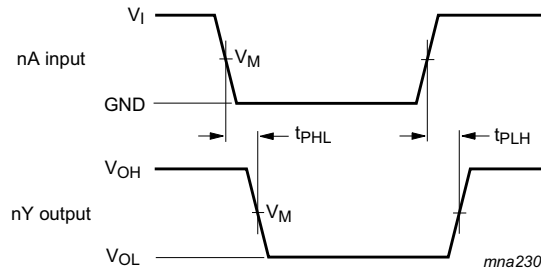
## 10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0$  V. Test circuit is shown in [Figure 8](#).

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0$ V			-40 °C to +85 °C; $V_{CC} = 5.0$ V $\pm 0.5$ V		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$	LOW to HIGH propagation delay	nA to nY, see <a href="#">Figure 6</a>	1.0	2.8	4.1	1.0	4.6	ns
$t_{PHL}$	HIGH to LOW propagation delay	nA to nY; see <a href="#">Figure 6</a>	1.0	3.1	4.6	1.0	4.9	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$\overline{nOE}$ to nY; see <a href="#">Figure 7</a>	1.0	3.2	5.0	1.0	5.9	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$\overline{nOE}$ to nY; see <a href="#">Figure 7</a>	1.0	4.2	6.2	1.0	6.8	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$\overline{nOE}$ to nY; see <a href="#">Figure 7</a>	1.0	4.1	5.4	1.0	6.2	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$\overline{nOE}$ to nY; see <a href="#">Figure 7</a>	1.5	2.8	5.0	1.5	5.5	ns

## 11. Waveforms



$V_M = 1.5\text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (nA) to output (nY)**



$V_M = 1.5\text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**



Table 8. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_I$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
3.0 V	1 MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	open	7.0 V

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

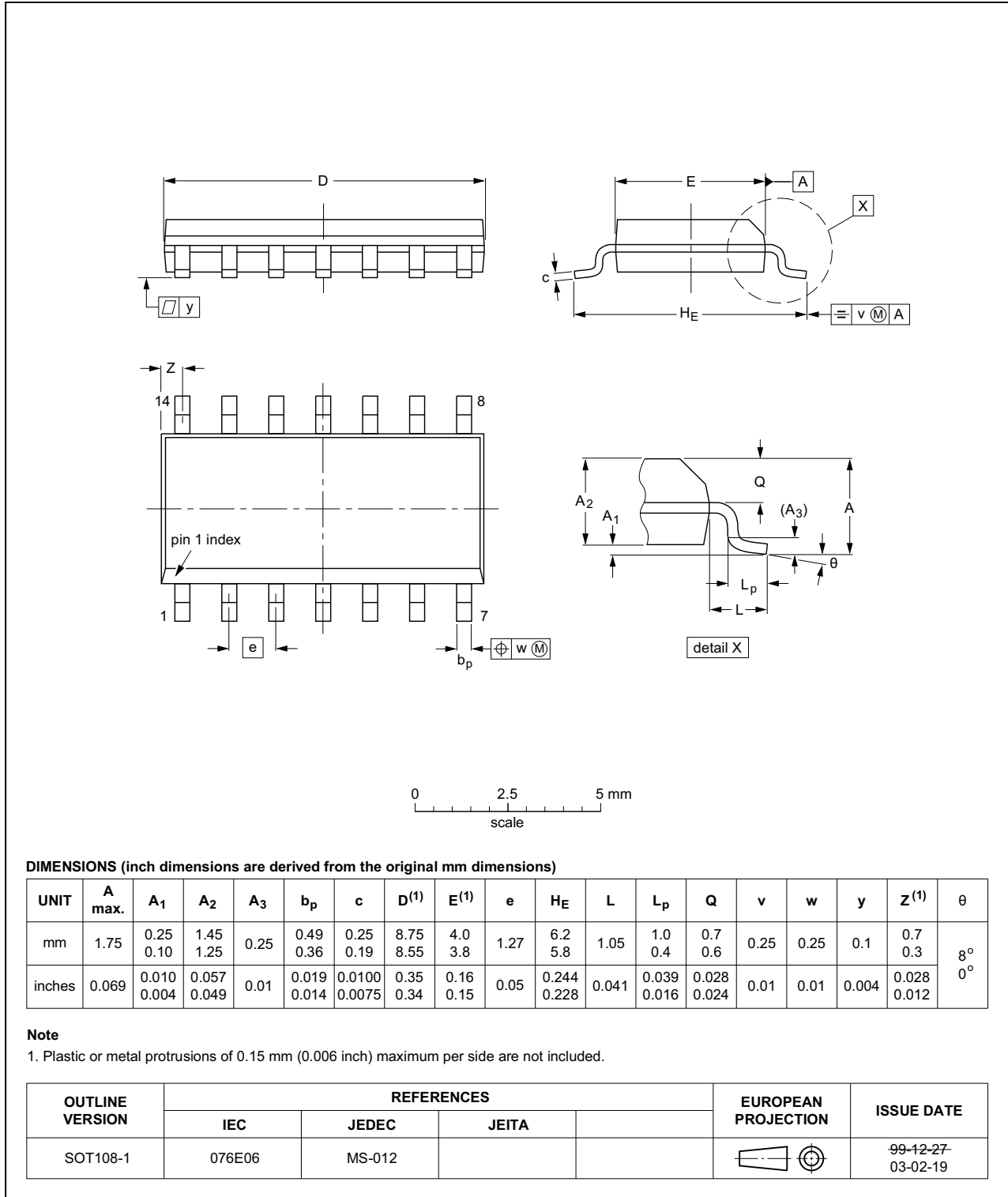


Fig 9. Package outline SOT108-1 (SO14)



SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

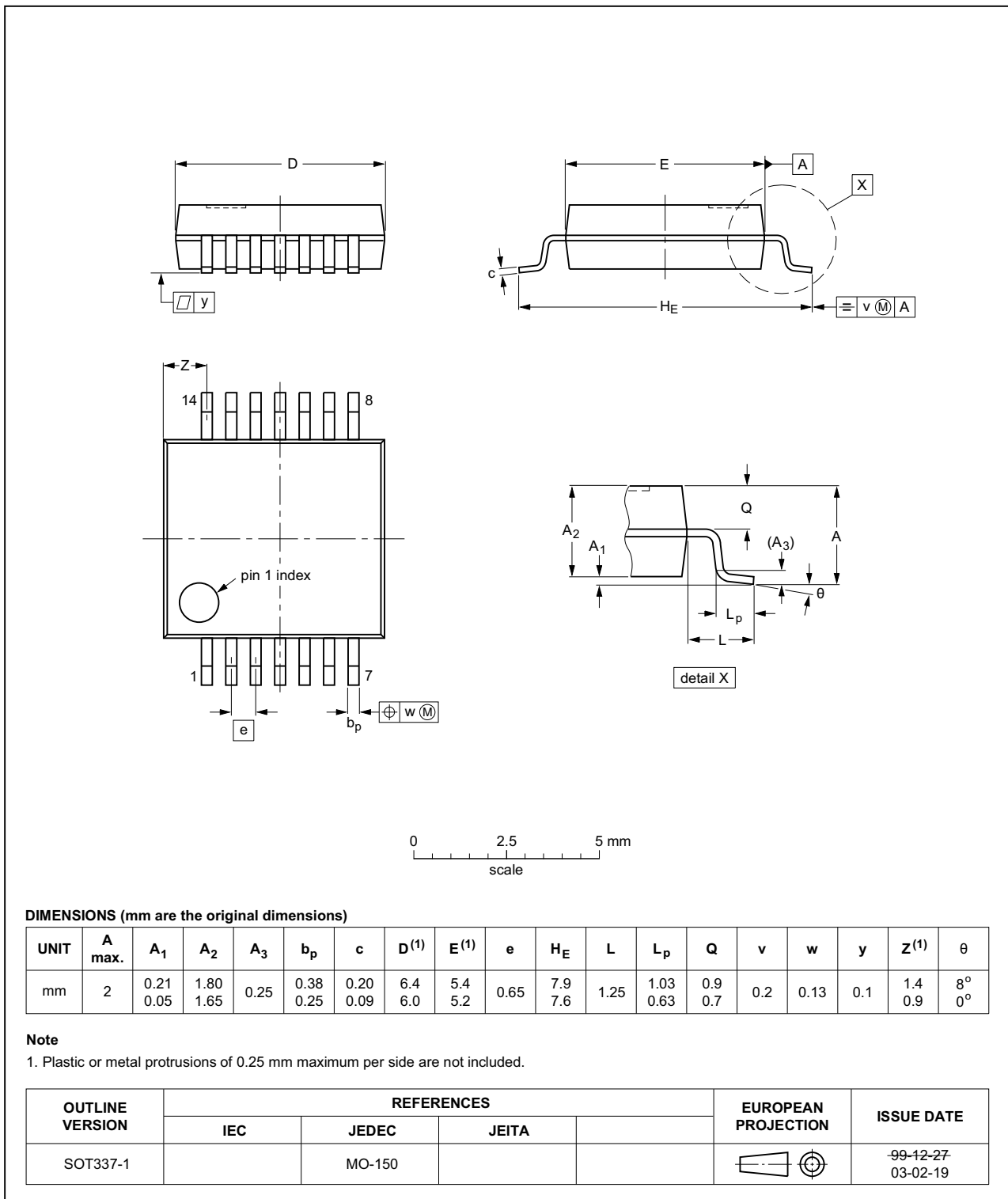


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	BipolarCMOS
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT125 v.7	20151125	Product data sheet	-	74ABT125 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number 74ABT125N (SOT27-1) removed.</li> </ul>			
74ABT125 v.6	20111103	Product data sheet	-	74ABT125 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated</li> </ul>			
74ABT125 v.5	20101124	Product data sheet	-	74ABT125 v.4
74ABT125 v.4	20100427	Product data sheet	-	74ABT125 v.3
74ABT125 v.3	20080429	Product data sheet	-	74ABT125 v.2
74ABT125 v.2	19980116	Product specification	-	74ABT125 v.1
74ABT125 v.1	19960305	-	-	-

## 15. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А