NB6N14S

3.3 V 1:4 AnyLevel™ Differential Input to LVDS Fanout Buffer/Translator

The NB6N14S is a differential 1:4 Clock or Data Receiver and will accept AnyLevel™ differential input signals: LVPECL, CML or LVDS. These signals will be translated to LVDS and four identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6N14S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6N14S has a wide input common mode range from GND + 50 mV to V_{CC} − 50 mV. Combined with the 50 Ω internal termination resistors at the inputs, the NB6N14S is ideal for translating a variety of differential or single−ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6N14S is offered in a small 3 mm x 3 mm 16−QFN package. Application notes, models, and support documentation are available at *www.onsemi.com*.

The NB6N14S is a member of the ECLinPS MAX™ family of high performance products.

Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum RMS Clock Jitter
- Typically 10 ps Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- V_{REF_AC} Reference Output
- TIA/EIA – 644 Compliant
- Functionally Compatible with Existing 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb−Free Devices

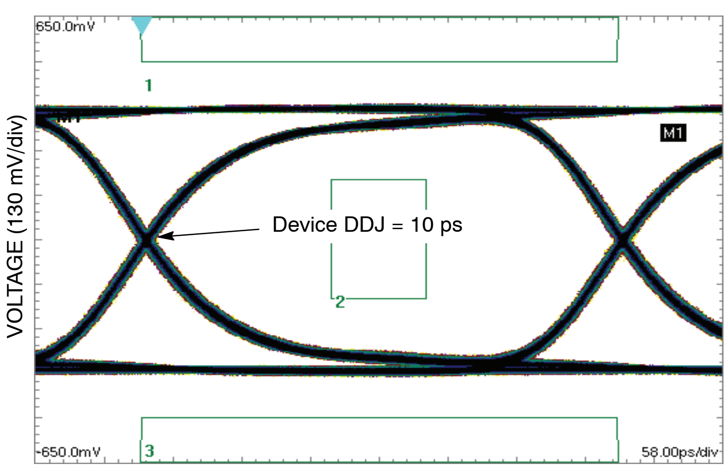

Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23-1} (V_{INPP} = 400 mV; Input Signal DDJ = 14 ps)

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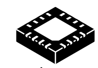
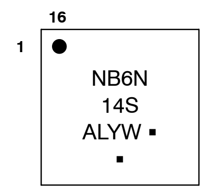
MARKING DIAGRAM*



QFN−16
MN SUFFIX
CASE 485G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

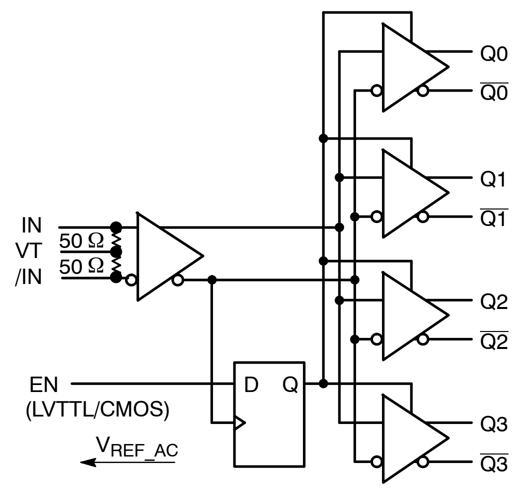


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

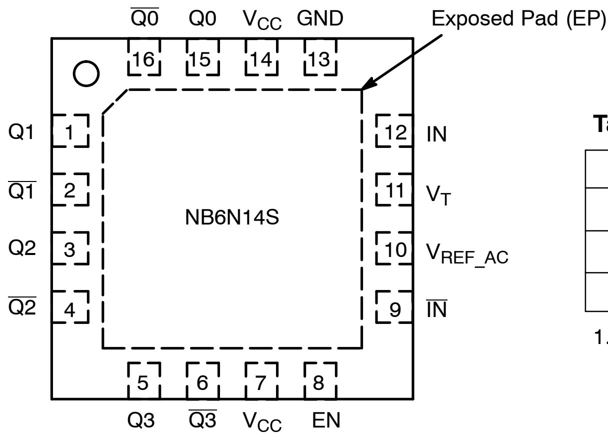


Figure 3. NB6N14S Pinout, 16−pin QFN (Top View)

Table 1. TRUTH TABLE

IN	$\overline{IN}$	EN	Q	$\overline{Q}$
0	1	1	0	1
1	0	1	1	0
x	x	0	0 (Note 1)	1 (Note 1)

1. On next transition of the input signal (IN).

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q1	LVDS Output	Non−inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
2	$\overline{Q1}$	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
3	Q2	LVDS Output	Non−inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
4	$\overline{Q2}$	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	Q3	LVDS Output	Non−inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
6	$\overline{Q3}$	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
7	V_{CC}	−	Positive Supply Voltage.
8	EN	LVTTL / LVCMOS Input	Synchronous Output Enable. When LOW, Q outputs will go LOW and Qb outputs will go HIGH on the next negative transition of IN input. The internal DFF register is clocked on the falling edge of IN input; see Figure 19. The EN pin has an internal pullup resistor and defaults HIGH when left open.
9	$\overline{IN}$	LVPECL, CML, LVDS	Inverted Differential Input
10	V_{REF_AC}	LVPECL Output	The V_{REF_AC} reference output can be used to rebias capacitor−coupled differential or single−ended input signals. For the capacitor−coupled IN and/or INb inputs, V_{REF_AC} should be connected to the VT pin and bypassed to ground with a 0.01 μF capacitor.
11	V_T	LVPECL Output	Internal 100 Ω Center−tapped Termination Pin for IN and $\overline{IN}$
12	IN	LVPECL, CML, LVDS	Non−inverted Differential Input. (Note 2)
13	GND	−	Negative Supply Voltage.
14	V_{CC}	−	Positive Supply Voltage.
15	Q0	LVDS Output	Non−inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
16	$\overline{Q0}$	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

2. In the differential configuration, when the input termination pin (VT) is connected to a termination voltage or left open, and if no signal is applied on IN/$\overline{IN}$ inputs, then the device will be susceptible to self−oscillation.

Table 3. ATTRIBUTES

Characteristics		Value
Moisture Sensitivity (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Transistor Count		225
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.8	V
V_{IN}	Positive Input	GND = 0 V	$V_{IN} \le V_{CC}$	3.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		35 70	mA mA
I_{OSC}	Output Short Circuit Current Line−to−Line (Q to $\overline{Q}$) Line−to−End (Q or $\overline{Q}$ to GND) TIA/EIA − 644 Compliant	Q or $\overline{Q}$ to GND Q to $\overline{Q}$	Continuous Continuous	12 24	mA
I_{REF_AC}	V_{REF_AC} Sink/Source Current			± 0.5	mA
T_A	Operating Temperature Range	QFN−16		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN−16 QFN−16	41.6 35.2	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P (Note 4)	QFN−16	4.0	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Note 9)		65	100	mA
DIFFERENTIAL INPUTS DRIVEN SINGLE−ENDED (Figures 10, 11, 15, and 17)					
V_{th}	Input Threshold Reference Voltage Range (Note 8)	GND +100		V_{CC} − 100	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	GND		V_{th} − 100	mV
V_{REF_AC}	Reference Output Voltage (Note 11)	V_{CC} − 1.600	V_{CC} − 1.425	V_{CC} − 1.300	V
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6, 7, 8, 9, 16, and 18)					
V_{IHD}	Differential Input HIGH Voltage	100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CC} − 100	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	GND + 50		V_{CC} − 50	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	100		V_{CC}	mV
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω
LVDS OUTPUTS (Note 5)					
V_{OD}	Differential Output Voltage	250		450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States (Note 10)	0	1	25	mV
V_{OS}	Offset Voltage (Figure 14)	1125		1375	mV
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States (Note 10)	0	1	25	mV
V_{OH}	Output HIGH Voltage (Note 6)		1425	1600	mV
V_{OL}	Output LOW Voltage (Note 7)	900	1075		mV
LVTTL/LVCMOS INPUTS					
V_{IH}	Input HIGH Voltage (Note 7, 8)	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage (Note 7, 8)	GND		0.8	V
I_{IH}	Input HIGH Current	−150		150	μA
I_{IL}	Input LOW Current	−150		150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 13.
6. V_{OH}max = V_{OS}max + ½ V_{OD}max.
7. V_{OL}max = V_{OS}min − ½ V_{OD}max.
8. V_{th} is applied to the complementary input when operating in single−ended mode.
9. Input termination pins open, D/$\overline{D}$ at the DC level within V_{CMR} and output pins loaded with R_L = 100 Ω across differential.
10. Parameter guaranteed by design verification not tested in production.
11. V_{REF_AC} used to rebias capacitor−coupled inputs only (see Figures 10 and 11).

Table 6. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V; (Note 12)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{inMax}	Maximum Input Clock Frequency	2.0			2.0			2.0			GHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) f_{in} ≤ 1.0 GHz (Figure 4) f_{in}= 1.5 GHz f_{in}= 2.0 GHz	220 200 170	350 300 270		220 200 170	350 300 270		220 200 170	350 300 270		mV
f_{DATA}	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t_{PLH}, t_{PHL}	Differential Input to Differential Output Propagation Delay	300	450	600	300	450	600	300	450	600	ps
t_s t_h	Setup Time Hold Time	300 500	60 70		300 500	60 70		300 500	60 70		
t_{SKEW}	Within Device Skew (Note 17) Device−to−Device Skew (Note 16)		5 30	20 200		5 30	20 200		5 30	20 200	ps
t_{JITTER}	RMS Random Clock Jitter (Note 14) f_{in} = 1.0 GHz f_{in} = 1.5 GHz Deterministic Jitter (Note 15) f_{DATA} = 622 Mb/s f_{DATA} = 1.5 Gb/s f_{DATA} = 2.488 Gb/s		0.5 0.5 10 10 10			0.5 0.5 10 10 10			0.5 0.5 10 10 10		ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 13)	100		V_{CC}− GND	100		V_{CC}− GND	100		V_{CC}− GND	mV
t_r t_f	Output Rise/Fall Times @ 250 MHz Q, $\overline{Q}$ (20% − 80%)	60	120	190	60	120	190	60	120	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing $V_{INPPmin}$ with 50% duty cycle clock source and V_{CC} − 1400 mV offset. All loading with an external R_L = 100 Ω. Input edge rates 150 ps (20%−80%). See Figure 13.
13. Input voltage swing is a single−ended measurement operating in differential mode.
14. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.
15. Deterministic jitter with input NRZ data at PRBS 2^{23}−1 and K28.5.
16. Skew is measured between outputs under identical transition @ 250 MHz.
17. The worst case condition between Q0/$\overline{Q0}$ and Q1/$\overline{Q1}$ from either D0/$\overline{D0}$ or D1/$\overline{D1}$, when both outputs have the same transition.

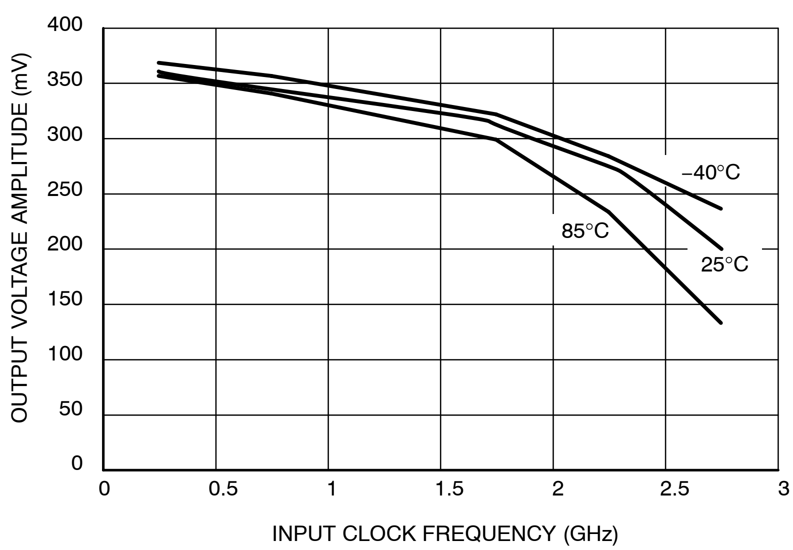


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) and Temperature (@ V_{CC} = 3.3 V)

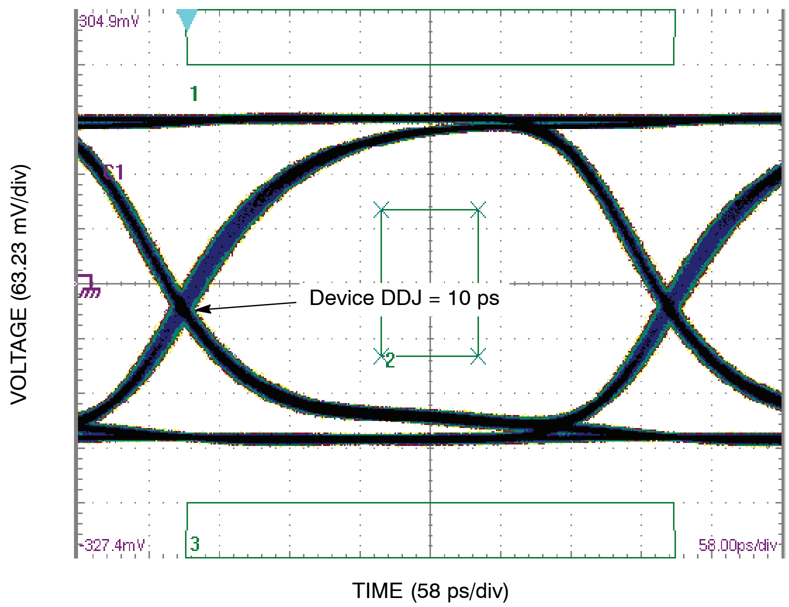


Figure 5. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23-1} and OC48 mask (V_{INPP} = 100 mV; Input Signal DDJ = 14 ps)

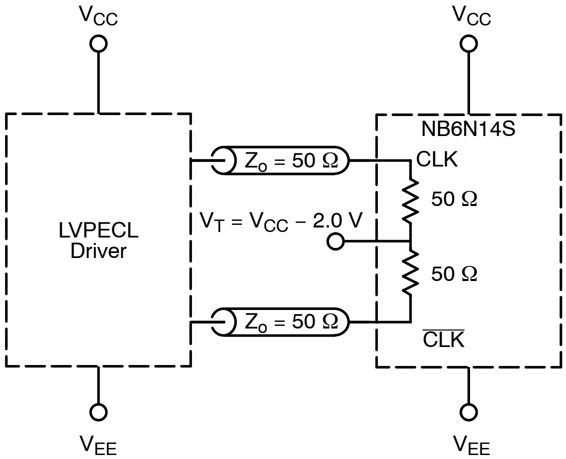


Figure 6. LVPECL Interface

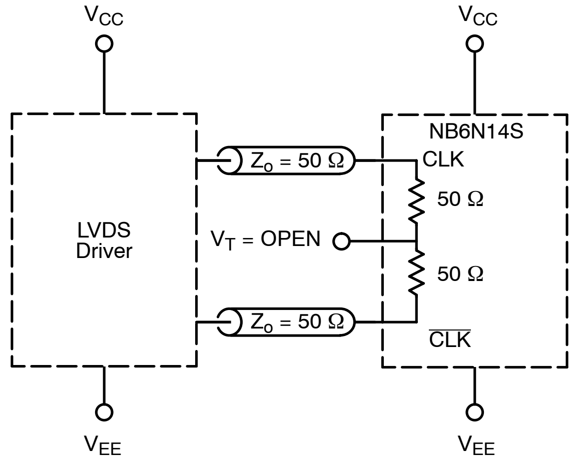


Figure 7. LVDS Interface

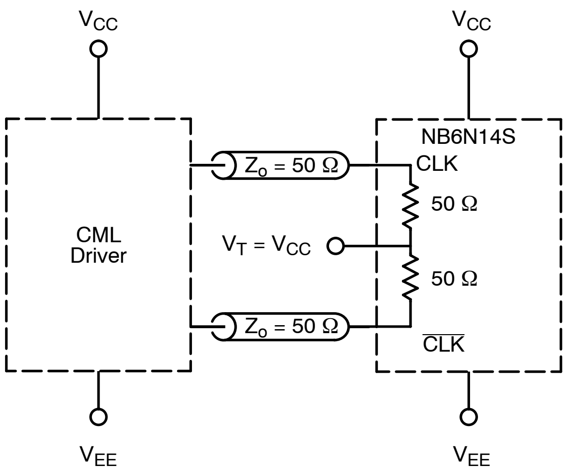


Figure 8. Standard 50 Ω Load CML Interface

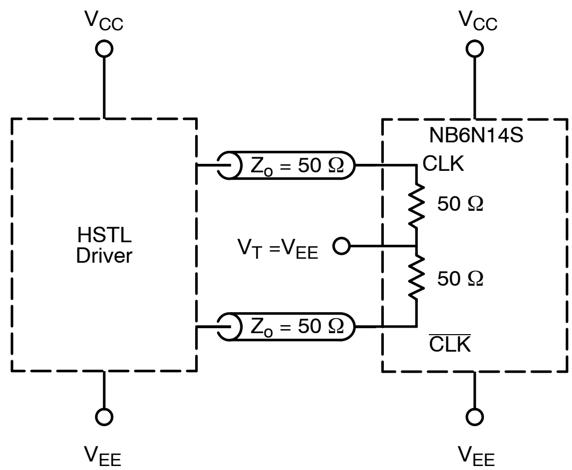


Figure 9. Standard 50 Ω Load HSTL Interface

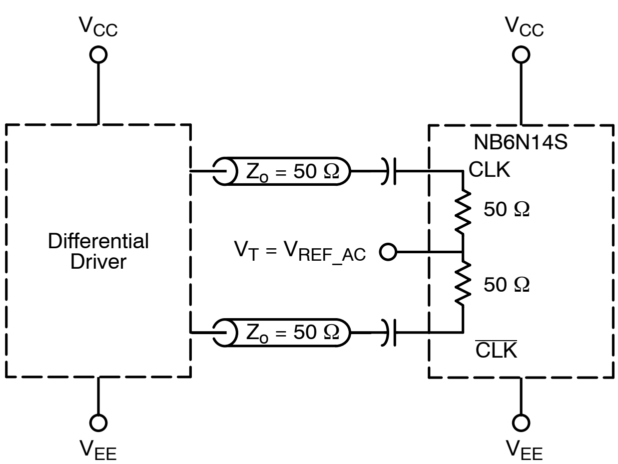


Figure 10. Capacitor−Coupled Differential Interface (V_T Connected to V_{REF_AC})

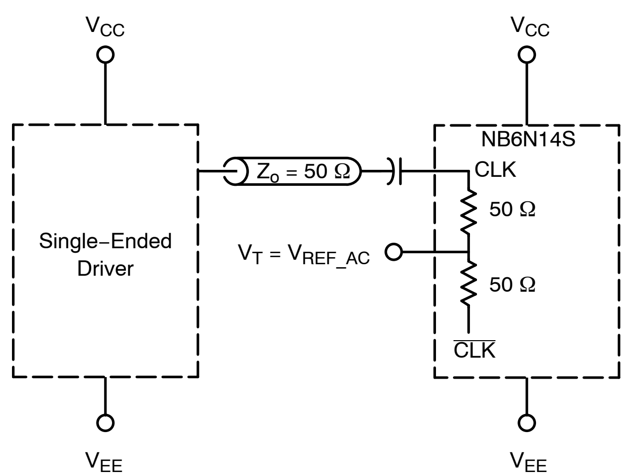


Figure 11. Capacitor−Coupled Single−Ended Interface (V_T Connected to V_{REF_AC})

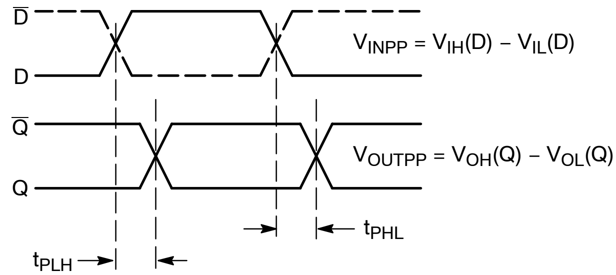


Figure 12. AC Reference Measurement

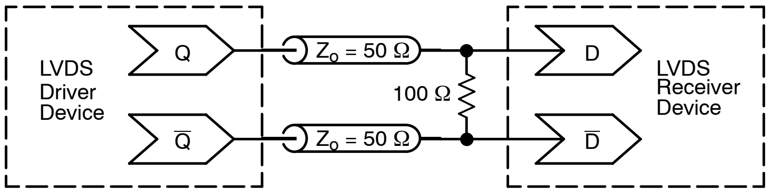


Figure 13. Typical LVDS Termination for Output Driver and Device Evaluation

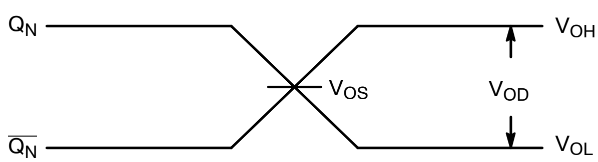


Figure 14. LVDS Output

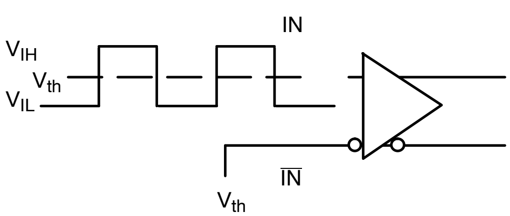


Figure 15. Differential Input Driven Single−Ended

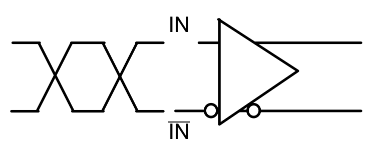


Figure 16. Differential Inputs Driven Differentially

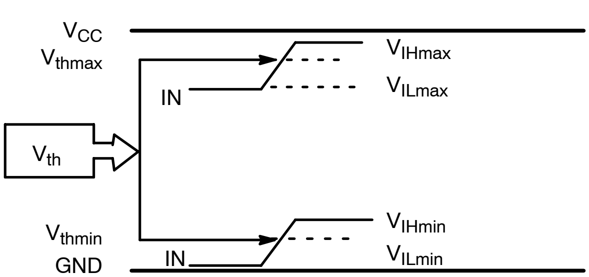


Figure 17. V_{th} Diagram

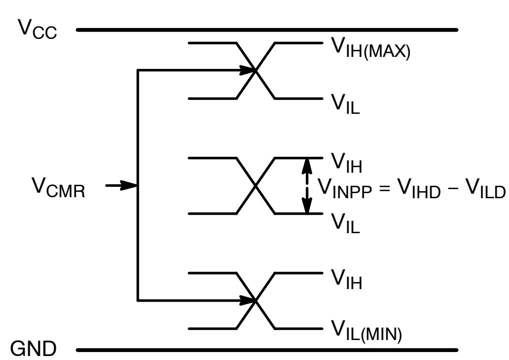


Figure 18. V_{CMR} Diagram

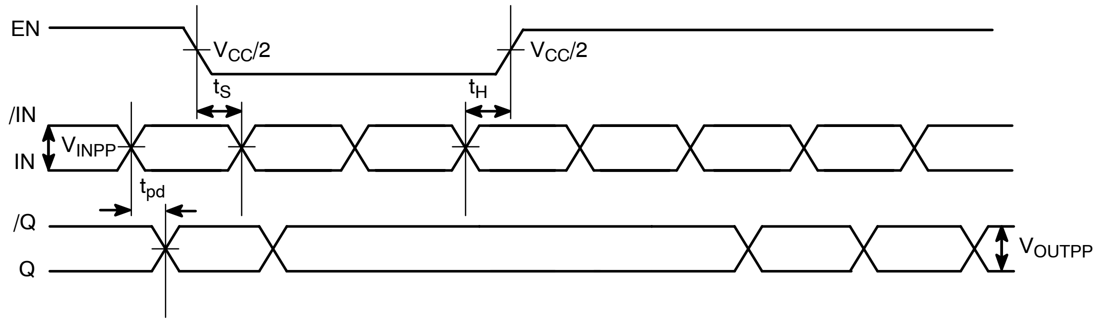


Figure 19. EN Timing Diagram

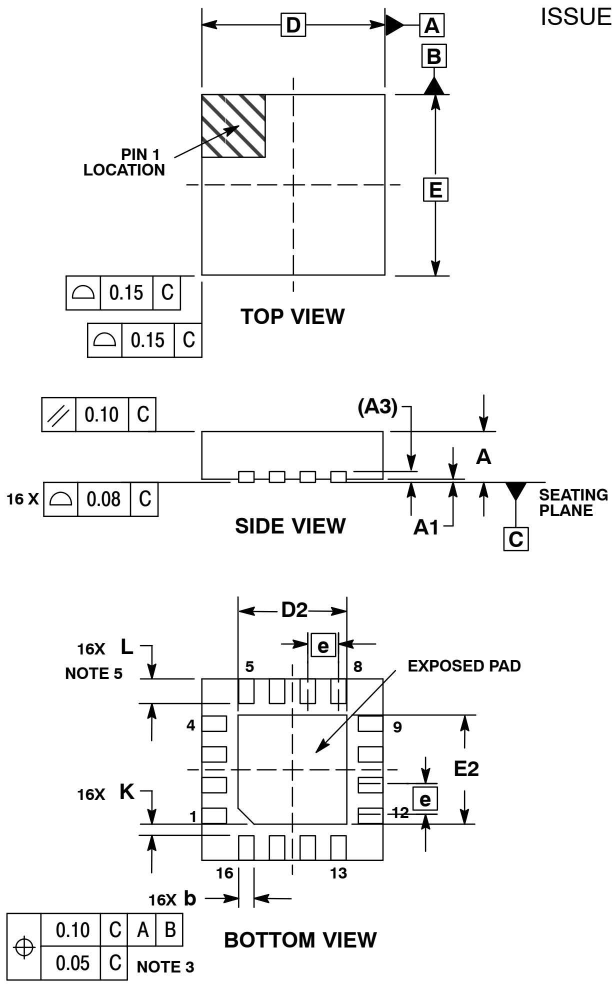
ORDERING INFORMATION

Device	Package	Shipping†
NB6N14SMNG	QFN−16, 3 X 3 mm (Pb−Free)	123 Units / Rail
NB6N14SMNR2G	QFN−16, 3 X 3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

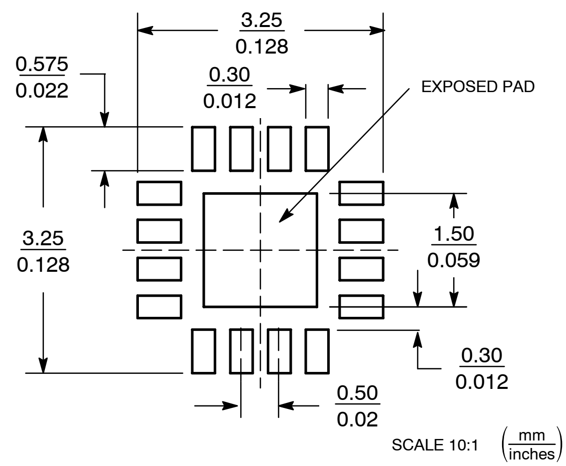
16 PIN QFN
CASE 485G−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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OCEAN CHIPS
Океан Электроники
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Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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AVIC JONHON

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Разъемы специального, военного и аэрокосмического назначения:

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А