

NVMFS4C05N

Power MOSFET

30 V, 116 A, Single N-Channel, SO-8 FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVMFS4C05NWF – Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJA} (Notes 1, 2 and 4)	Steady State	T _A = 25°C	I _D	24.7	A
		T _A = 80°C		19.6	
Power Dissipation R _{θJA} (Notes 1, 2 and 4)		T _A = 25°C	P _D	3.61	W
Continuous Drain Current R _{θJC} (Notes 1, 2, 3 and 4)		T _C = 25°C	I _D	116	A
Continuous Drain Current R _{θJC} (Notes 1, 2, 3 and 4)		T _C = 80°C		92	
Power Dissipation R _{θJC} (Notes 1, 2, 3 and 4)		T _C = 25°C	P _D	79	W
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	174	A
Operating Junction and Storage Temperature			T _J , T _{STG}	−55 to +175	°C
Source Current (Body Diode)			I _S	72	A
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, I _L = 29 A _{pk} , L = 0.1 mH)			E _{AS}	42	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

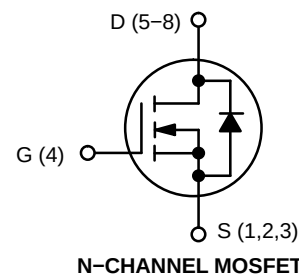
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as one second is higher but dependent on pulse duration and duty cycle.



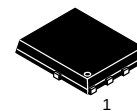
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	3.4 m Ω @ 10 V	116 A
	5.0 m Ω @ 4.5 V	

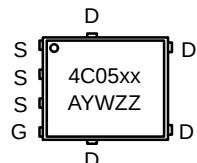


N-CHANNEL MOSFET



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4C05N = Specific Device Code for NVMFS4C05N
4C05WF = Specific Device Code of NVMFS4C05NWF
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFS4C05NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NVMFS4C05NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel
NVMFS4C05NWFT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NVMFS4C05NWFT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVMFS4C05N

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.9	°C/W
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	41.6	

5. Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			12		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	μA
		$T_J = 125^\circ\text{C}$			10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.3		2.2	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.1		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		2.7	3.4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		4.0	5.0	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		68		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$	0.3	1.0	2.0	Ω

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1972		pF
Output Capacitance	C_{OSS}			1215		
Reverse Transfer Capacitance	C_{RSS}			59		
Capacitance Ratio	C_{RSS}/C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.030		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		14		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.3		
Gate-to-Source Charge	Q_{GS}			6.0		
Gate-to-Drain Charge	Q_{GD}			5.0		
Gate Plateau Voltage	V_{GP}			3.1		V
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		30		nC

SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		11		ns
Rise Time	t_r			32		
Turn-Off Delay Time	$t_{d(OFF)}$			21		
Fall Time	t_f			7.0		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		8.0		ns
Rise Time	t_r			26		
Turn-Off Delay Time	$t_{d(OFF)}$			26		
Fall Time	t_f			5.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.77	1.1	V
			$T_J = 125^\circ\text{C}$		0.62		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$			40.2		ns
Charge Time	t_a				20.3		
Discharge Time	t_b				19.9		
Reverse Recovery Charge	Q_{RR}				30.2		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

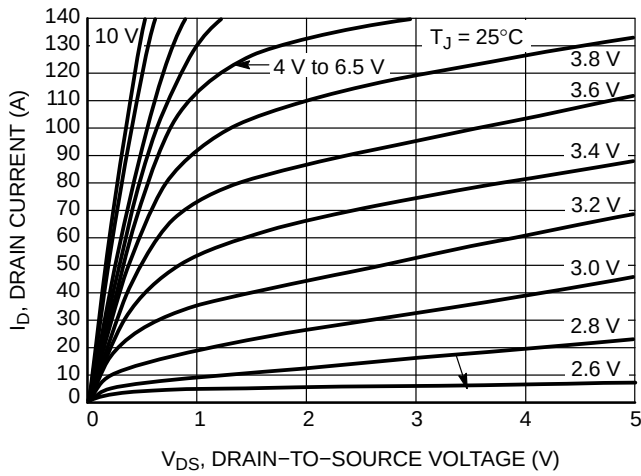


Figure 1. On-Region Characteristics

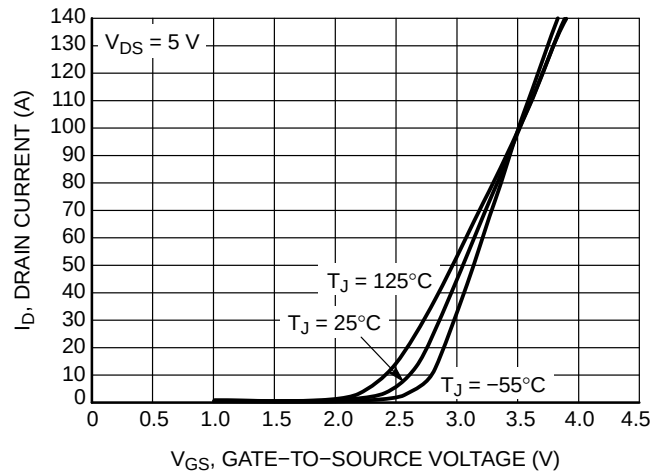


Figure 2. Transfer Characteristics

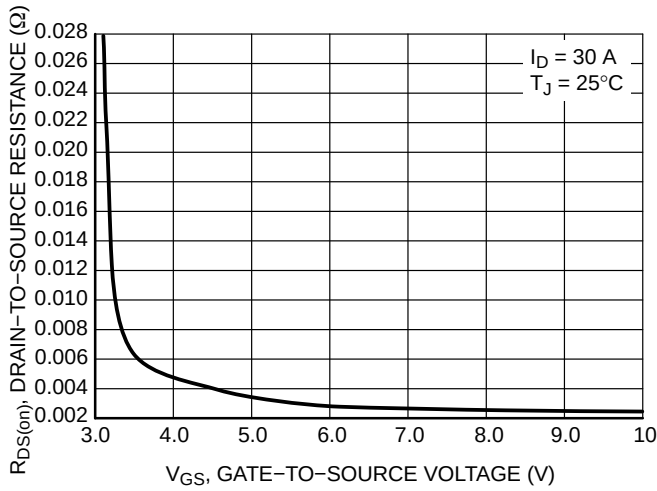


Figure 3. On-Resistance vs. V_{GS}

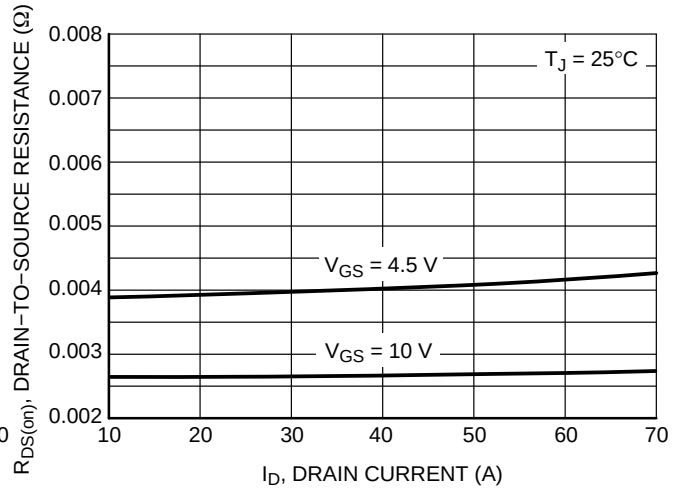


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

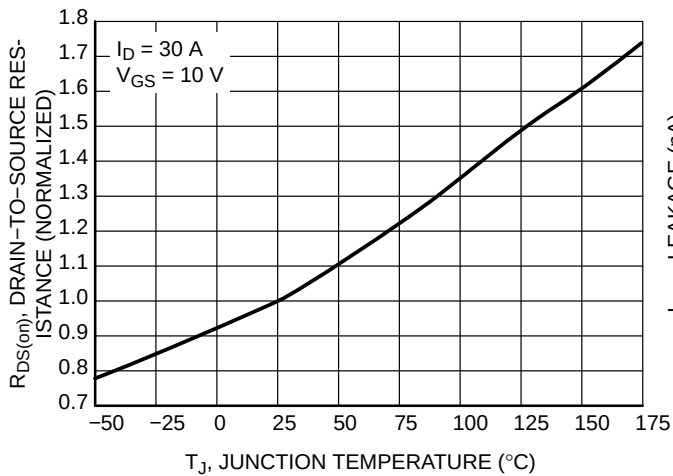


Figure 5. On-Resistance Variation with Temperature

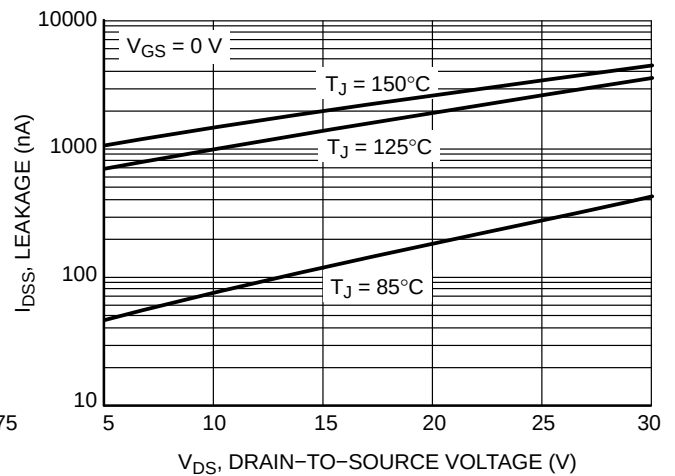


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

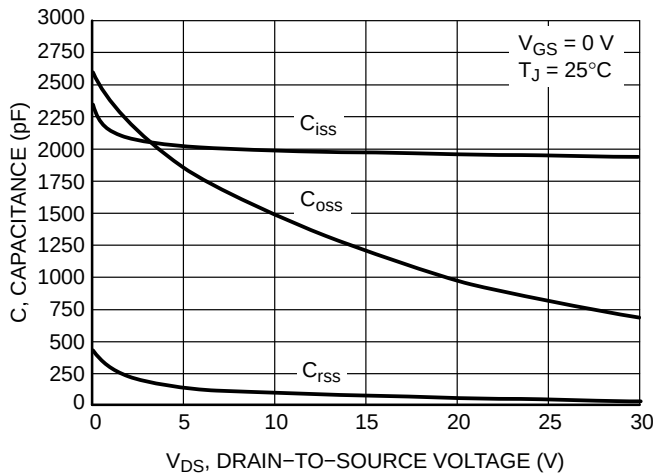


Figure 7. Capacitance Variation

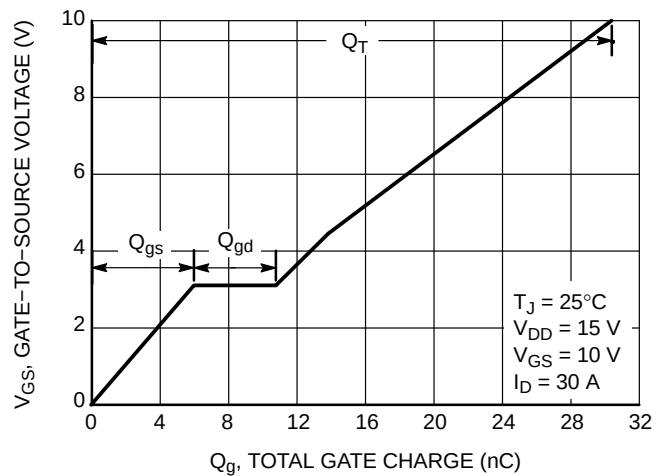


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

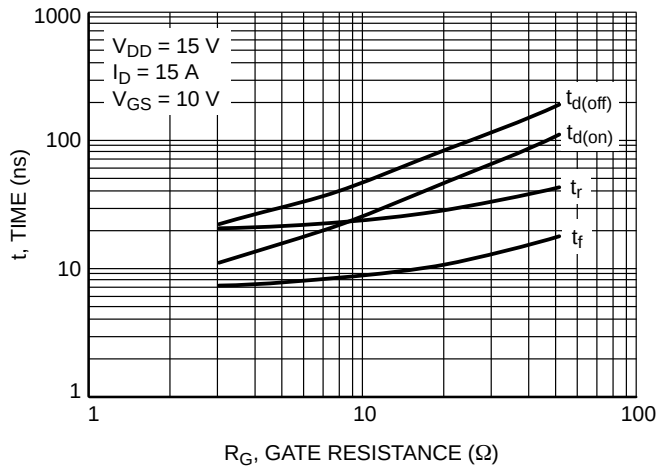


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

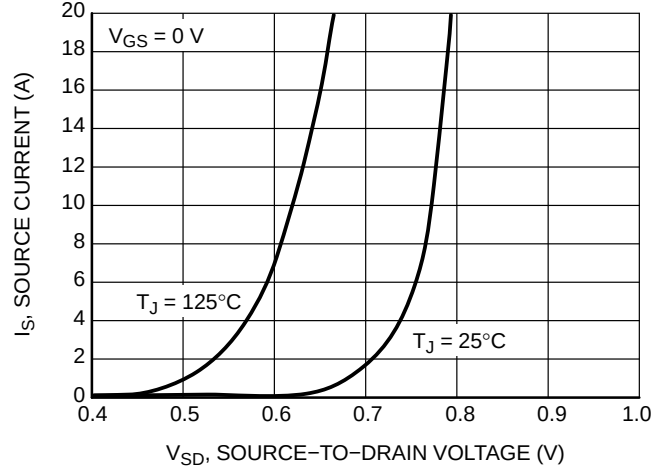


Figure 10. Diode Forward Voltage vs. Current

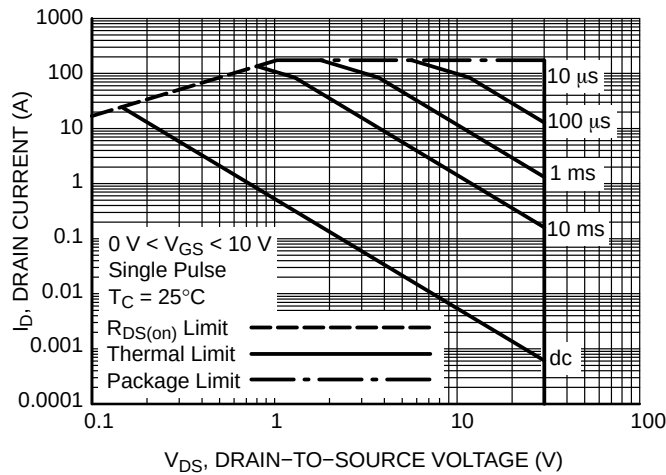


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

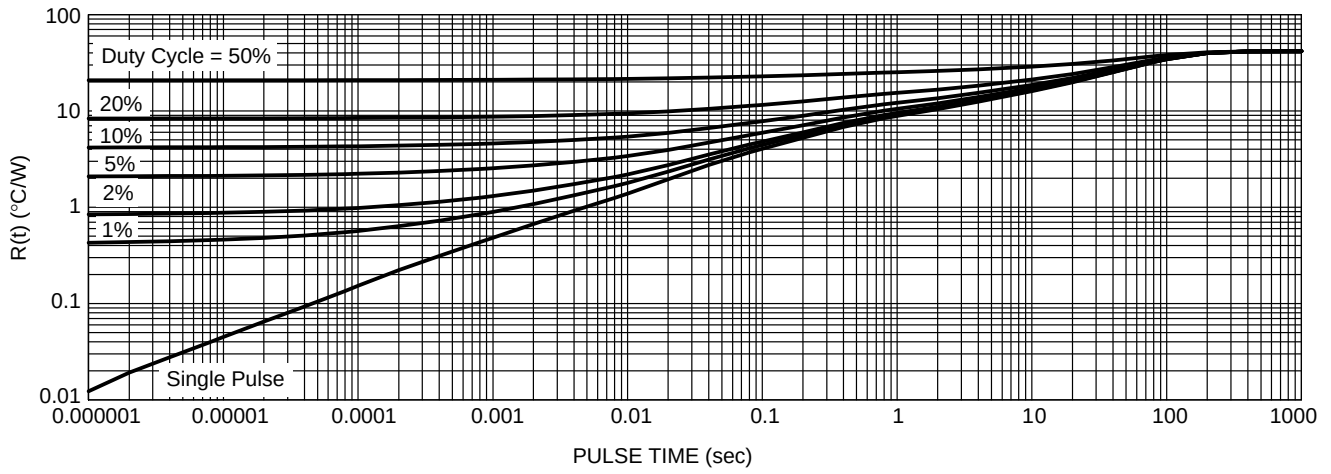


Figure 12. Thermal Response

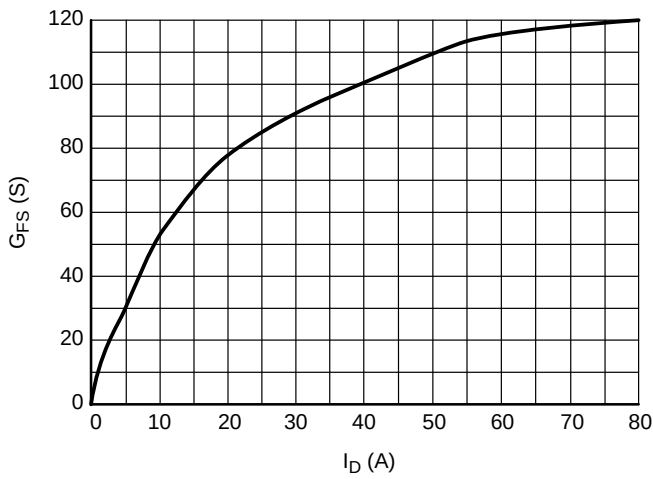


Figure 13. G_{FS} vs. I_D

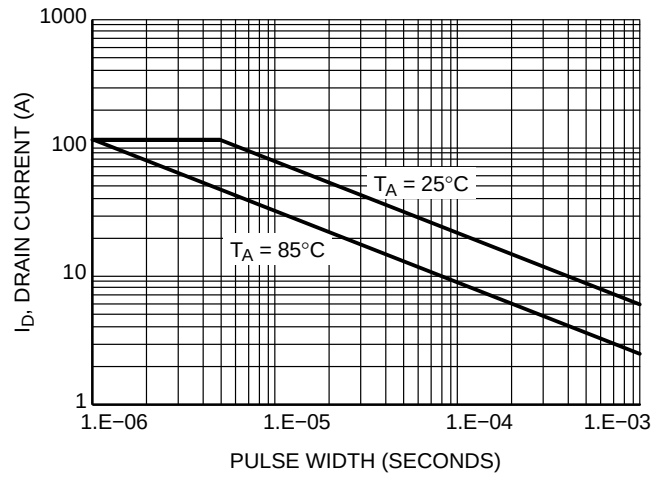


Figure 14. Avalanche Characteristics

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PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE K

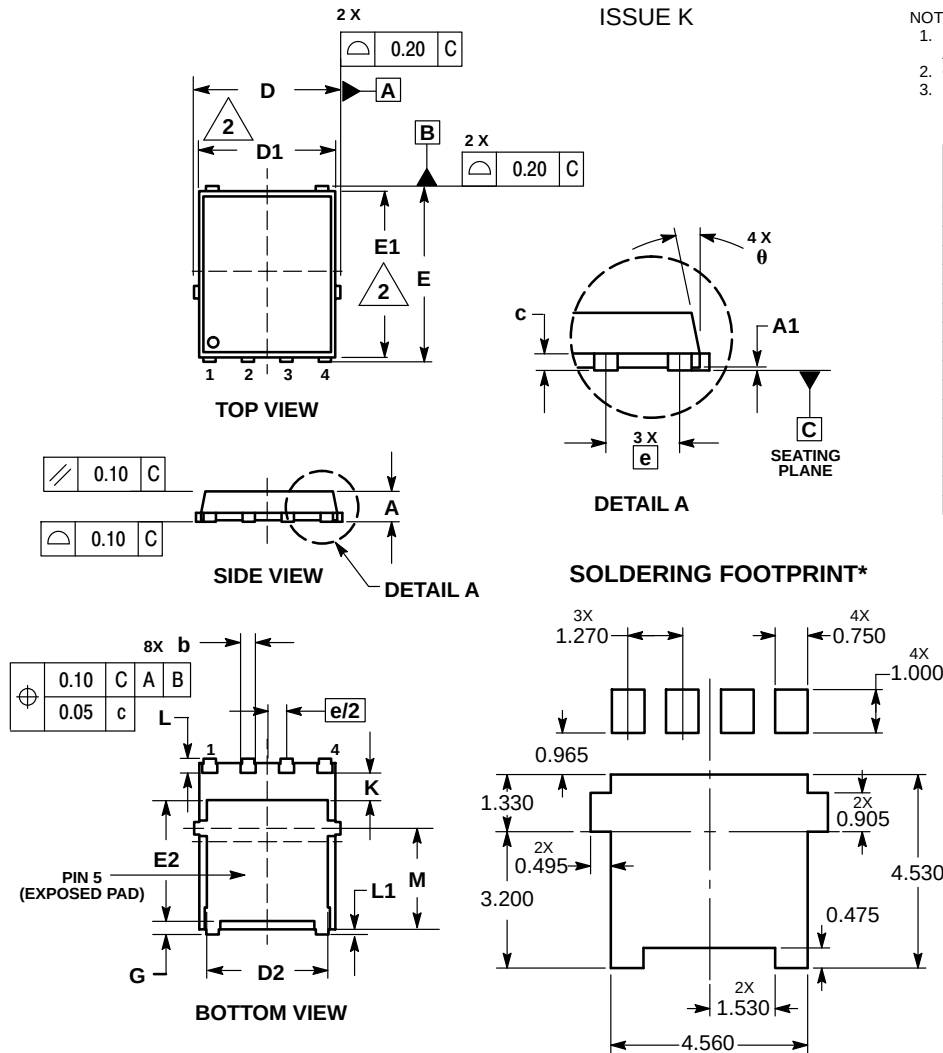
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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