Dual, 200 mA, Low Noise, High PSRR Voltage Regulator

Data Sheet

ADP220/ADP221

FEATURES

- Input voltage range: 2.5 V to 5.5 V
- Dual independent 200 mA low dropout voltage regulators
- Miniature 6-ball, 1.0 mm × 1.5 mm WLCSP and 6-ball bumped bare die
- Initial accuracy: ±1%
- Stable with 1 µF ceramic output capacitors
- No noise bypass capacitor required
- Two independent logic controlled enables
- Overcurrent and thermal protection
- Active output pull-down (ADP221)
- Key specifications
  - High PSRR
    - 76 dB PSRR up to 1 kHz
    - 70 dB PSRR at 10 kHz
    - 60 dB PSRR at 100 kHz
    - 40 dB PSRR at 1 MHz
  - Low output noise
    - 27 µV rms typical output noise at V_{OUT} = 1.2 V
    - 50 µV rms typical output noise at V_{OUT} = 2.8 V
- Excellent transient response
- Low dropout voltage: 150 mV @ 200 mA load
- 60 µA typical ground current at no load, both LDOs enabled
- 100 µs fast turn-on circuit
- Guaranteed 200 mA output current per regulator
- −40°C to +125°C junction temperature

APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment
- Portable medical devices
- Post dc-to-dc regulation

TYPICAL APPLICATION CIRCUITS

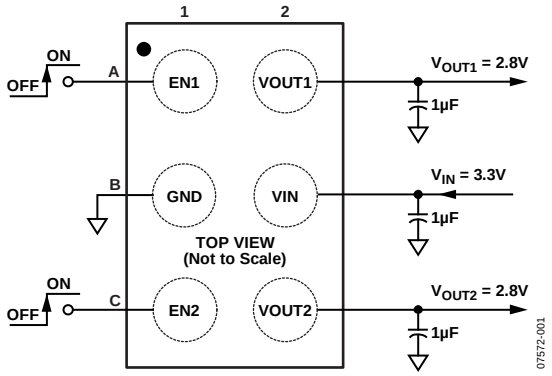

Figure 1. Typical Application Circuit

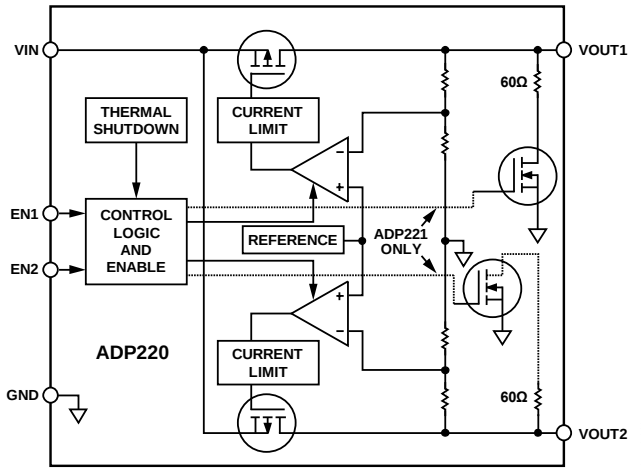

Figure 2. Block Diagram of the ADP220/ADP221

GENERAL DESCRIPTION

The 200 mA dual output ADP220/ADP221 combine high PSRR, low noise, low quiescent current, and low dropout voltage in a voltage regulator ideally suited for wireless applications with demanding performance and board space requirements.

The low quiescent current, low dropout voltage, and wide input voltage range of the ADP220/ADP221 extend the battery life of portable devices. The ADP220/ADP221 maintain power supply rejection greater than 60 dB for frequencies as high as 100 kHz while operating with a low headroom voltage. The ADP220 offers much lower noise performance than competing LDOs without the need for a noise bypass capacitor. The ADP221 also includes an active pull-down to quickly discharge output loads.

The ADP220/ADP221 are available in a miniature 6-ball WLCSP package and 6-ball bumped bare die and is stable with tiny 1 µF ± 30% ceramic output capacitors, resulting in the smallest possible board area for a wide variety of portable power needs.

The ADP220/ADP221 are available in many output voltage combinations, ranging from 0.8 V to 3.3 V, and offer overcurrent and thermal protection to prevent damage in adverse conditions.

Rev. H

Document Feedback

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REVISION HISTORY

1/13—Rev. G to Rev. H

Changes to Undervoltage Lockout Input Voltage Rising Parameter and Undervoltage Lockout Input Voltage Falling Parameter, Table 1 3

11/12—Rev. F to Rev. G

Added 6-Ball Bumped Bare Die (CD-6-7) ..... Universal
Change to Undervoltage Lockout Input Voltage Rising Parameter, Table 1 3
Updated Outline Dimensions 17
Moved Ordering Guide 18

4/12—Rev. E to Rev. F

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11/10—Rev. D to Rev. E

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5/10—Rev. C to Rev. D

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1/10—Rev. B to Rev. C

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10/09—Rev. A to Rev. B

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Changes to Table 3 and Table 4 5
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3/09—Rev. 0 to Rev. A

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10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.5 V (whichever is greater), EN1 = EN2 = V_{IN}, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = C_{OUT1} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.5		5.5	V
OPERATING SUPPLY CURRENT WITH BOTH REGULATORS ON	I_{GND}	I_{OUT} = 0 µA		60		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			120	µA
		I_{OUT} = 10 mA		70		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			140	µA
		I_{OUT} = 200 mA		120		µA
		I_{OUT} = 200 mA, T_J = −40°C to +125°C			220	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN1= EN2 = GND		0.1		µA
		EN1= EN2 = GND, T_J = −40°C to +125°C			2	µA
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT}		−1		+1	%
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−2		+2	%
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V		0.01		%/V
		V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.03		+0.03	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 200 mA		0.001		%/mA
		I_{OUT} = 1 mA to 200 mA, T_J = −40°C to +125°C			0.003	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	V_{OUT} = 3.3 V				mV
		I_{OUT} = 10 mA		7.5		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			12	mV
		I_{OUT} = 200 mA		150		mV
		I_{OUT} = 200 mA, T_J = −40°C to +125°C			230	mV
START-UP TIME[3]	$t_{START-UP}$	V_{OUT} = 3.3 V, both initially off, enable one		240		µs
		V_{OUT} = 0.8 V, both initially off, enable one		100		µs
		V_{OUT} = 3.3 V, one initially on, enable second		180		µs
		V_{OUT} = 0.8 V, one initially on, enable second		20		µs
ACTIVE PULL-DOWN RESISTANCE	$t_{SHUTDOWN}$	V_{OUT} = 2.8 V, R_{LOAD} = ∞, C_{OUT} = 1 µF, ADP221 only		80		Ω
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}		240	300	440	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		155		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN1 = EN2 = V_{IN} or GND		0.1		µA
		EN1 = EN2 = V_{IN} or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$				2.45	V
Input Voltage Falling	$UVLO_{FALL}$		2.2		2.35	V
Hysteresis	$UVLO_{HYS}$			100		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		56		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.8 V		50		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 2.5 V		45		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 1.2 V		27		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	V_{IN} = 2.5 V, V_{OUT} = 0.8 V, I_{OUT} = 100 mA				
		100 Hz		76		dB
		1 kHz		76		dB
		10 kHz		70		dB
		100 kHz		60		dB
		1 MHz		40		dB
		V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 100 mA				
		100 Hz		68		dB
		1 kHz		68		dB
		10 kHz		68		dB
		100 kHz		60		dB
		1 MHz		40		dB

[1] Based on an end-point calculation using 1 mA and 200 mA loads.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.
[3] Start-up time is defined as the time between the rising edge of ENx to V_{OUTx} being at 90% of its nominal value.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		1	Ω

[1] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with LDOs.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	–0.3 V to +6.5 V
VOUT1, VOUT2 to GND	–0.3 V to VIN
EN1, EN2 to GND	–0.3 V to +6.5 V
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP220/ADP221 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a four-layer, 4 inch × 3 inch, circuit board. Refer to JEDEC JESD 51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package. Factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JEDEC JESD51-8 and JESD51-12 for more detailed information on Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	Ψ_{JB}	Unit
6-Ball, 0.5 mm Pitch WLCSP	260	43.8	°C/W
6-Ball Bumped Bare Die	260	43.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

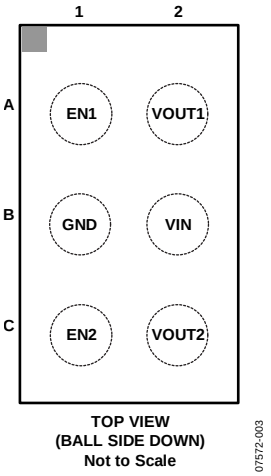

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	EN1	Enable Input for Regulator 1. Drive EN1 high to turn on Regulator 1; drive it low to turn off Regulator 1. For automatic startup, connect EN1 to VIN.
B1	GND	Ground Pin.
C1	EN2	Enable Input for Regulator 2. Drive EN2 high to turn on Regulator 2; drive it low to turn off Regulator 2. For automatic startup, connect EN2 to VIN.
A2	VOUT1	Regulated Output Voltage 1. Connect a 1 µF or greater output capacitor between VOUT1 and GND.
B2	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
C2	VOUT2	Regulated Output Voltage 2. Connect a 1 µF or greater output capacitor between VOUT2 and GND.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3 V, V_{OUT1} = V_{OUT2} = 2.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT1} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

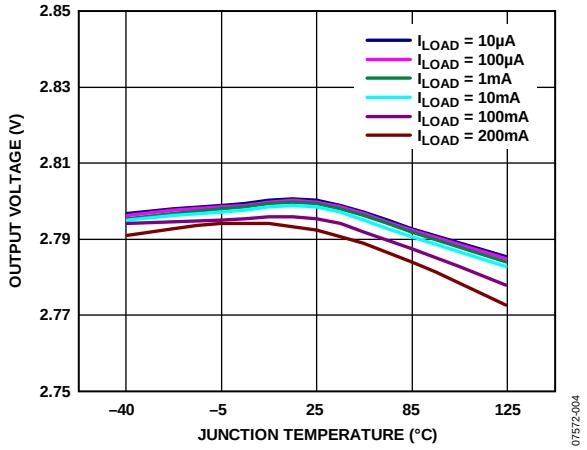

Figure 4. Output Voltage vs. Junction Temperature

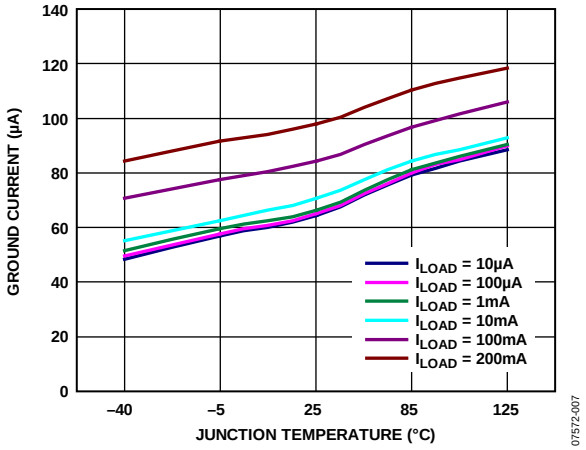

Figure 7. Ground Current vs. Junction Temperature, Single Output Loaded

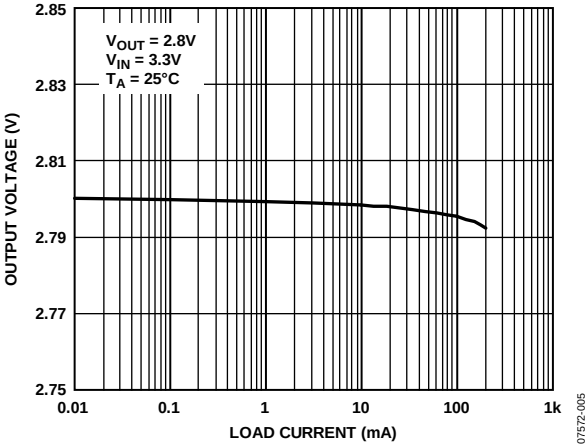

Figure 5. Output Voltage vs. Load Current

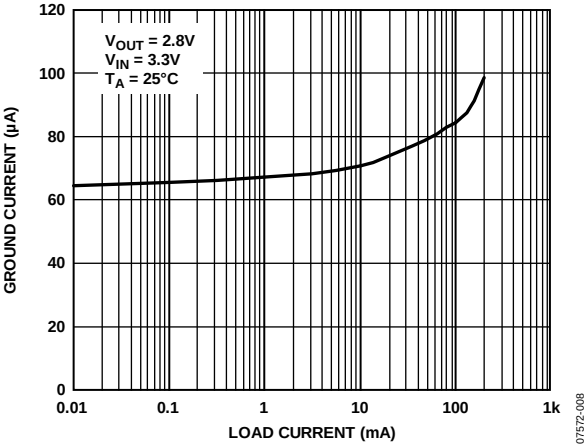

Figure 8. Ground Current vs. Load Current, Single Output Loaded

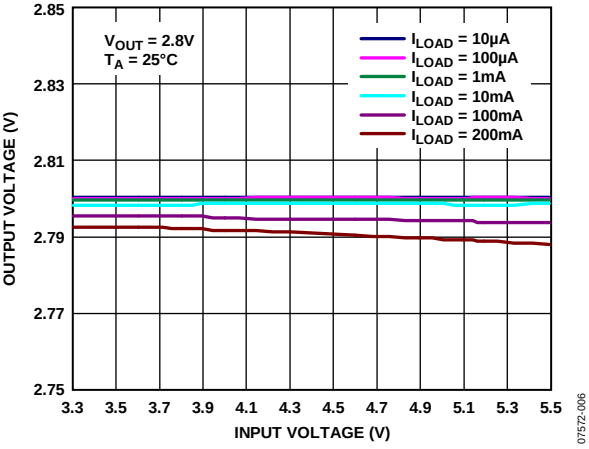

Figure 6. Output Voltage vs. Input Voltage

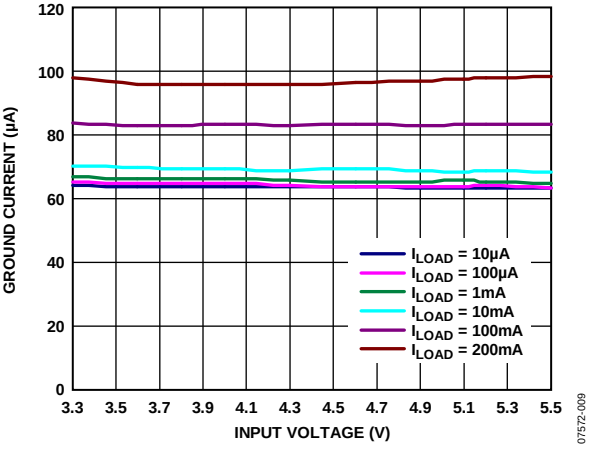

Figure 9. Ground Current vs. Input Voltage, Single Output Loaded

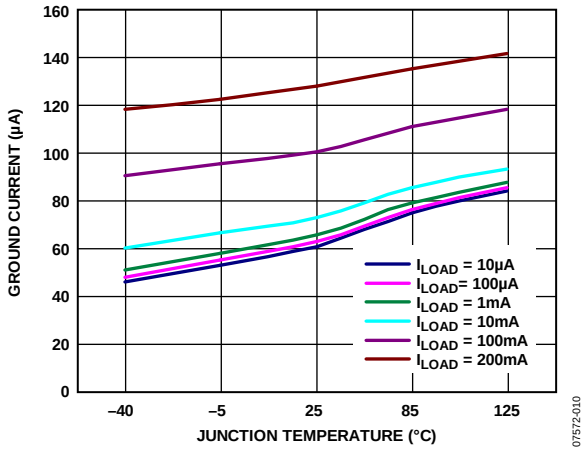

Figure 10. Ground Current vs. Junction Temperature, Both Outputs Loaded

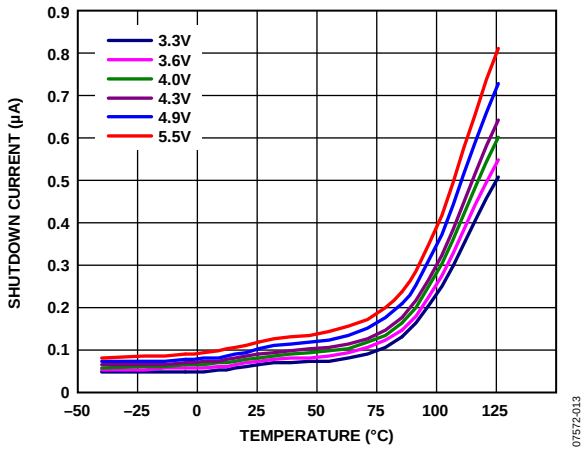

Figure 13. Shutdown Current vs. Temperature at Various Input Voltages

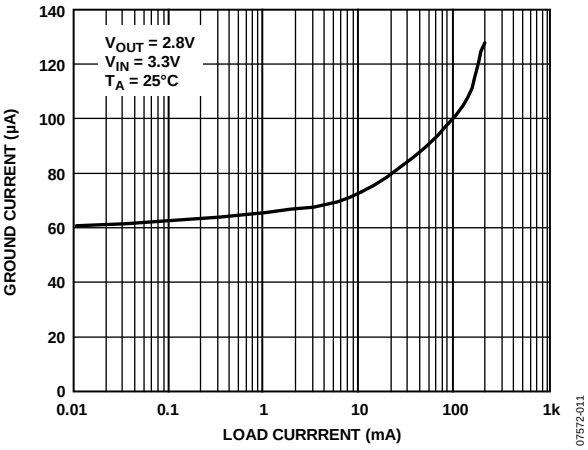

Figure 11. Ground Current vs. Load Current, Both Outputs Loaded

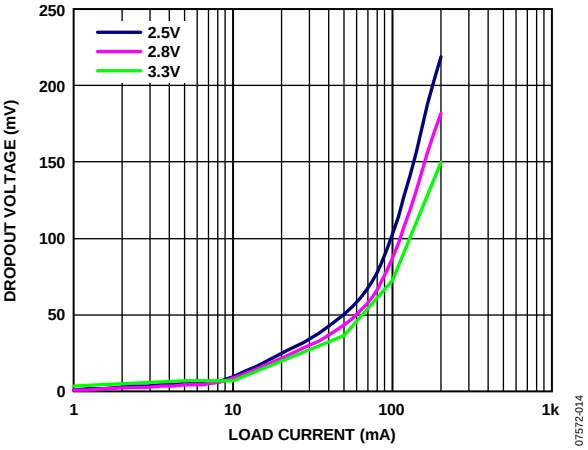

Figure 14. Dropout Voltage vs. Load Current and Output Voltage

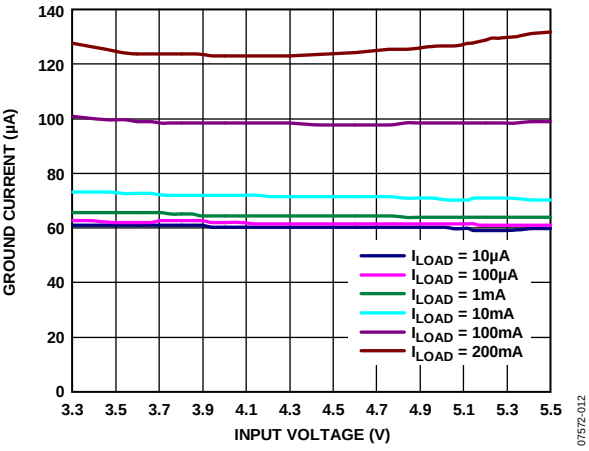

Figure 12. Ground Current vs. Input Voltage, Both Outputs Loaded

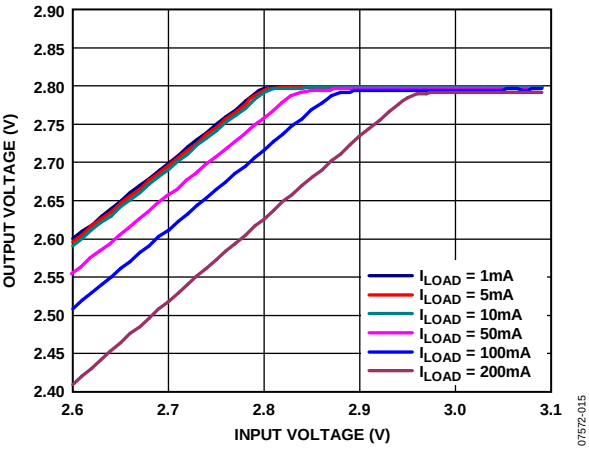

Figure 15. Output Voltage vs. Input Voltage (In Dropout)

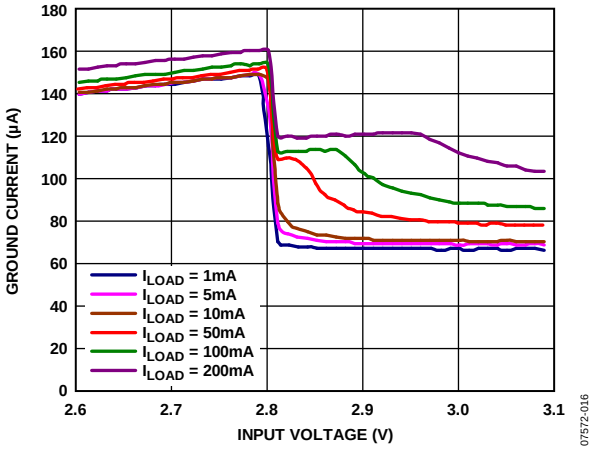

Figure 16. Ground Current vs. Input Voltage (In Dropout)

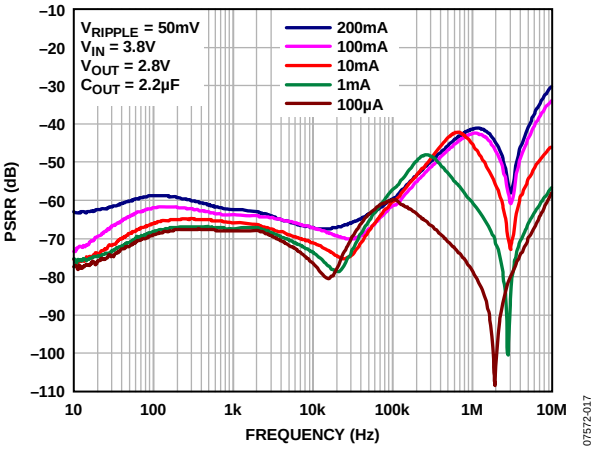

Figure 17. Power Supply Rejection Ratio vs. Frequency, 2.8 V

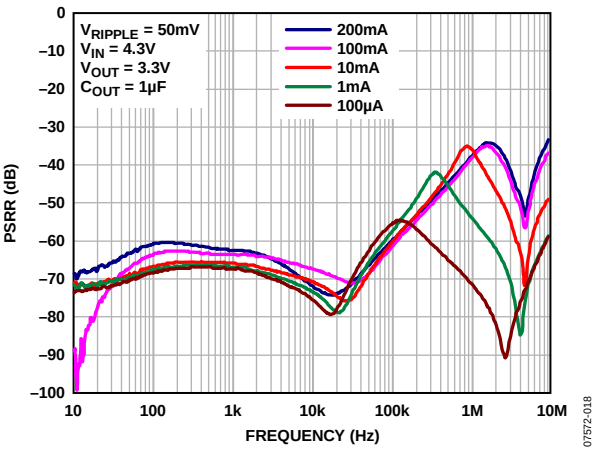

Figure 18. Power Supply Rejection Ratio vs. Frequency, 3.3 V

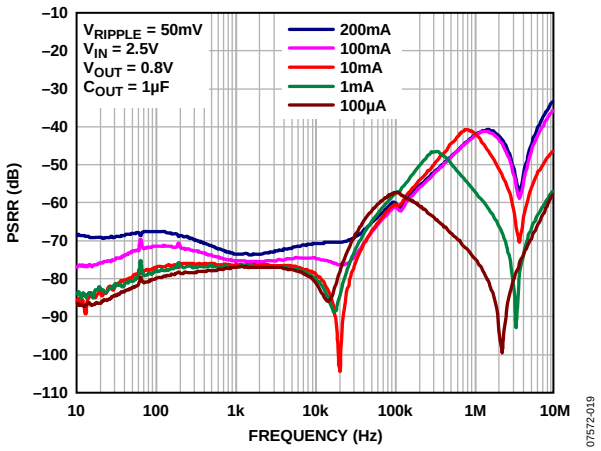

Figure 19. Power Supply Rejection Ratio vs. Frequency, 0.8 V

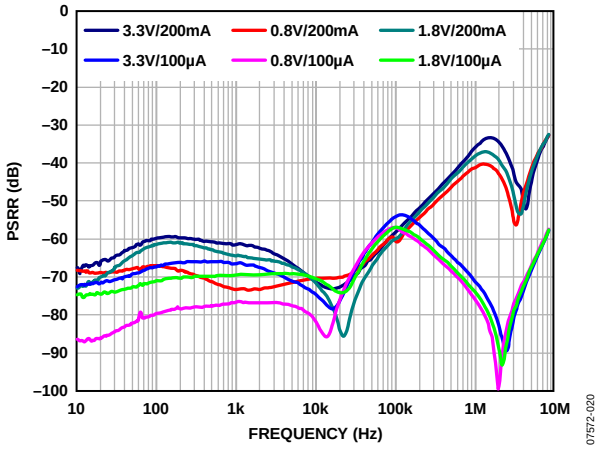

Figure 20. Power Supply Rejection Ratio vs. Frequency, at Various Output Voltages and Load Currents

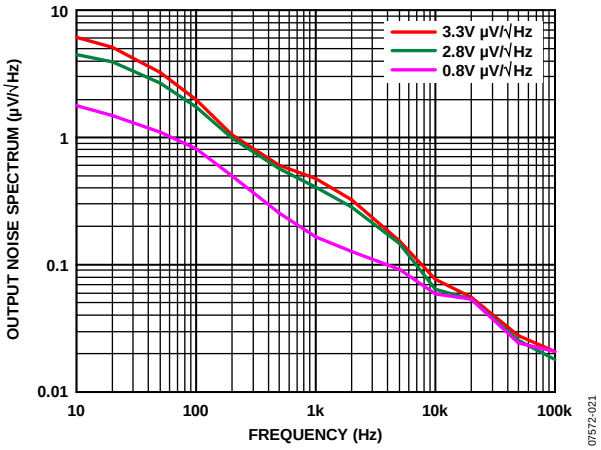

Figure 21. Output Noise Spectrum, V_{IN} = 5 V, I_{LOAD} = 10 mA

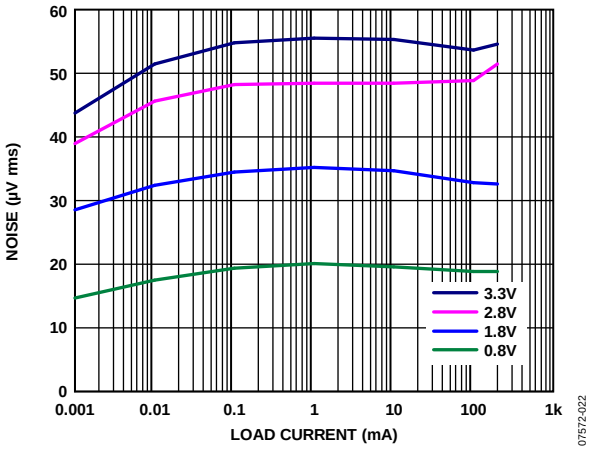

Figure 22. Output Noise vs. Load Current and Output Voltage, V_{IN} = 5 V

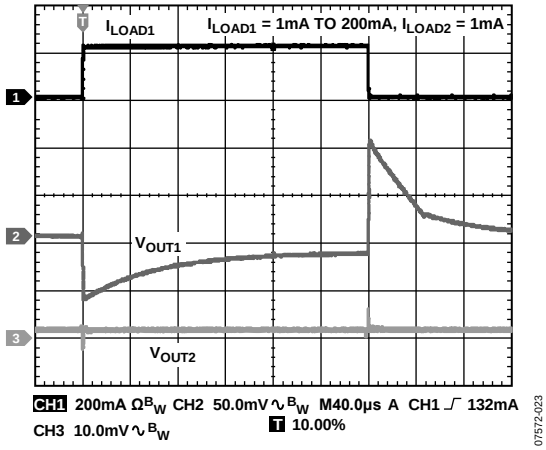

Figure 23. Load Transient Response,
I_{LOAD1} = 1 mA to 200 mA, I_{LOAD2} = 1 mA
CH1 = I_{LOAD1}, CH2 = V_{OUT1}, CH3 = V_{OUT2}

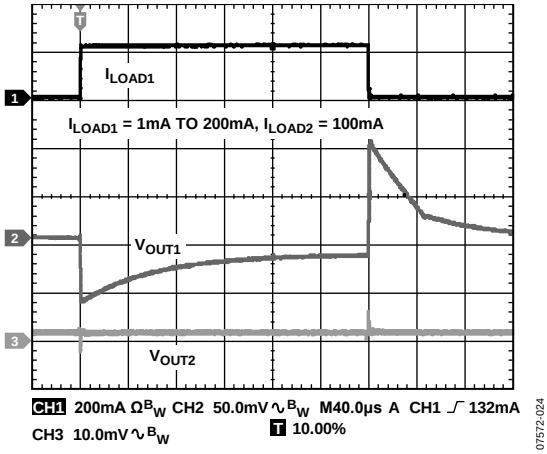

Figure 24. Load Transient Response,
I_{LOAD1} = 1 mA to 200 mA, I_{LOAD2} = 100 mA,
CH1 = I_{LOAD1}, CH2 = V_{OUT1}, CH3 = V_{OUT2}

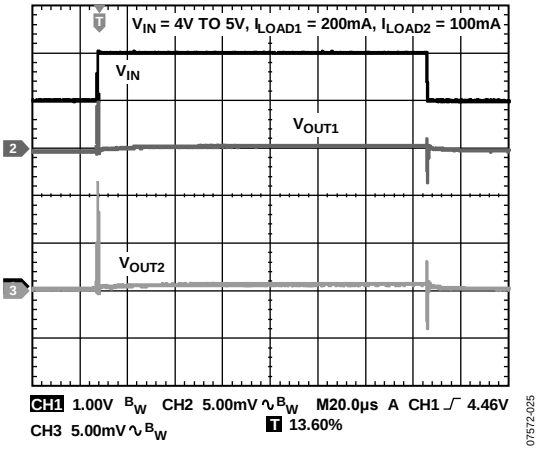

Figure 25. Line Transient Response,
V_{IN} = 4 V to 5 V, I_{LOAD1} = 200 mA, I_{LOAD2} = 100 mA
CH1 = V_{IN}, CH2 = V_{OUT1}, CH3 = V_{OUT2}

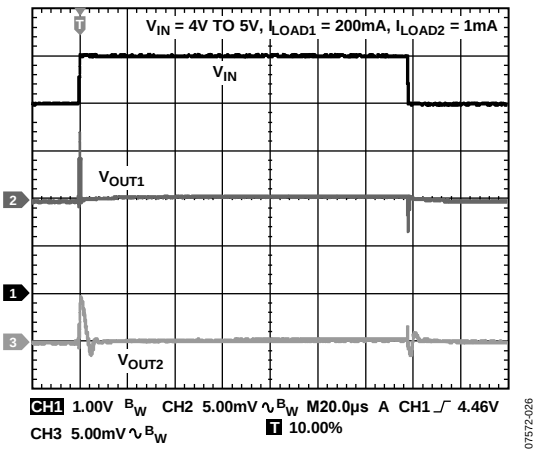

Figure 26. Line Transient Response
V_{IN} = 4 V to 5 V, I_{LOAD1} = 200 mA, I_{LOAD2} = 1 mA
CH1 = V_{IN}, CH2 = V_{OUT1}, CH3 = V_{OUT2}

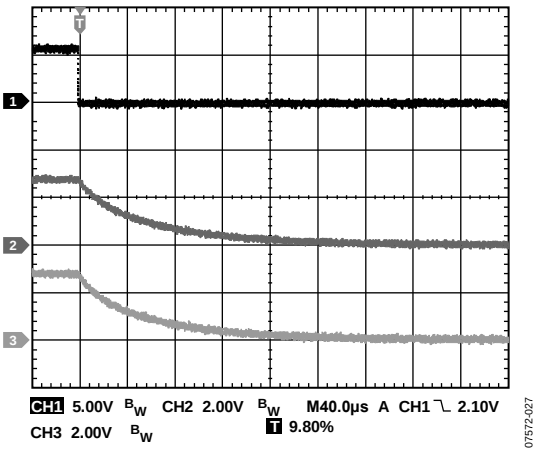

Figure 27. Shutdown Response, ADP221

THEORY OF OPERATION

The ADP220/ADP221 are low quiescent current, low dropout linear regulators that operate from 2.5 V to 5.5 V and provide up to 200 mA of current from each output. Drawing a low 120 µA quiescent current (typical) at full load makes the ADP220/ADP221 ideal for battery-operated portable equipment. Shutdown current consumption is typically 100 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP220/ADP221 provide excellent transient performance.

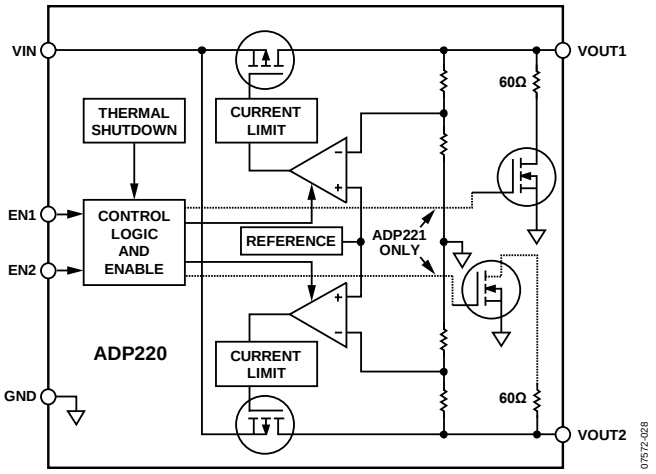

Figure 28. Internal Block Diagram

Internally, the ADP220/ADP221 consist of a reference, two error amplifiers, two feedback voltage dividers, and two PMOS pass transistors. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

The ADP221 also includes an active pull-down circuit to rapidly discharge the output load capacitance when each output is disabled.

The ADP220/ADP221 are available in multiple output voltage options ranging from 0.8 V to 3.3 V. The ADP220/ADP221 use the EN1/EN2 pins to enable and disable the VOUT1/VOUT2 pins under normal operating conditions. When EN1/EN2 are high, VOUT1/VOUT2 turn on; when EN1/EN2 are low, VOUT1/VOUT2 turn off. For automatic startup, EN1/EN2 can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP220/ADP221 are designed for operation with small, space-saving ceramic capacitors, but the parts function with most commonly used capacitors as long as care is taken with regards to the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP220/ADP221. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP220/ADP221 to large changes in the load current. Figure 29 and Figure 30 show the transient responses for output capacitance values of 1 µF and 4.7 µF, respectively.

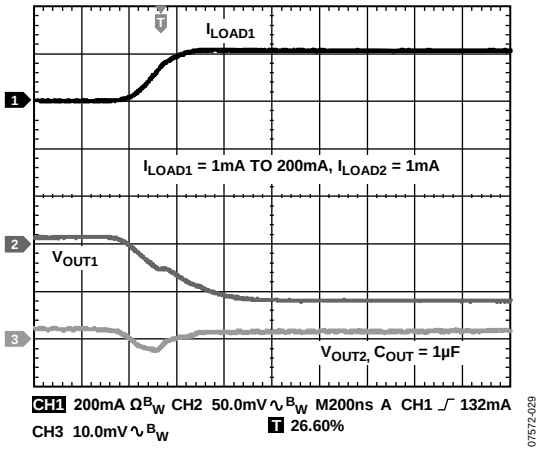

Figure 29. Output Transient Response
I_{LOAD1} = 1 mA to 200 mA, I_{LOAD2} = 1 mA
CH1 = I_{LOAD1}, CH2 = V_{OUT1}, CH3 = V_{OUT2}, C_{OUT} = 1 µF

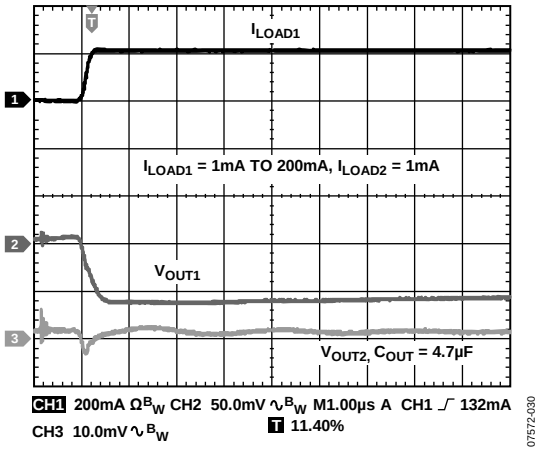

Figure 30. Output Transient Response
I_{LOAD1} = 1 mA to 200 mA, I_{LOAD2} = 1 mA
CH1 = I_{LOAD1}, CH2 = V_{OUT1}, CH3 = V_{OUT2}, C_{OUT} = 4.7 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If an output capacitance greater than 1 µF is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADP220/ADP221, as long as the capacitor meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have an adequate dielectric to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 31 depicts the capacitance vs. voltage bias characteristic of an 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of the package or voltage rating.

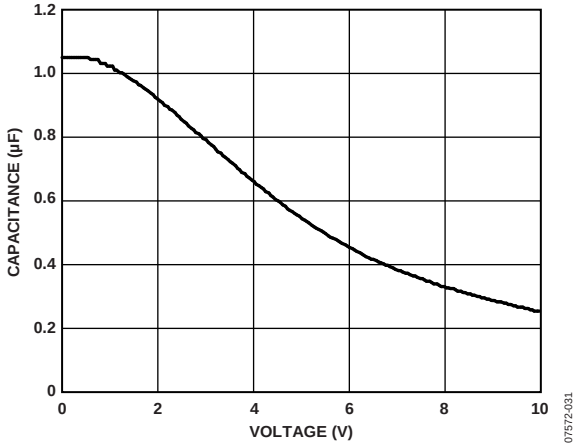

Figure 31. Capacitance vs. Voltage Bias Characteristic

Equation 1 can be used to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, TEMPCO over −40°C to +85°C is assumed to be 15% for an X5R dielectric. TOL is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V from the graph in Figure 31.

Substituting these values into Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP220/ADP221, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP220/ADP221 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 2.2 V. This ensures that the inputs of the ADP220/ADP221 and the output behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP220/ADP221 use the ENx pins to enable and disable the VOUTx pins under normal operating conditions. Figure 32 shows a rising voltage on ENx crossing the active threshold, then V_{OUTx} turns on. When a falling voltage on ENx crosses the inactive threshold, V_{OUTx} turns off.

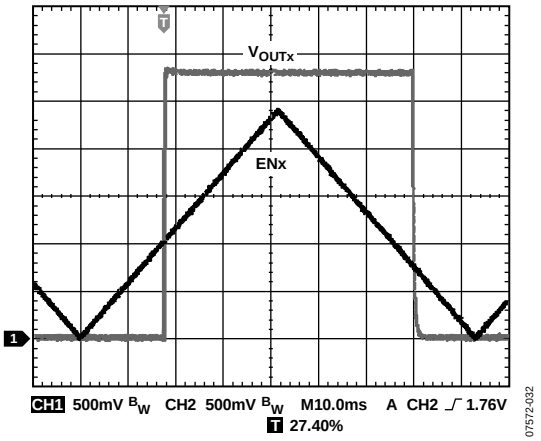

Figure 32. Typical ENx Pin Operation

As shown in Figure 32, the ENx pins have built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the ENx pins as it passes through the threshold points.

The active/inactive thresholds of the ENx pins are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 33 shows typical ENx active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

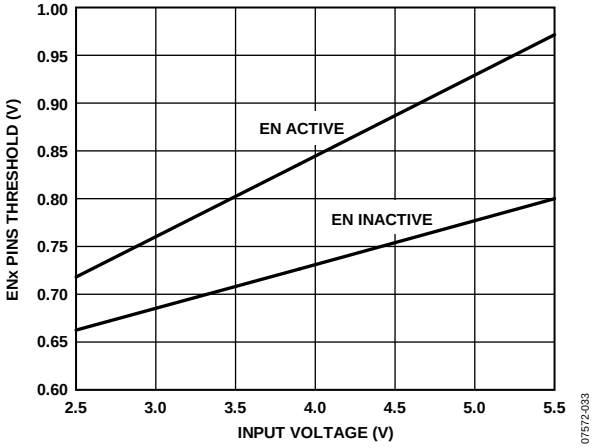

Figure 33. Typical ENx Pins Thresholds vs. Input Voltage

The ADP220/ADP221 utilize an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 2.8 V option is approximately 220 µs from the time the ENx active threshold is crossed to when the output reaches 90% of its final value. The start-up time is somewhat dependent on the output voltage setting and increases slightly as the output voltage increases.

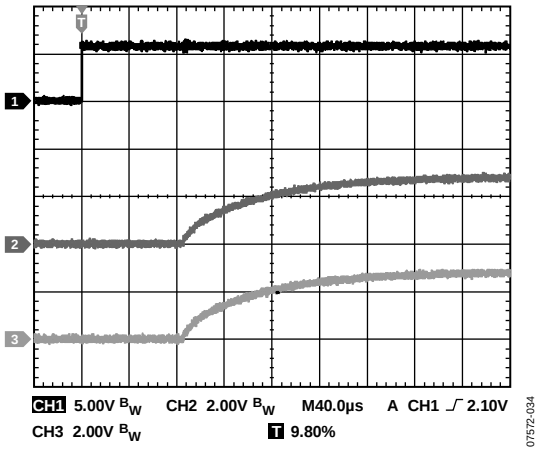

Figure 34. Typical Start-Up Time

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP220/ADP221 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP220/ADP221 are designed to current limit when the output load reaches 300 mA (typical). When the output load exceeds 300 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is built-in, which limits the junction temperature to a maximum of 155°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 155°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 140°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUTx to GND occurs. At first, the ADP220/ADP221 current limit, so that only 300 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 155°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 140°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 155°C. This thermal oscillation between 140°C and 155°C causes a current oscillation between 0 mA and 300 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

In most applications, the ADP220/ADP221 do not dissipate much heat due to high efficiency. However, in applications with a high ambient temperature and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 155°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 140°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP220/ADP221 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered on the PCB. Table 6 shows typical θ_{JA} values for the ADP220/ADP221 for various PCB copper sizes.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	ADP220/ADP221 (°C/W)
0[1]	200
50	119
100	118
300	115
500	113

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP220/ADP221 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = \Sigma[(V_{IN} - V_{OUT}) \times I_{LOAD}] + \Sigma(V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_A + \{\Sigma[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. Figure 35 to Figure 39 show junction temperature calculations for different ambient temperatures, total power dissipation, and areas of PCB copper.

In cases where the board temperature is known, the thermal characterization parameter, Ψ_{JB}, can be used to estimate the junction temperature rise. T_J is calculated from T_B and P_D using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical Ψ_{JB} value for the 6-ball WLCSP is 43.8°C/W.

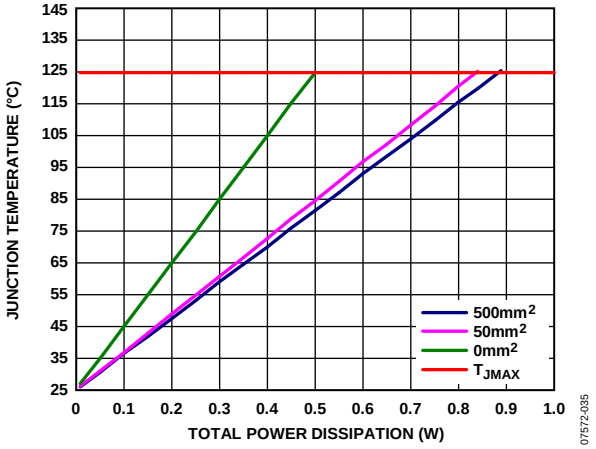

Figure 35. Junction Temperature vs. Total Power Dissipation, T_A = 25°C

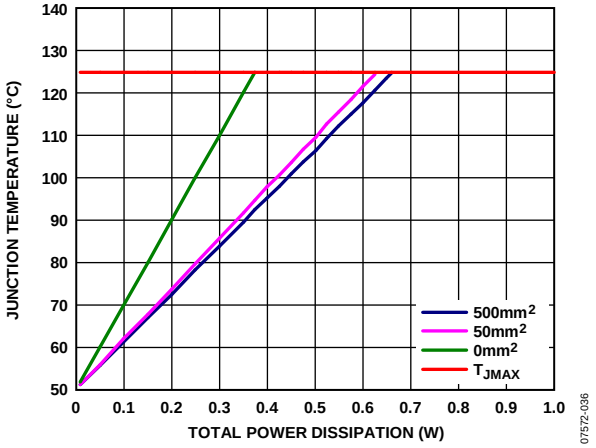

Figure 36. Junction Temperature vs. Total Power Dissipation, T_A = 50°C

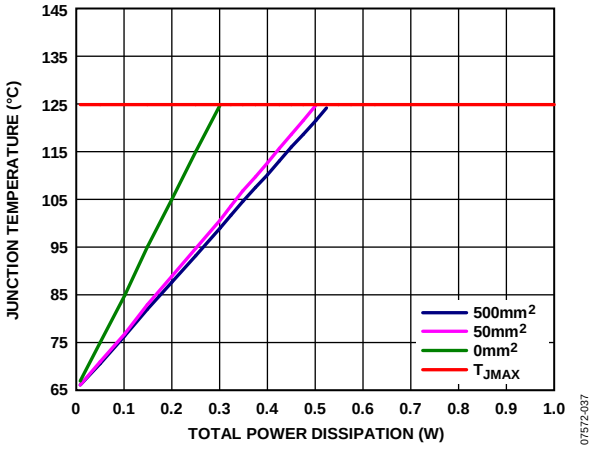

Figure 37. Junction Temperature vs. Total Power Dissipation, T_A = 65°C

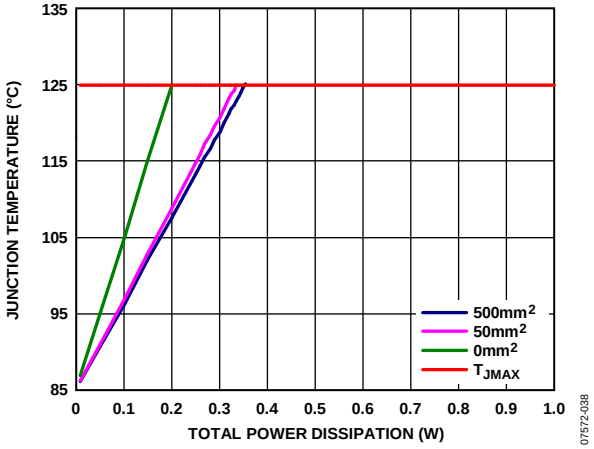

Figure 38. Junction Temperature vs. Total Power Dissipation, T_A = 85°C

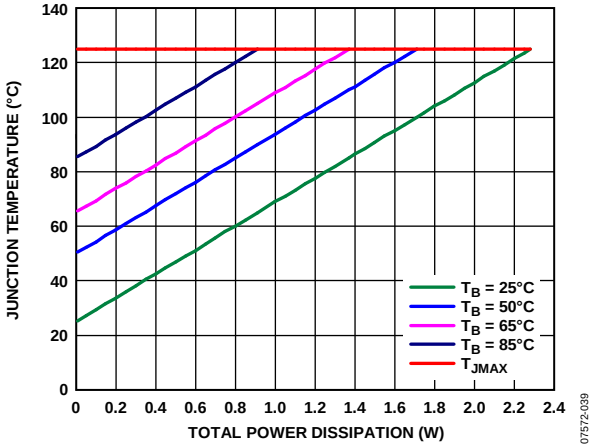

Figure 39. Junction Temperature vs. Total Power Dissipation and Board Temperature

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP220/ADP221. However, as shown in Table 6, a point of diminishing returns eventually is reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitors as close as possible to the VOUT1, VOUT2, and GND pins. Use 0402 or 0603 size capacitors and resistors to achieve the smallest possible footprint solution on boards where area is limited.

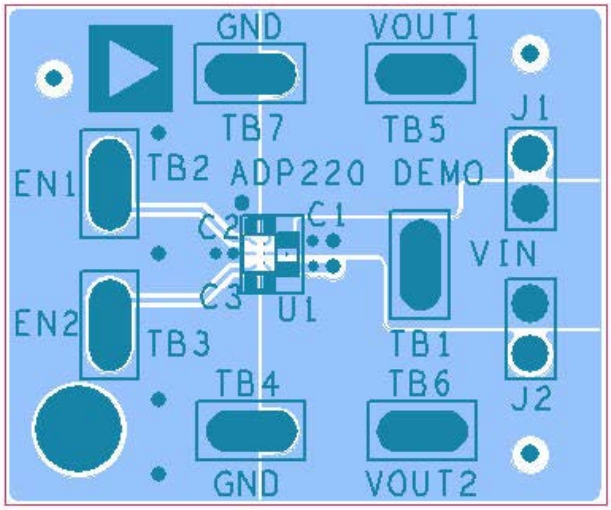

Figure 40. Example of PCB Layout, Top Side

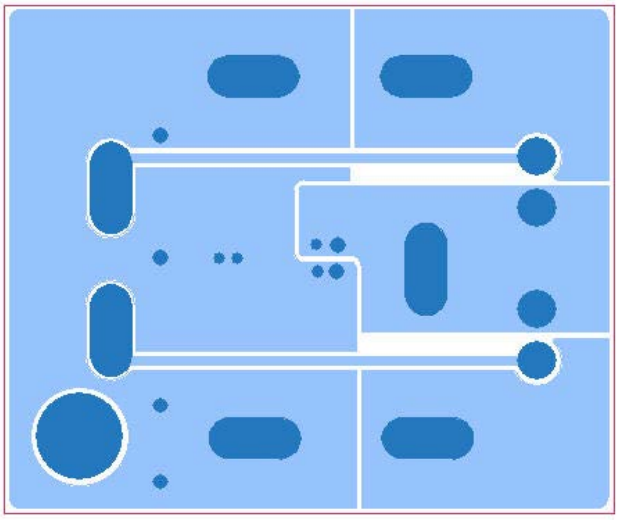

Figure 41. Example of PCB Layout, Bottom Side

OUTLINE DIMENSIONS

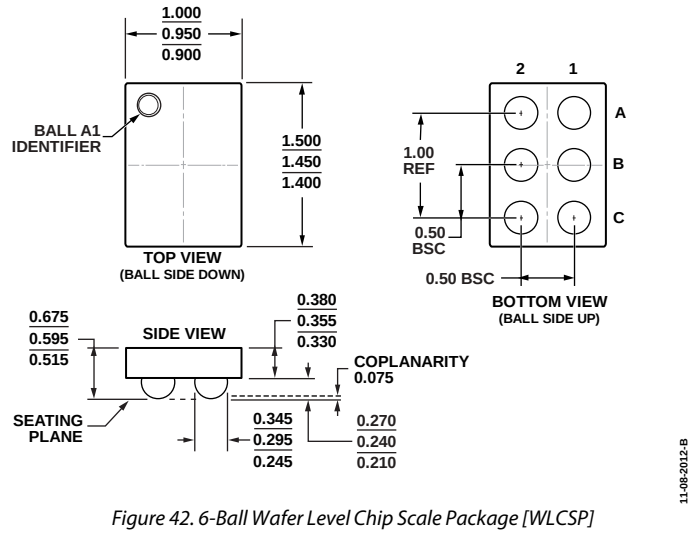

Figure 42. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-2)
Dimensions show in millimeters

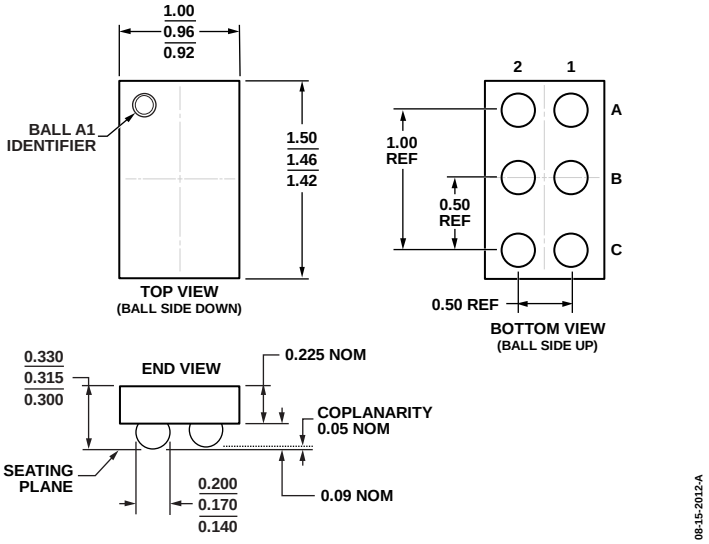

Figure 43. 6-Ball Bumped Bare Die Sales [BUMPED_CHIP]
(CD-6-7)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	V_{OUT1}/V_{OUT2} Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP220ACBZ-1118R7	−40°C to +125°C	1.1/1.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LFY
ADP220ACBZ-1812R7	−40°C to +125°C	1.8/1.2	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LEK
ADP220ACBZ-1827R7	−40°C to +125°C	1.8/2.7	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LEH
ADP220ACBZ-2623R7	−40°C to +125°C	2.6/2.3	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LGD
ADP220ACBZ-26235R7	−40°C to +125°C	2.6/2.35	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	L9L
ADP220ACBZ-2812R7	−40°C to +125°C	2.8/1.2	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	L8W
ADP220ACBZ-2818R7	−40°C to +125°C	2.8/1.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LEL
ADP220ACBZ-2827R7	−40°C to +125°C	2.8/2.7	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	L8X
ADP220ACBZ-2828R7	−40°C to +125°C	2.8/2.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	L8Y
ADP220ACBZ275275R7	−40°C to +125°C	2.75/2.75	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	L8Z
ADP220ACBZ-3033R7	−40°C to +125°C	3.0/3.3	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LH4
ADP220ACBZ-1212R7	−40°C to +125°C	1.2/1.2	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LLT
ADP220ACBZ-2525R7	−40°C to +125°C	2.5/2.5	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LLU
ADP221ACBZ2828-R7	−40°C to +125°C	2.8/2.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	L90
ADP221ACBZ-1818-R7	−40°C to +125°C	1.8/1.8	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	LJ0
ADP221ACDZ-1818-R7	−40°C to +125°C	1.8/1.8	6-Ball Bumped Bare Die Sales [Bump Chip]	CD-6-7	LJ0
ADP220-2828-EVALZ	−40°C to +125°C	2.8/2.8	2.8 V/2.8 V Evaluation Board		
ADP221-2828-EVALZ	−40°C to +125°C	2.8/2.8	2.8 V/2.8 V with Output Discharge Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local Analog Devices sales or distribution representative.

NOTES

NOTES

D07572-0-1/13(H)

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