CY7C1041GN

4-Mbit (256K words × 16 bit) Static RAM

Features

- High speed
  - t_{AA} = 10 ns / 15 ns
- Low active and standby currents
  - Active current: I_{CC} = 38-mA typical
  - Standby current: I_{SB2} = 6-mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 44-pin SOJ, 44-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1041GN is high-performance CMOS fast static RAM Organized as 256K words by 16-bits.

Data writes are performed by asserting the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW, while providing the data on I/O_0 through I/O_{15} and address on A_0 through A_{17} pins. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control write operations to the upper and lower bytes of the specified memory location. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

Data reads are performed by asserting the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state during the following events:

- The device is deselected ($\overline{CE}$ HIGH)
- The control signals ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$) are de-asserted

The logic block diagram is on page 2.

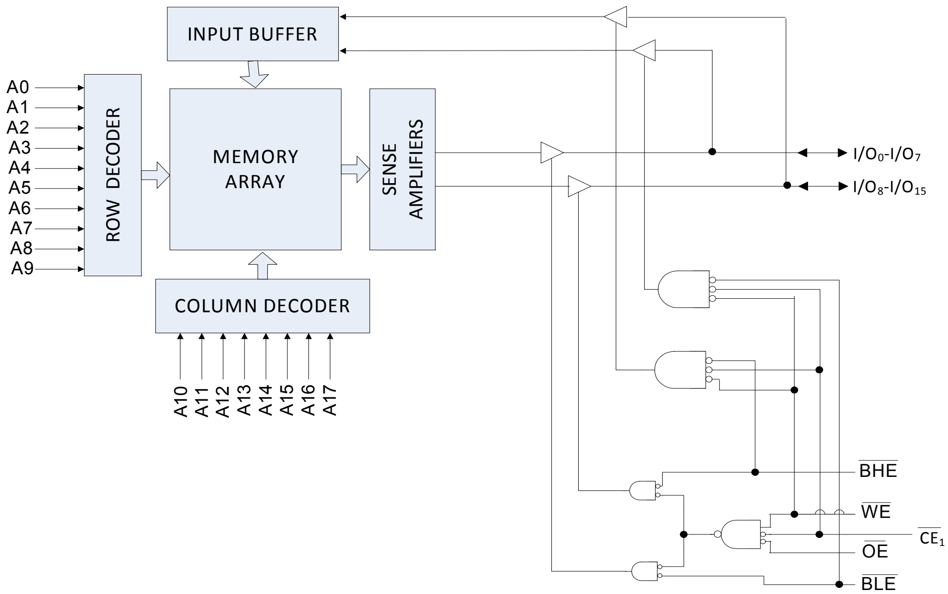
Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns) 10/15	Power Dissipation			
				Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
				Typ [1]	Max	Typ [1]	Max
CY7C1041GN18	Industrial	1.65 V–2.2 V	15	–	40	6	8
CY7C1041GN30		2.2 V–3.6 V	10	38	45		
CY7C1041GN		4.5 V–5.5 V	10	38	45		

Notes

1. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1041GN



Contents

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Package/Grade ID: BVXI [2, 3]

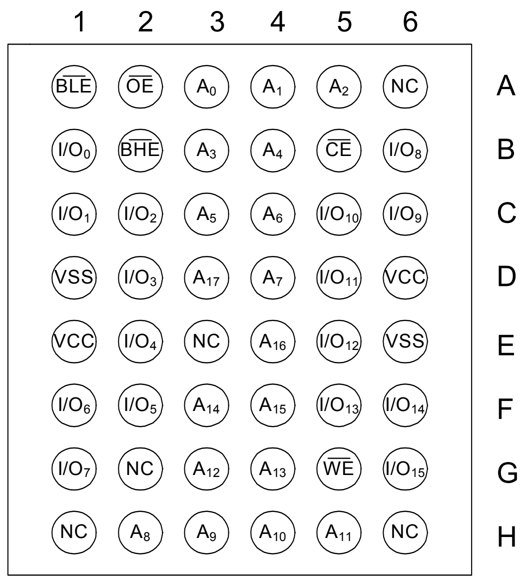


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Package/Grade ID: BVJXI [2]

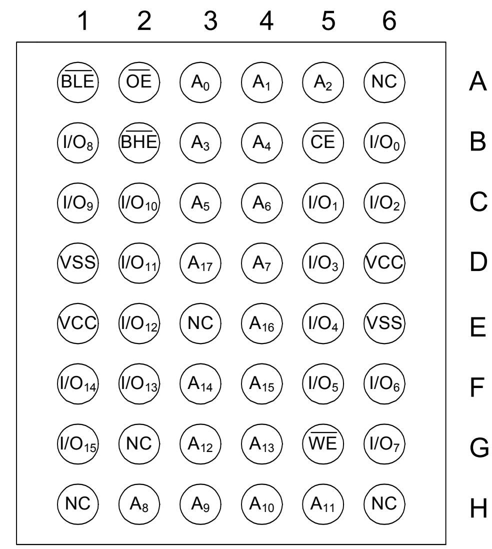
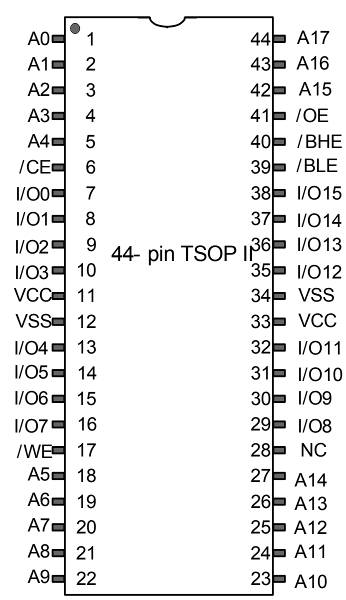


Figure 3. 44-pin TSOP II / 44-pin SOJ pinout [2]



Notes

2. NC pins are not connected internally to the die.
3. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O$_{[7:0]}$ and I/O$_{[15:8]}$ balls are swapped.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [4] .... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in HI-Z State [4] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage [4] .... –0.5 V to V_{CC} + 0.5 V

Current into outputs (in LOW state) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions	10 ns / 15 ns			Unit
				Min	Typ[5]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA	1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA	2	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA	V_{CC} – 0.5[6]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA	–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA	–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–	1.4	–	V_{CC} + 0.2[4]	V
		2.2 V to 2.7 V	–	2	–	V_{CC} + 0.3[4]	
		2.7 V to 3.6 V	–	2	–	V_{CC} + 0.3[4]	
		4.5 V to 5.5 V	–	2.2	–	V_{CC} + 0.5[4]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	–	–0.2[4]	–	0.4	V
		2.2 V to 2.7 V	–	–0.3[4]	–	0.6	
		2.7 V to 3.6 V	–	–0.3[4]	–	0.8	
		4.5 V to 5.5 V	–	–0.5[4]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}	–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	–	+1	µA
I_{CC}	Operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels; f = 100 MHz	–	38	45	mA
			f = 66.7 MHz	–	–	40	
I_{SB1}	Automatic CE power-down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	–	15	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0	–	6	8	mA

Notes

4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
6. This parameter is guaranteed by design and not tested.

Capacitance

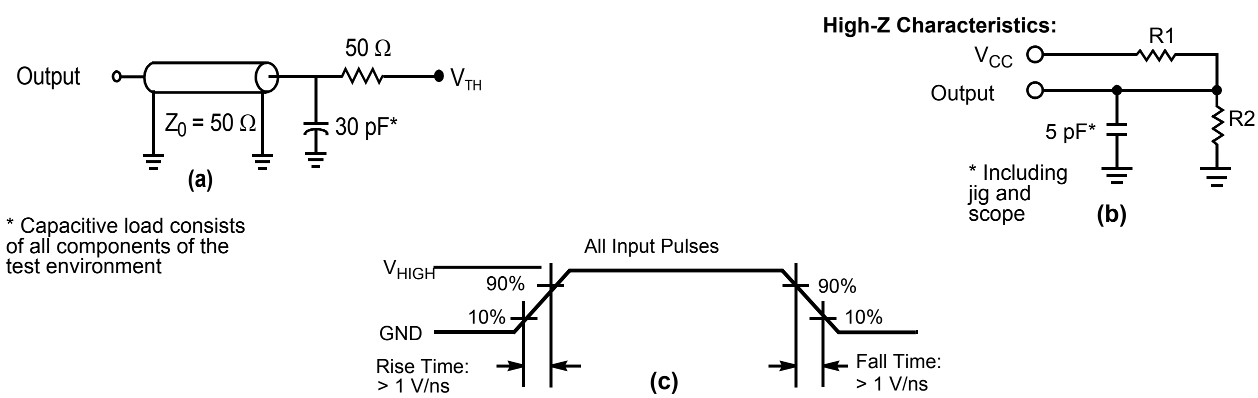
Parameter [7]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	10	10	pF
C_{OUT}	I/O capacitance		10	10	10	pF

Thermal Resistance

Parameter [7]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.35	55.37	68.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.74	30.41	15.97	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [8]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device AC operation assumes a 100-μs ramp time from 0 to $V_{CC(min)}$ and a 100-μs wait time after V_{CC} stabilization.

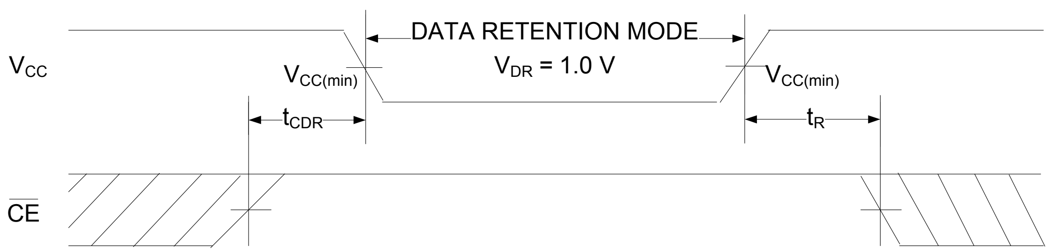
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.2 V, $\overline{CE} \geq V_{CC} - 0.2$ V[9], $V_{IN} \geq V_{CC} - 0.2$ V, or $V_{IN} \leq 0.2$ V	–	8	mA
t_{CDR}[10]	Chip deselect to data retention time		0	–	ns
t_R[9, 10]	Operation recovery time	$V_{CC} \geq 2.2$ V	10	–	ns
		$V_{CC} < 2.2$ V	15	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform [9]



Notes

9. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC\ (min)} \geq 100$ µs.
10. These parameters are guaranteed by design.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [11]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	15	–	ns
t_{AA}	Address to data	–	10	–	15	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data [12]	–	10	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data	–	4.5	–	8	ns
t_{LZOE}	$\overline{OE}$ LOW to low impedance [13, 14]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z [13, 14]	–	5	–	8	ns
t_{LZCE}	$\overline{CE}$ LOW to low impedance [12, 13, 14]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to HI-Z [12, 13, 14]	–	5	–	8	ns
t_{PU}	$\overline{CE}$ LOW to power-up [12, 14, 15]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [12, 14, 15]	–	10	–	15	ns
t_{DBE}	Byte enable to data valid	–	4.5	–	8	ns
t_{LZBE}	Byte enable to low impedance [14]	0	–	0	–	ns
t_{HZBE}	Byte disable to HI-Z [14]	–	6	–	8	ns
Write Cycle [15, 16]						
t_{WC}	Write cycle time	10	–	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [12]	7	–	12	–	ns
t_{AW}	Address setup to write end	7	–	12	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	12	–	ns
t_{SD}	Data setup to write end	5	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low impedance [13, 14]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z [13, 14]	–	5	–	8	ns
t_{BW}	Byte Enable to write end	7	–	12	–	ns

Notes

11. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 4 on page 6, unless specified otherwise.
12. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
13. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 4 on page 6. Transition is measured ±200 mV from steady state voltage.
14. These parameters are guaranteed by design and are not tested.
15. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write cycle pulse width in Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [17, 18]

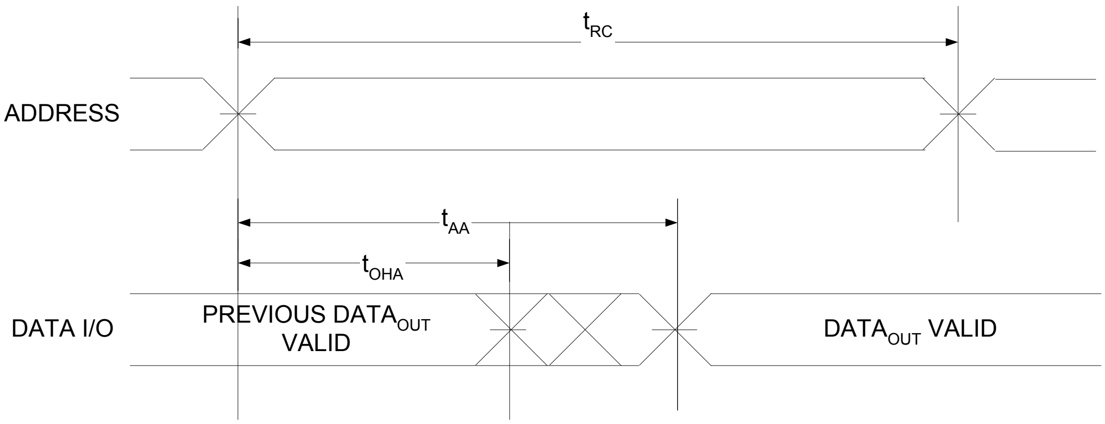
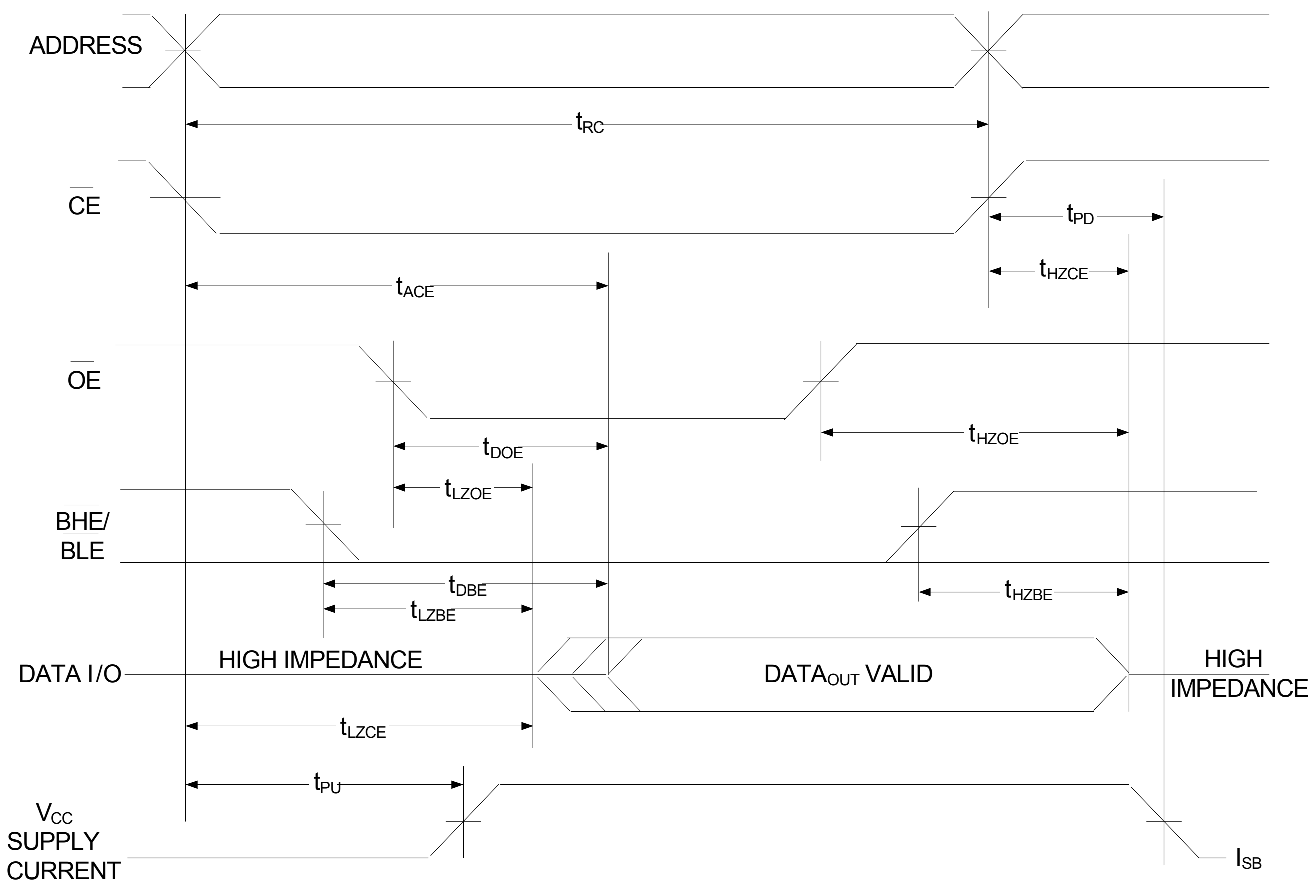


Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [18, 19]



Notes

17. The device is continuously selected, $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
18. $\overline{WE}$ is HIGH for the read cycle.
19. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{CE}$ Controlled) [20, 21]

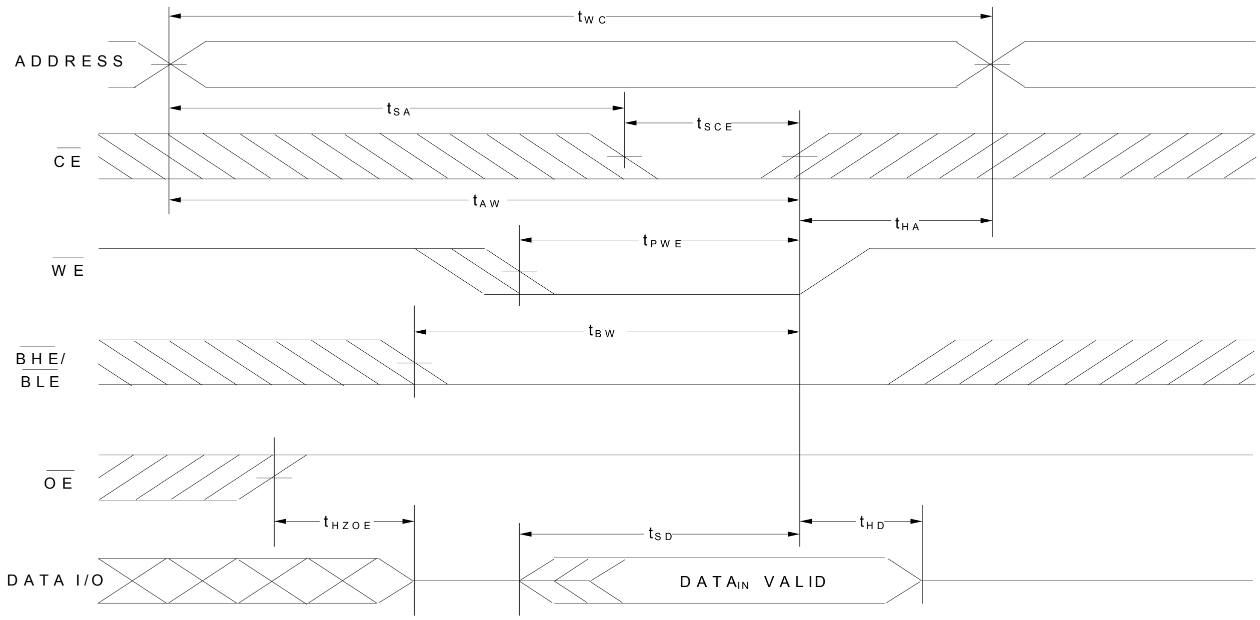
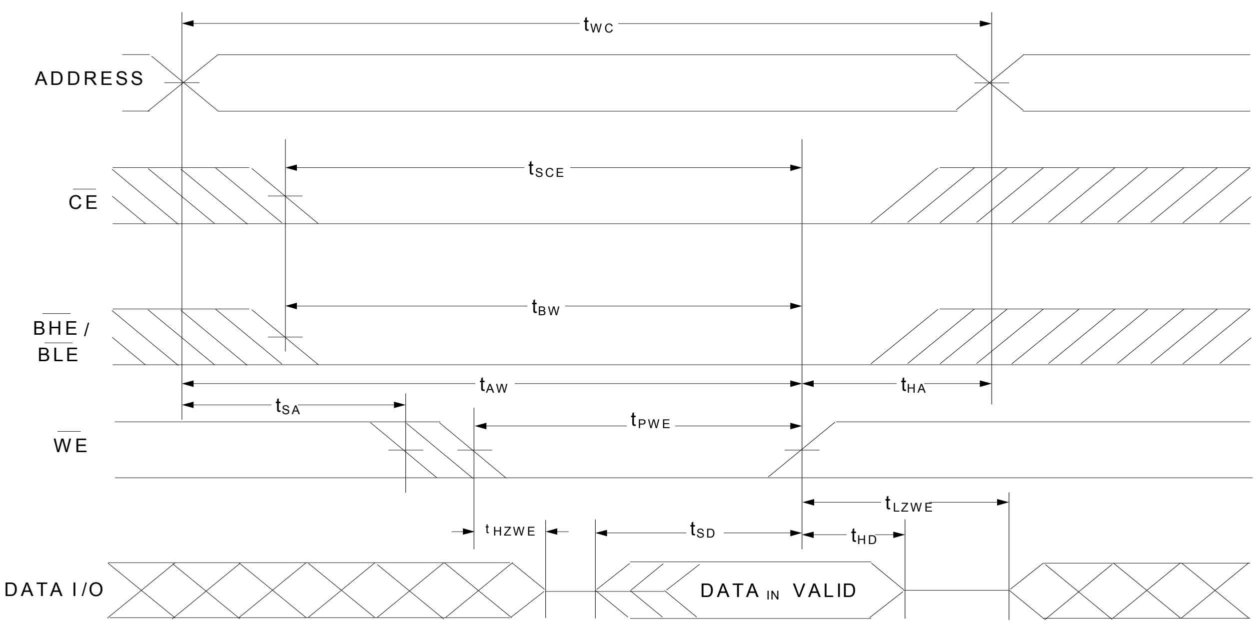


Figure 9. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [20, 21, 22]



Notes

20. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
22. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms (continued)

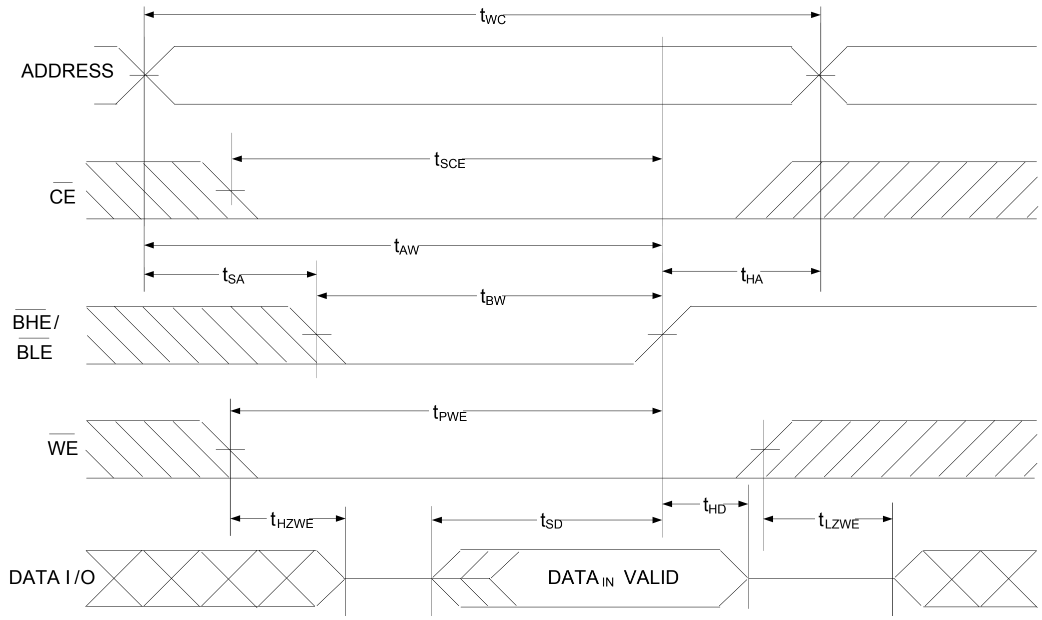


Figure 10. Write Cycle No. 3 (BLE or BHE Controlled) [23, 24]

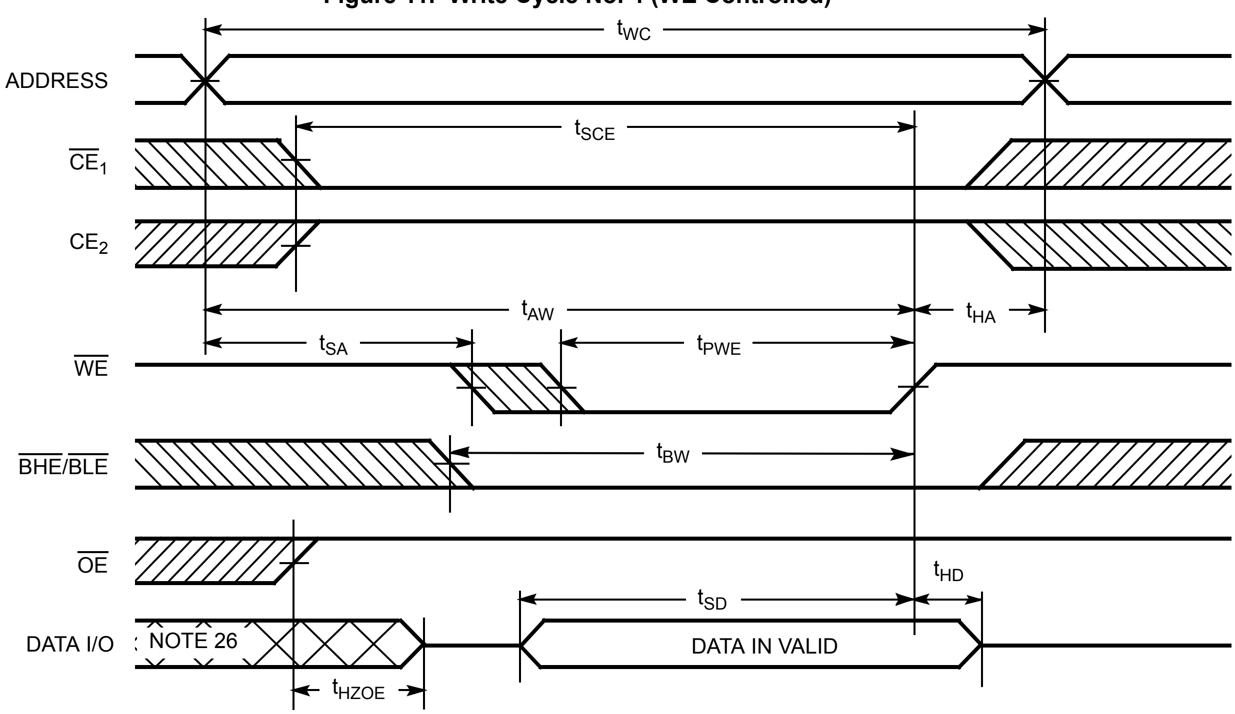


Figure 11. Write Cycle No. 4 (WE Controlled) [23, 24, 25]

Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
25. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
26. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

CE	OE	WE	BLE	BHE	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X[27]	X[27]	X[27]	X[27]	HI-Z	HI-Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I_{CC})

Notes

27. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1041GN30-10ZSXI	51-85087	44-pin TSOP II	Industrial
		CY7C1041GN30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7C1041GN30-10BVJXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC Compatible	
	4.5 V–5.5 V	CY7C1041GN-10ZSXI		44-pin TSOP II	

Ordering Code Definitions

CY 7 C 1 04 1 GN XX - XX XX X I

Temperature Range: I = Industrial

Pb-free

Package Type: XX = ZS or BV or BVJ
ZS = 44-pin TSOP II; BV = 48-ball VFBGA;
BVJ = 48-ball VFBGA JEDEC Compatible

Speed: XX = 10 ns

Voltage Range:
30 = 2.2 V–3.6 V

Process Technology: Revision Code “GN” = 65 nm

Data Width: 1 = × 16-bits

Density: 04 = 4-Mbit

Family Code: 1 = Fast Asynchronous SRAM family

Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

Package Diagrams

Figure 12. 44-pin TSOP II (Z44) Package Outline, 51-85087

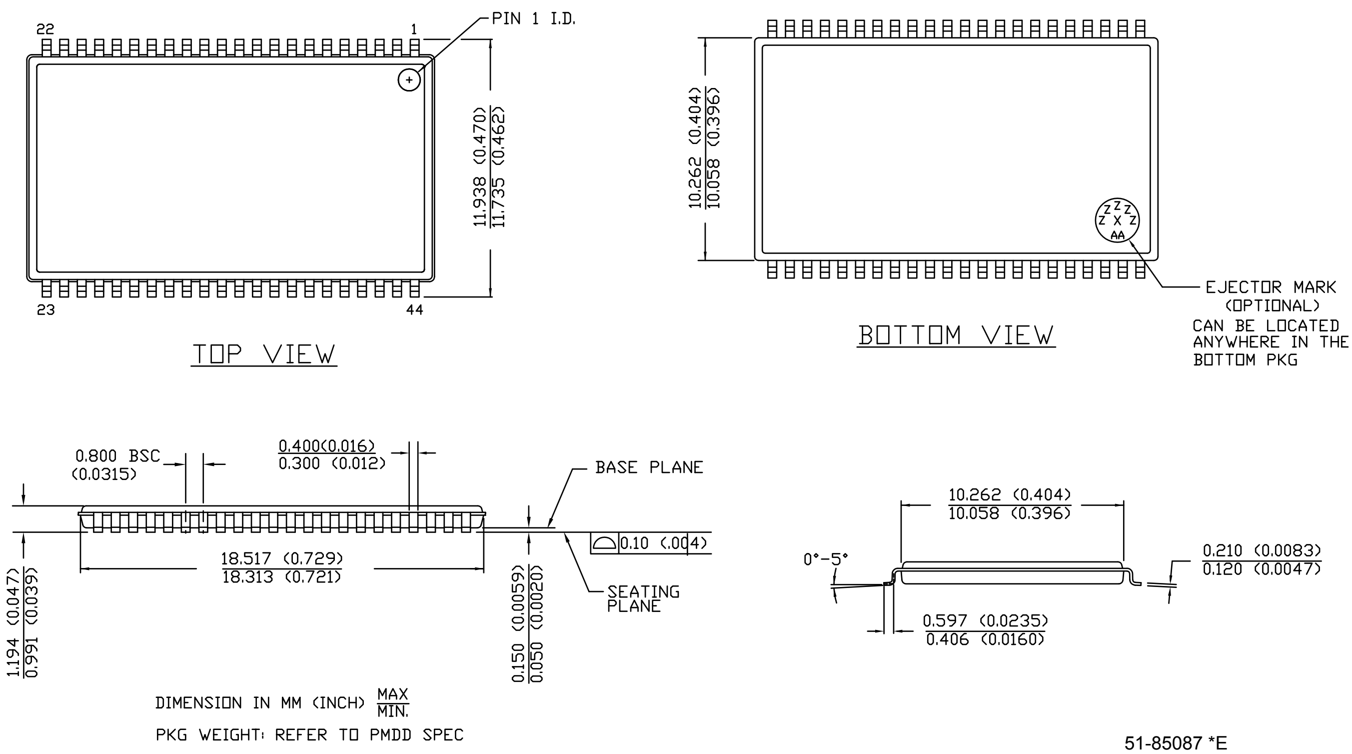
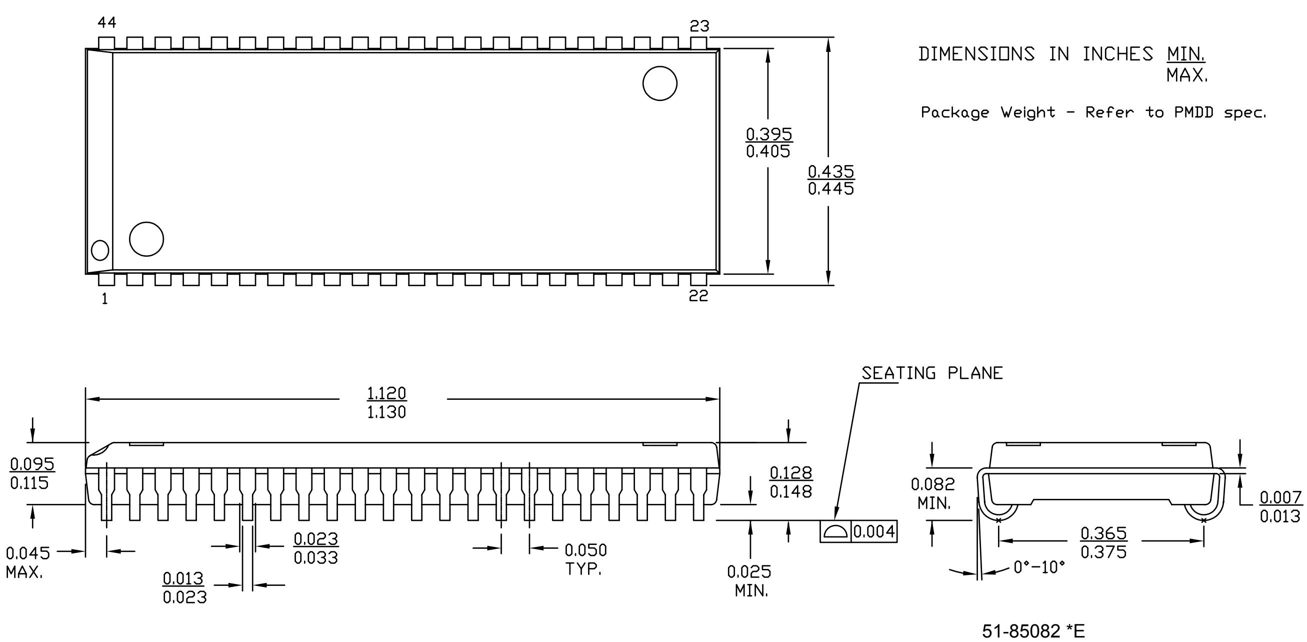
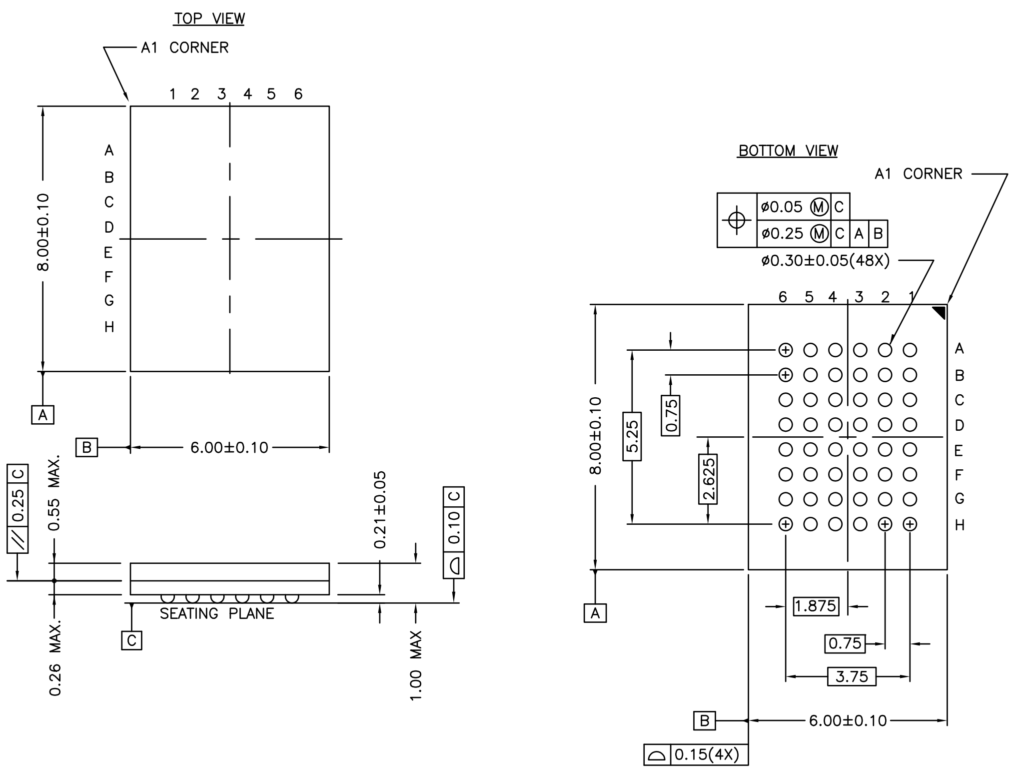


Figure 13. 44-pin SOJ (400 Mils) Package Outline, 51-85082



Package Diagrams (continued)

Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random-access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	5074414	NILE	01/06/2016	New data sheet.
*A	5082573	NILE	01/12/2016	Updated Logic Block Diagram – CY7C1041GN. Updated Ordering Information: Updated part numbers.
*B	5120171	VINI	02/01/2016	Updated Logic Block Diagram – CY7C1041GN.

Document Title: CY7C1041GN, 4-Mbit (256K words × 16 bit) Static RAM
Document Number: 001-95413

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