

**4-Mbit (256K words × 16 bit) Static RAM**

**Features**

- High speed
  - $t_{AA} = 10 \text{ ns} / 15 \text{ ns}$
- Low active and standby currents
  - Active current:  $I_{CC} = 38\text{-mA}$  typical
  - Standby current:  $I_{SB2} = 6\text{-mA}$  typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 44-pin SOJ, 44-pin TSOP II, and 48-ball VFBGA packages

**Functional Description**

CY7C1041GN is high-performance CMOS fast static RAM Organized as 256K words by 16-bits.

Data writes are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>15</sub> and address on A<sub>0</sub> through A<sub>17</sub> pins. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control write operations to the upper and lower bytes of the specified memory location.  $\overline{BHE}$  controls I/O<sub>8</sub> through I/O<sub>15</sub> and  $\overline{BLE}$  controls I/O<sub>0</sub> through I/O<sub>7</sub>.

Data reads are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). Byte accesses can be performed by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state during the following events:

- The device is deselected ( $\overline{CE}$  HIGH)
- The control signals ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ) are de-asserted

The logic block diagram is on page 2.

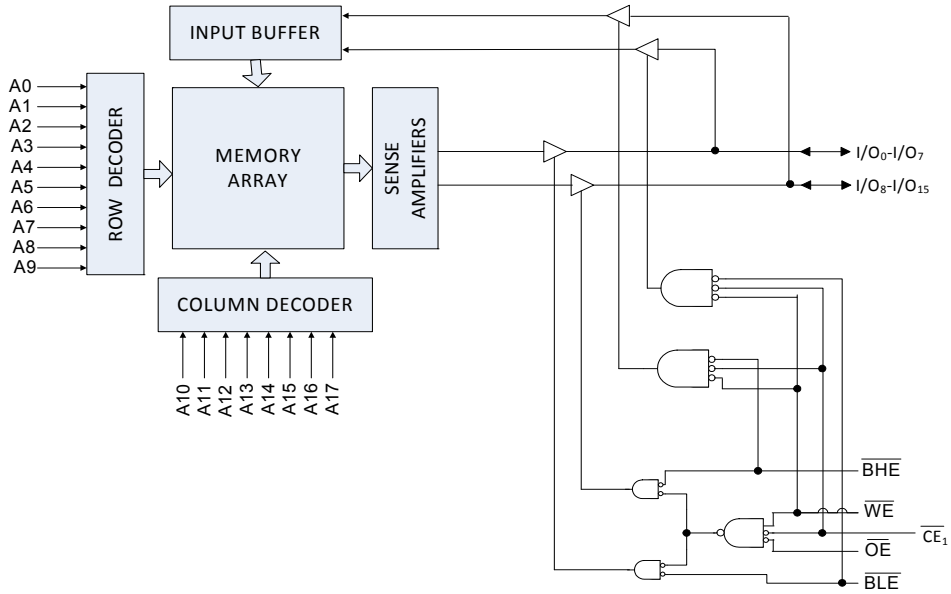
**Product Portfolio**

Product	Range	V <sub>CC</sub> Range (V)	Speed (ns) 10/15	Power Dissipation			
				Operating I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (mA)	
				f = f <sub>max</sub>			
				Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY7C1041GN18	Industrial	1.65 V–2.2 V	15	–	40	6	8
CY7C1041GN30		2.2 V–3.6 V	10	38	45		
CY7C1041GN		4.5 V–5.5 V	10	38	45		

**Notes**

1. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for a V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

Logic Block Diagram – CY7C1041GN



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### Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Package/Grade ID: BVXI [2, 3]

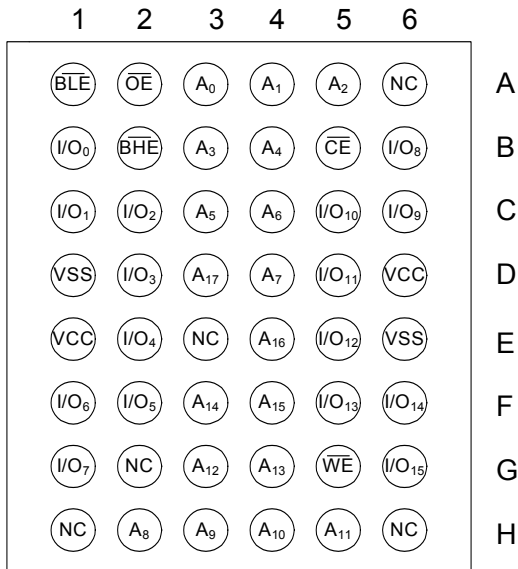


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout, Package/Grade ID: BVJXI [2]

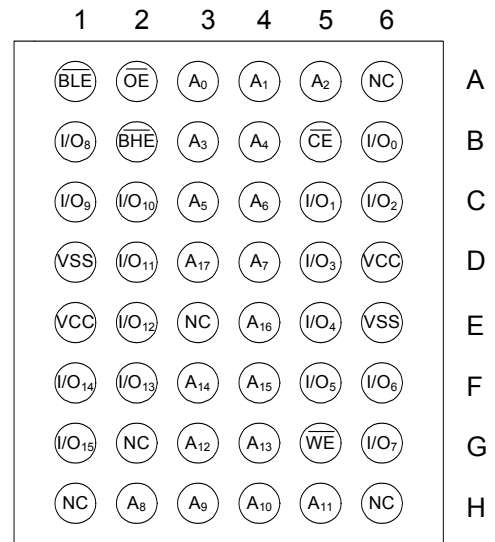
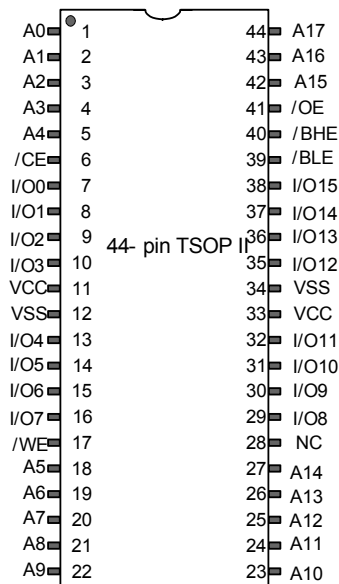


Figure 3. 44-pin TSOP II / 44-pin SOJ pinout [2]



**Notes**

- 2. NC pins are not connected internally to the die.
- 3. Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O<sub>[7:0]</sub> and I/O<sub>[15:8]</sub> balls are swapped.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
on V<sub>CC</sub> relative to GND [4] ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC voltage applied to outputs  
in HI-Z State [4] ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC input voltage [4] ..... -0.5 V to V<sub>CC</sub> + 0.5 V

Current into outputs (in LOW state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Grade	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

## DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit	
			Min	Typ <sup>[5]</sup>	Max		
V <sub>OH</sub>	Output HIGH voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	-	-	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2	-	-	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.2	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5 <sup>[6]</sup>	-	-	
V <sub>OL</sub>	Output LOW voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.2	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA	-	-	0.4	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
V <sub>IH</sub>	Input HIGH voltage	1.65 V to 2.2 V	-	1.4	-	V <sub>CC</sub> + 0.2 <sup>[4]</sup>	V
		2.2 V to 2.7 V	-	2	-	V <sub>CC</sub> + 0.3 <sup>[4]</sup>	
		2.7 V to 3.6 V	-	2	-	V <sub>CC</sub> + 0.3 <sup>[4]</sup>	
		4.5 V to 5.5 V	-	2.2	-	V <sub>CC</sub> + 0.5 <sup>[4]</sup>	
V <sub>IL</sub>	Input LOW voltage	1.65 V to 2.2 V	-	-0.2 <sup>[4]</sup>	-	0.4	V
		2.2 V to 2.7 V	-	-0.3 <sup>[4]</sup>	-	0.6	
		2.7 V to 3.6 V	-	-0.3 <sup>[4]</sup>	-	0.8	
		4.5 V to 5.5 V	-	-0.5 <sup>[4]</sup>	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	-	+1	μA	
I <sub>CC</sub>	Operating supply current	Max V <sub>CC</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	f = 100 MHz	-	38	45	mA
			f = 66.7 MHz	-	-	40	
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	-	15	mA	
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	6	8	mA	

### Notes

4. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 2 ns.

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

6. This parameter is guaranteed by design and not tested.

### Capacitance

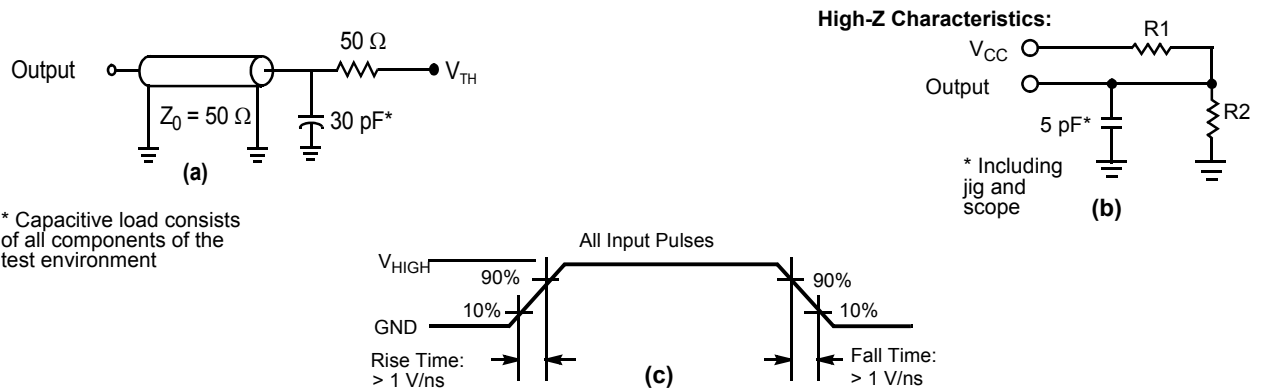
Parameter [7]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ)	10	10	10	pF
C <sub>OUT</sub>	I/O capacitance		10	10	10	pF

### Thermal Resistance

Parameter [7]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.35	55.37	68.85	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		14.74	30.41	15.97	°C/W

### AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [8]



\* Capacitive load consists of all components of the test environment

Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V <sub>TH</sub>	0.9	1.5	1.5	V
V <sub>HIGH</sub>	1.8	3	3	V

**Notes**

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device AC operation assumes a 100-μs ramp time from 0 to V<sub>CC</sub>(min) and a 100-μs wait time after V<sub>CC</sub> stabilization.

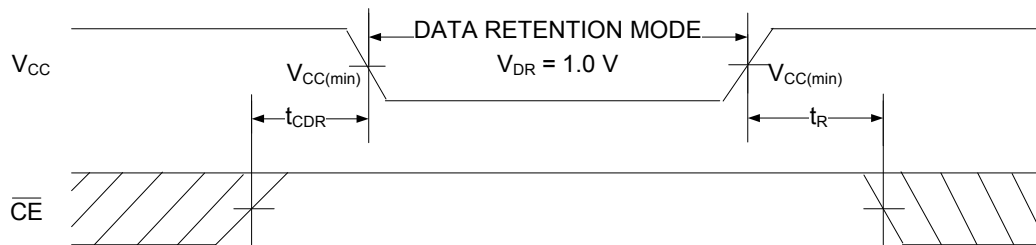
### Data Retention Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1	-	V
$I_{CCDR}$	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ <sup>[9]</sup> , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ , or $V_{IN} \leq 0.2\text{ V}$	-	8	mA
$t_{CDR}$ <sup>[10]</sup>	Chip deselect to data retention time		0	-	ns
$t_R$ <sup>[9, 10]</sup>	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10	-	ns
		$V_{CC} < 2.2\text{ V}$	15	-	ns

### Data Retention Waveform

Figure 5. Data Retention Waveform <sup>[9]</sup>



**Notes**

- 9. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)}$   $\geq 100\ \mu\text{s}$  or stable at  $V_{CC(min)}$   $\geq 100\ \mu\text{s}$ .
- 10. These parameters are guaranteed by design.

## AC Switching Characteristics

Over the operating range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter <sup>[11]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	10	–	15	–	ns
$t_{AA}$	Address to data	–	10	–	15	ns
$t_{OHA}$	Data hold from address change	3	–	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data <sup>[12]</sup>	–	10	–	15	ns
$t_{DOE}$	$\overline{OE}$ LOW to data	–	4.5	–	8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low impedance <sup>[13, 14]</sup>	0	–	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to HI-Z <sup>[13, 14]</sup>	–	5	–	8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low impedance <sup>[12, 13, 14]</sup>	3	–	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to HI-Z <sup>[12, 13, 14]</sup>	–	5	–	8	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[12, 14, 15]</sup>	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[12, 14, 15]</sup>	–	10	–	15	ns
$t_{DBE}$	Byte enable to data valid	–	4.5	–	8	ns
$t_{LZBE}$	Byte enable to low impedance <sup>[14]</sup>	0	–	0	–	ns
$t_{HZBE}$	Byte disable to HI-Z <sup>[14]</sup>	–	6	–	8	ns
<b>Write Cycle <sup>[15, 16]</sup></b>						
$t_{WC}$	Write cycle time	10	–	15	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end <sup>[12]</sup>	7	–	12	–	ns
$t_{AW}$	Address setup to write end	7	–	12	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	12	–	ns
$t_{SD}$	Data setup to write end	5	–	8	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low impedance <sup>[13, 14]</sup>	3	–	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to HI-Z <sup>[13, 14]</sup>	–	5	–	8	ns
$t_{BW}$	Byte Enable to write end	7	–	12	–	ns

### Notes

- Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3\text{ V}$ ) and  $V_{CC}/2$  (for  $V_{CC} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3\text{ V}$ ) and 0 to  $V_{CC}$  (for  $V_{CC} < 3\text{ V}$ ). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 4 on page 6, unless specified otherwise.
- For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . When  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW,  $\overline{CE}$  is HIGH.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 4 on page 6. Transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle pulse width in Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .



### Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [17, 18]

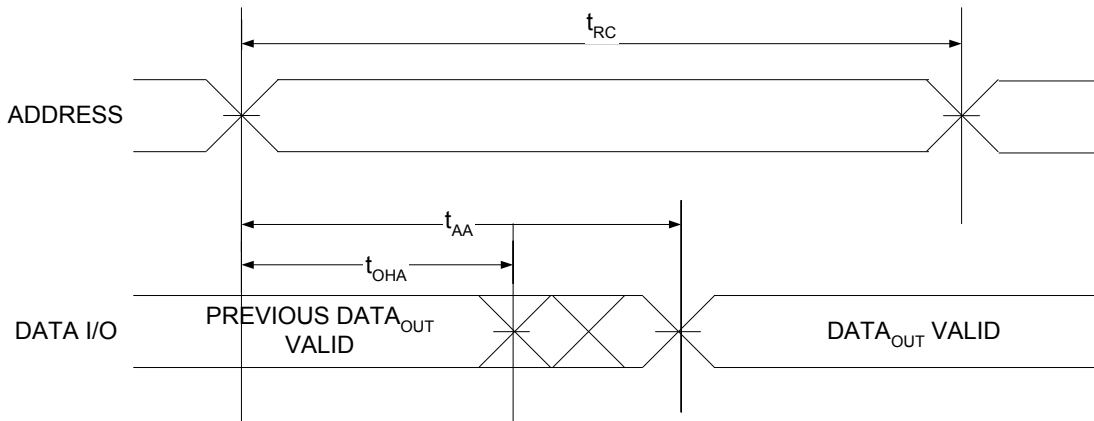
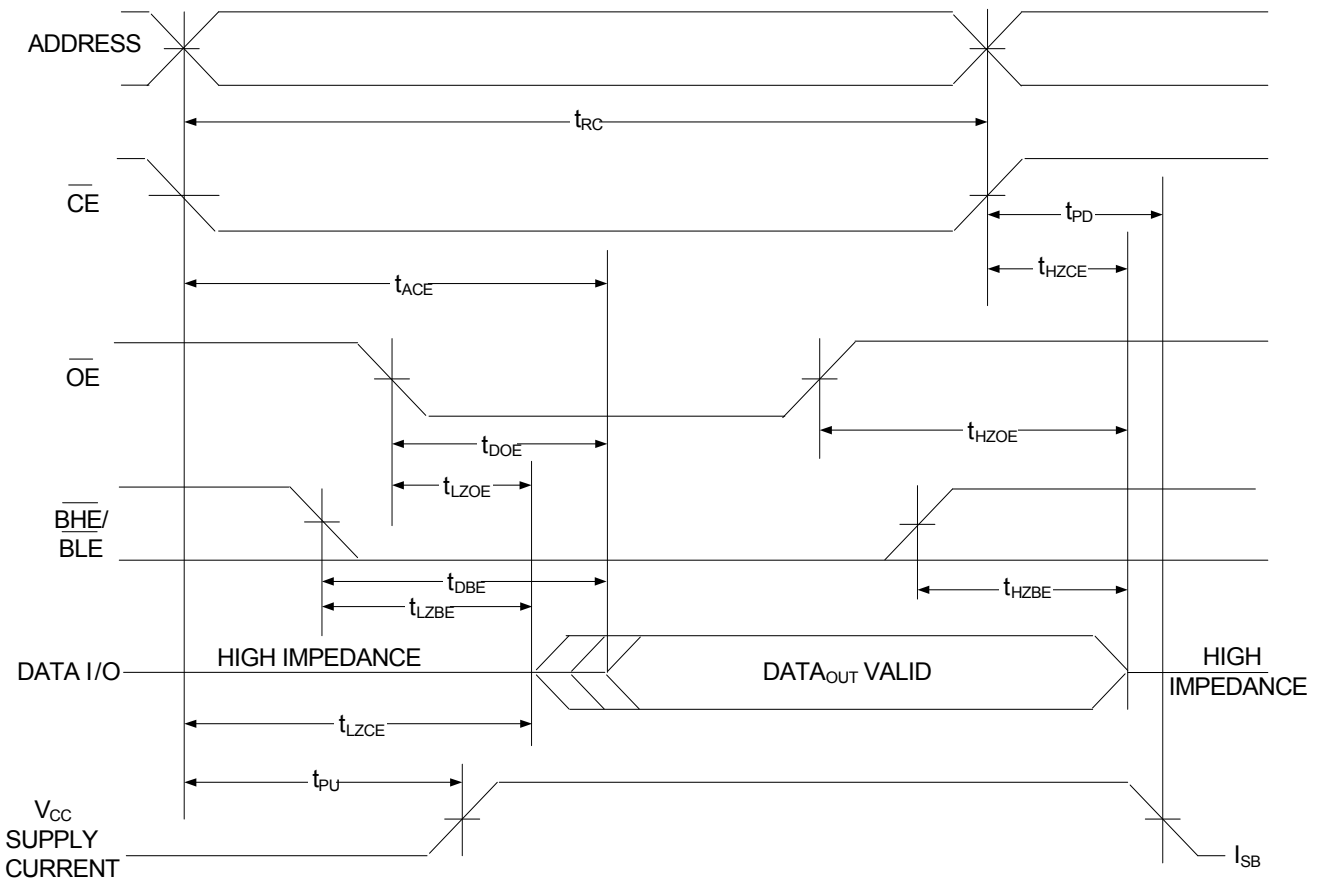


Figure 7. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [18, 19]



**Notes**

- 17. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .
- 18.  $\overline{WE}$  is HIGH for the read cycle.
- 19. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [20, 21]

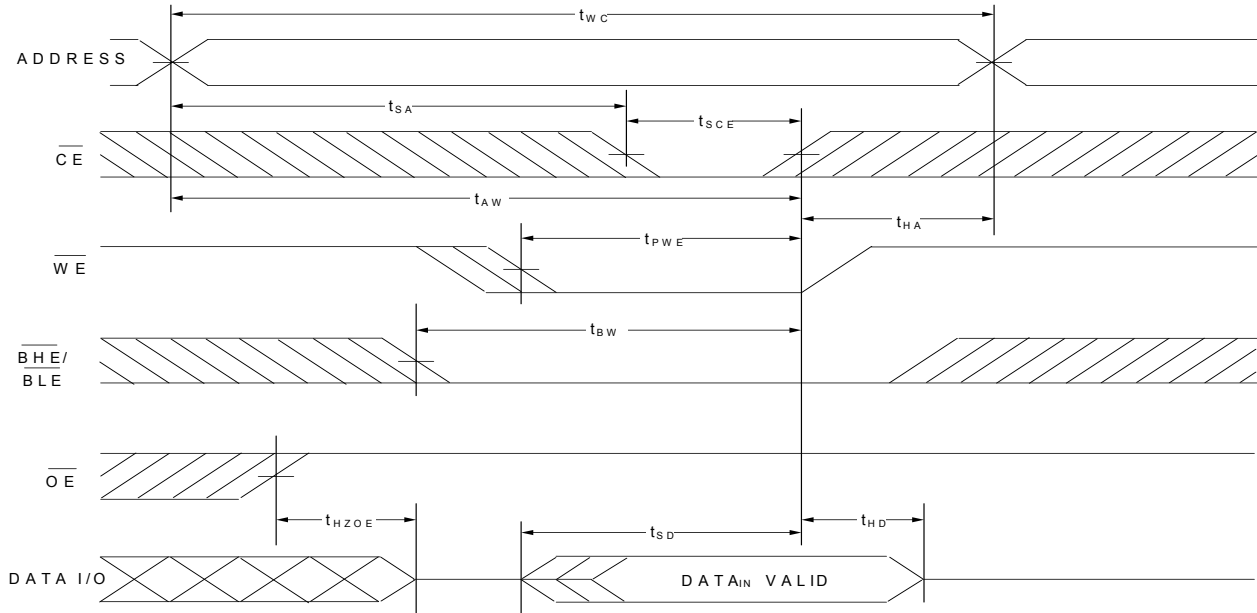
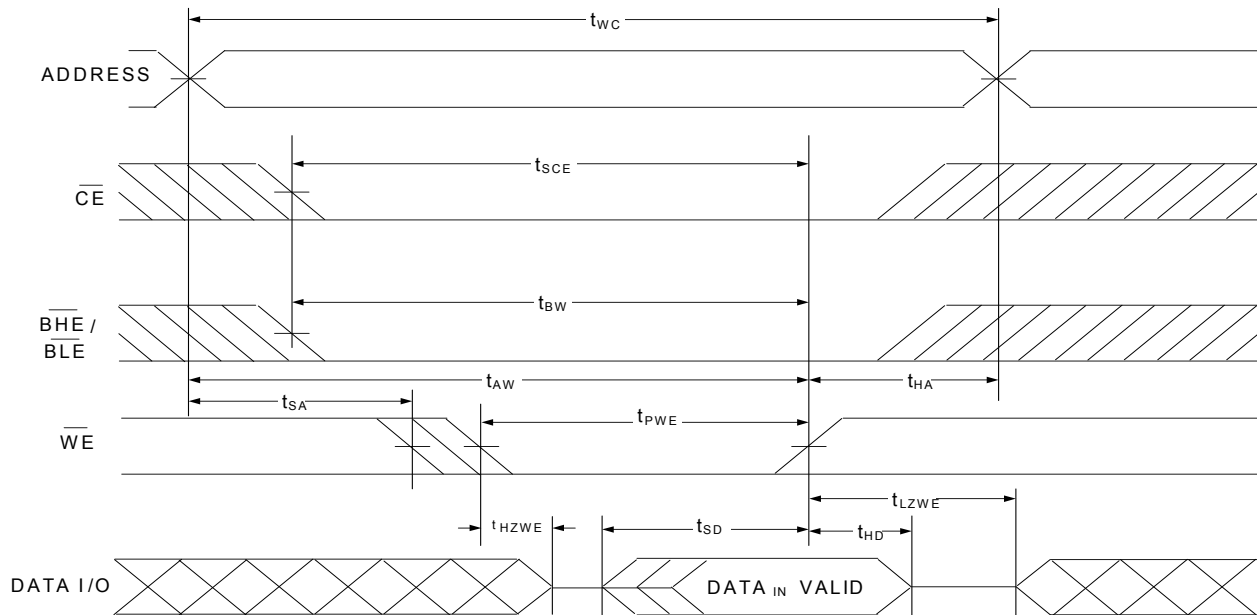


Figure 9. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [20, 21, 22]



Notes

- 20. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ , and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 21. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 22. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) [23, 24]

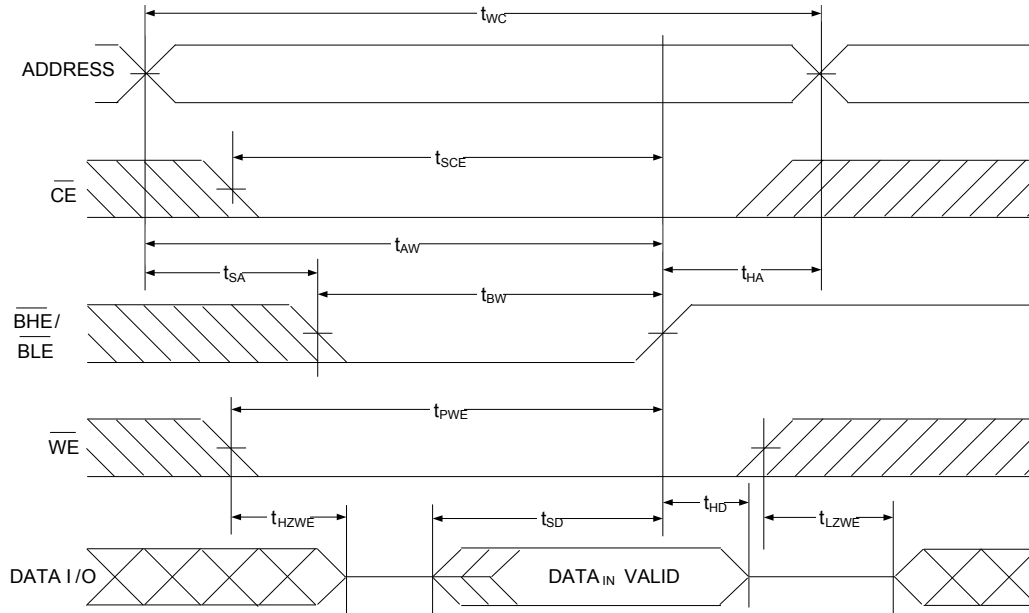
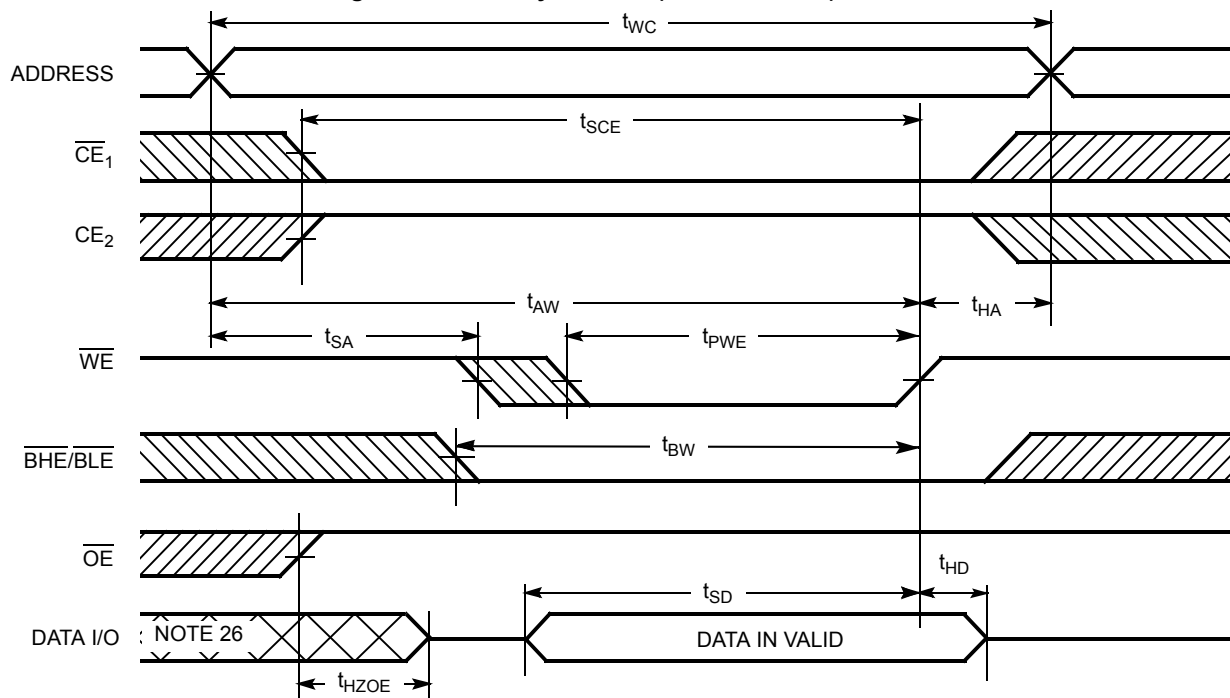


Figure 11. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled) [23, 24, 25]



Notes

23. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ , and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

24. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

25. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .

26. During this period the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X <sup>[27]</sup>	X <sup>[27]</sup>	X <sup>[27]</sup>	X <sup>[27]</sup>	HI-Z	HI-Z	Power down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

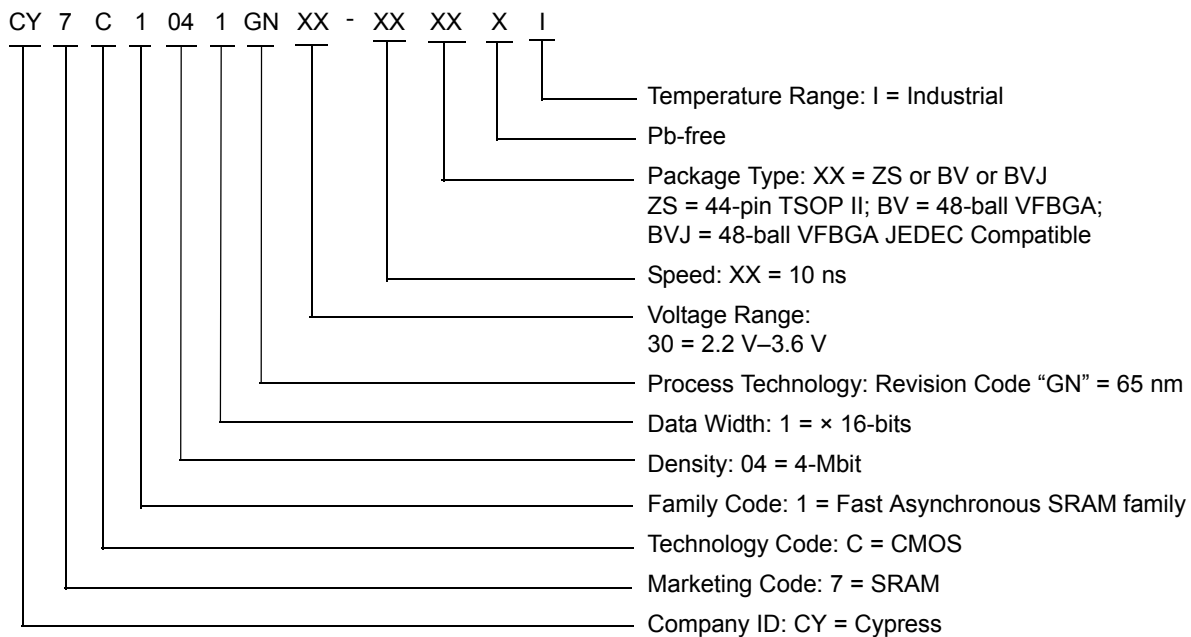
**Notes**

27. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

### Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1041GN30-10ZSXI	51-85087	44-pin TSOP II	Industrial
		CY7C1041GN30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7C1041GN30-10BVJXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC Compatible	
	4.5 V–5.5 V	CY7C1041GN-10ZSXI		44-pin TSOP II	

### Ordering Code Definitions



Package Diagrams

Figure 12. 44-pin TSOP II (Z44) Package Outline, 51-85087

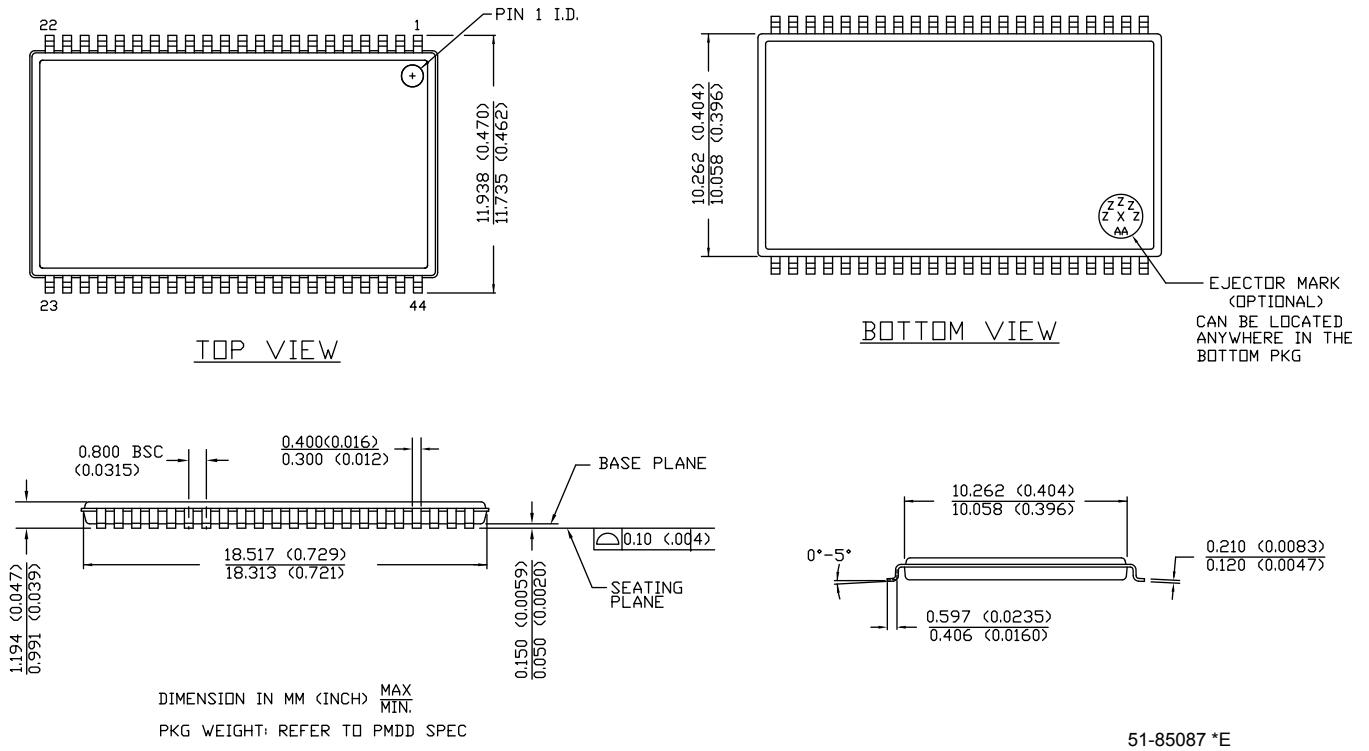
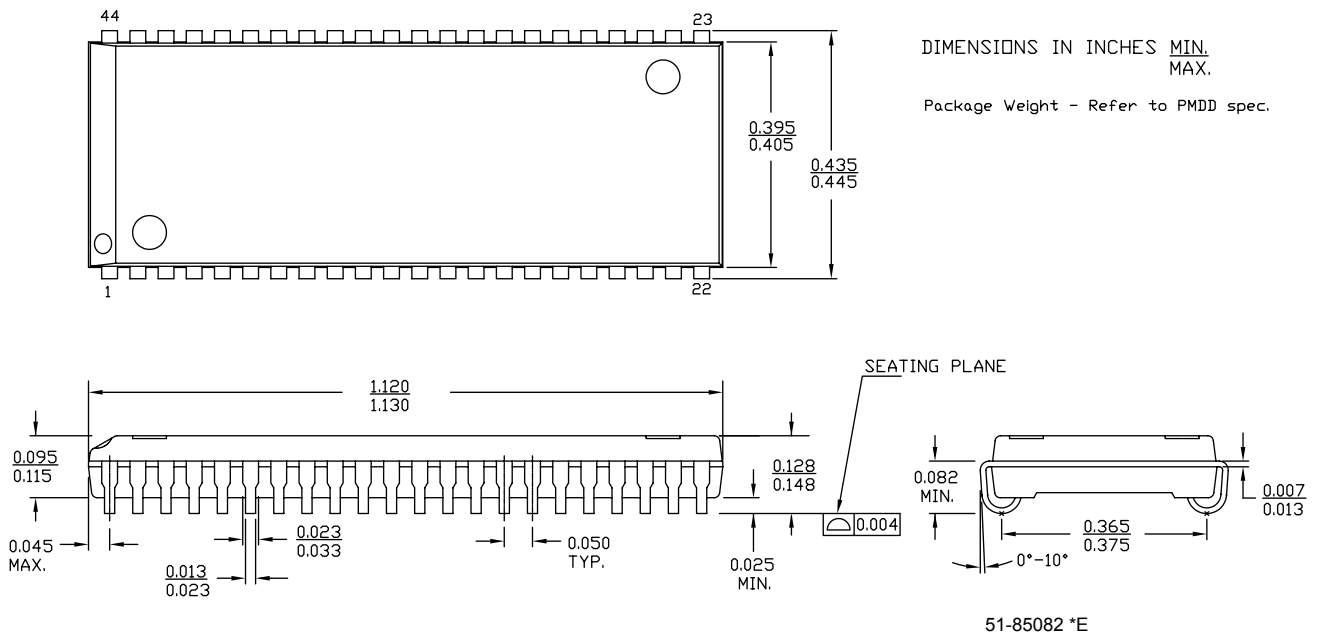
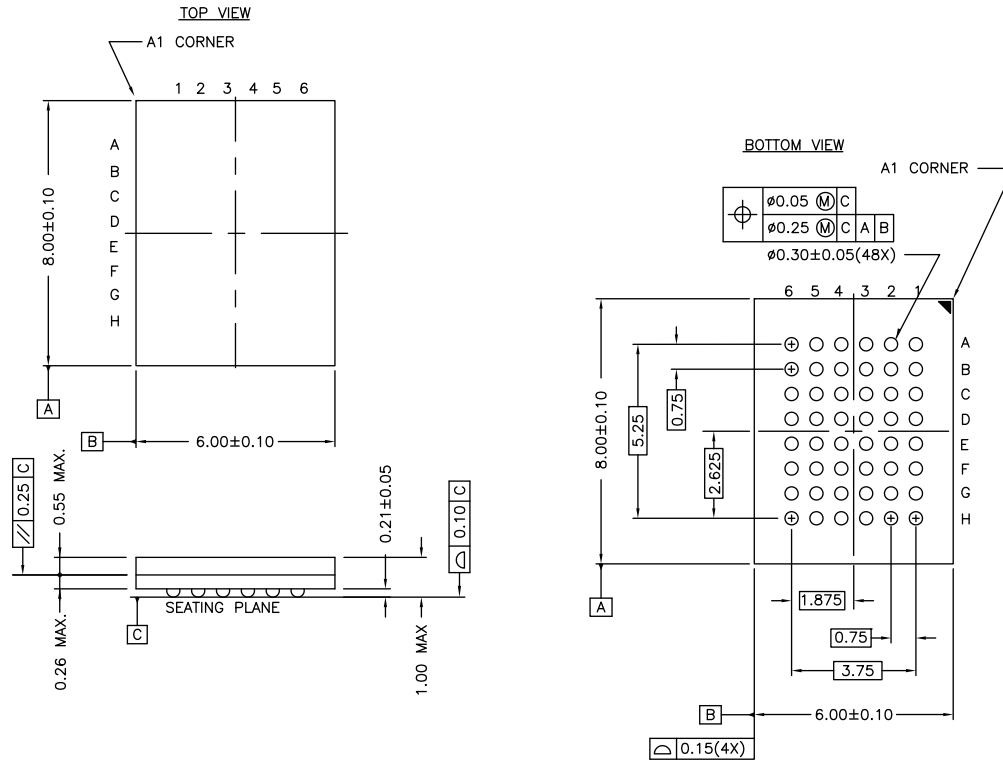


Figure 13. 44-pin SOJ (400 Mils) Package Outline, 51-85082



Package Diagrams (continued)

Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random-access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts



## Document History Page

Document Title: CY7C1041GN, 4-Mbit (256K words × 16 bit) Static RAM Document Number: 001-95413				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	5074414	NILE	01/06/2016	New data sheet.
*A	5082573	NILE	01/12/2016	Updated <a href="#">Logic Block Diagram – CY7C1041GN</a> . Updated <a href="#">Ordering Information</a> : Updated part numbers.
*B	5120171	VINI	02/01/2016	Updated <a href="#">Logic Block Diagram – CY7C1041GN</a> .

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