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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

June 2016

FDMD84100

Dual N-Channel PowerTrench® MOSFET

100 V, 21 A, 20 mΩ

Features

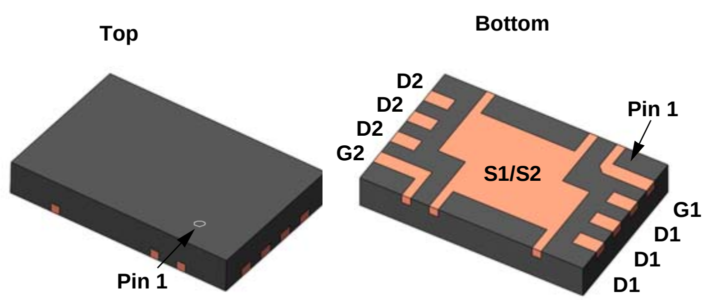
- Max $r_{DS(on)}$ = 20 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $r_{DS(on)}$ = 32 mΩ at V_{GS} = 6 V, I_D = 5.5 A
- Ideal for flexible layout in secondary side synchronous rectification
- Termination is Lead-free and RoHS Compliant
- 100% UIL tested

General Description

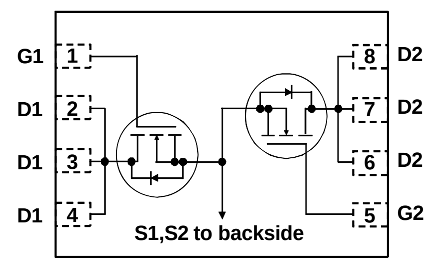
This package integrates two N-Channel devices connected internally in common-source configuration. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (3.3 x 5 mm) for higher power density.

Applications

- Isolated DC-DC Synchronous Rectifiers
- Common Ground Load Switches



Power 3.3 x 5



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		21	A
	-Continuous	T_A = 25 °C	(Note 1a)	7	
	-Pulsed		(Note 4)	80	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	121	mJ
P_D	Power Dissipation	T_C = 25 °C		23	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		5.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

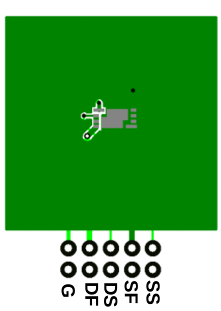
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
84100	FDMD84100	Power 3.3 x 5	13 ”	12 mm	3000 units

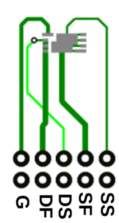
Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		74		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3.1	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A		16	20	mΩ
		V_{GS} = 6 V, I_D = 5.5 A		24	32	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125 °C		30	38	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 7 A		17		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V f = 1 MHz		734	980	pF
C_{oss}	Output Capacitance			168	225	pF
C_{rss}	Reverse Transfer Capacitance			6.6	15	pF
R_g	Gate Resistance		0.1	1.3	3	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 7 A V_{GS} = 10 V, R_{GEN} = 6 Ω		8.4	17	ns
t_r	Rise Time			2.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
t_f	Fall Time			2.8	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 7 A		11	16	nC
	Total Gate Charge	V_{GS} = 0 V to 6 V; V_{DD} = 50 V, I_D = 7 A		7.3	11	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 7 A		3.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs		43	70	ns
Q_{rr}	Reverse Recovery Charge			44	71	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 160 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 121 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 9 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 30 A.
4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25 °C unless otherwise noted

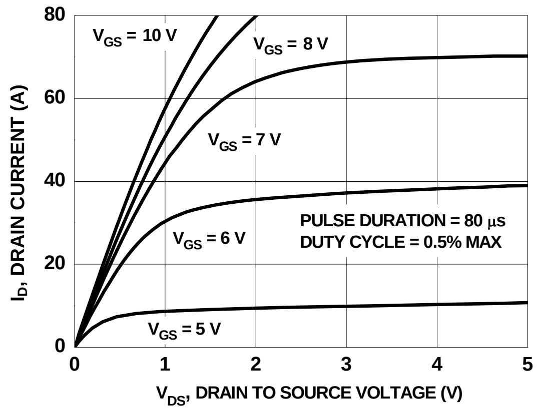


Figure 1. On-Region Characteristics

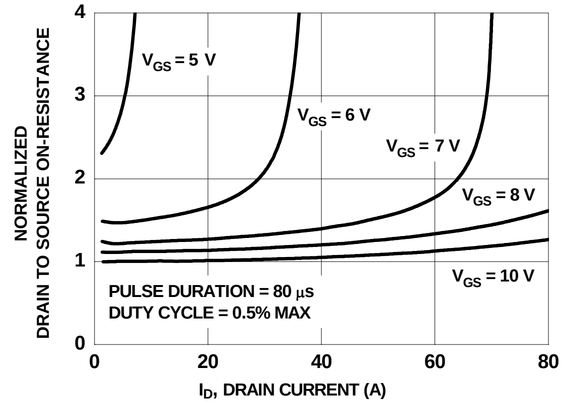


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

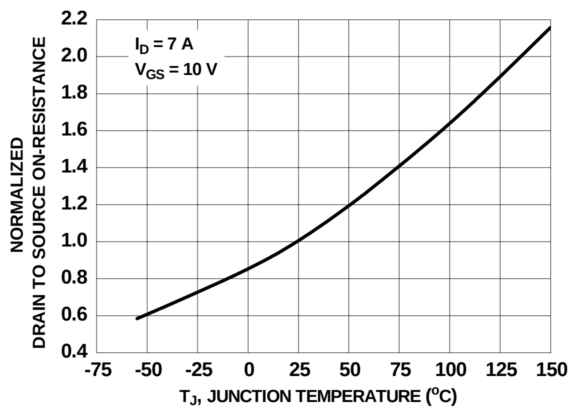


Figure 3. Normalized On-Resistance vs Junction Temperature

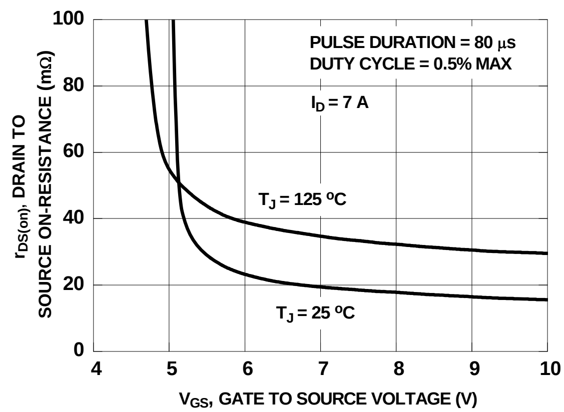


Figure 4. On-Resistance vs Gate to Source Voltage

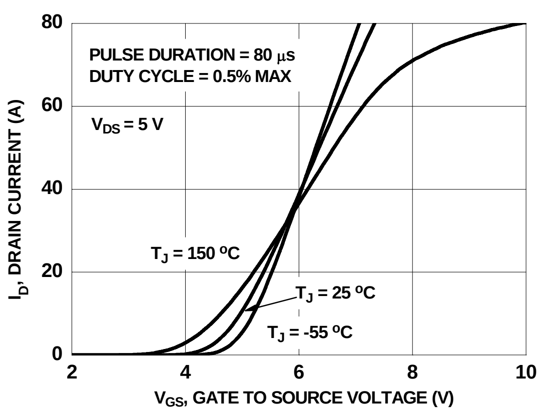


Figure 5. Transfer Characteristics

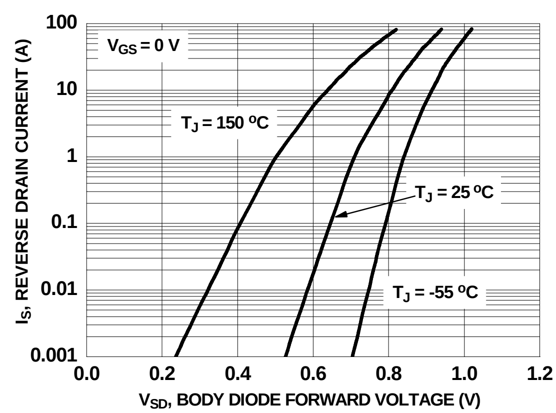


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

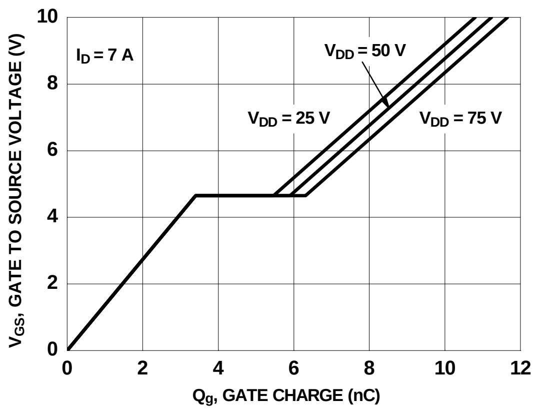


Figure 7. Gate Charge Characteristics

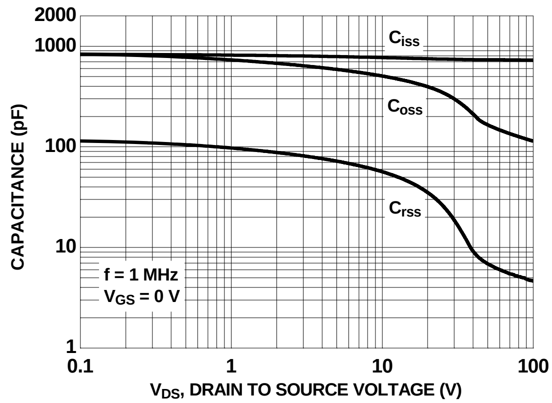


Figure 8. Capacitance vs Drain to Source Voltage

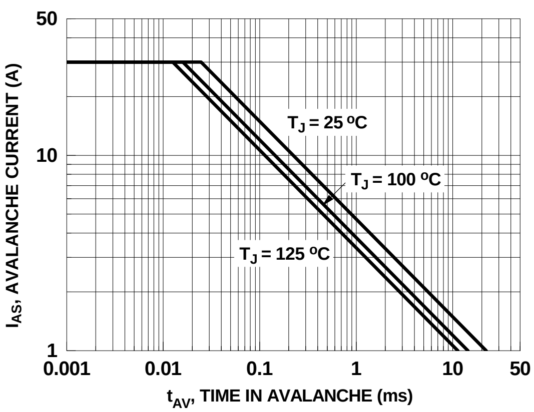


Figure 9. Unclamped Inductive Switching Capability

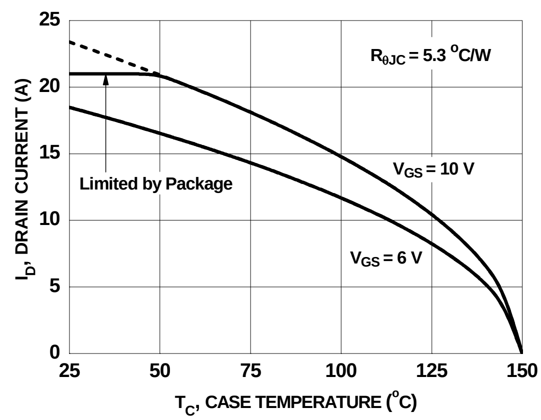


Figure 10. Maximum Continuous Drain Current vs Case Temperature

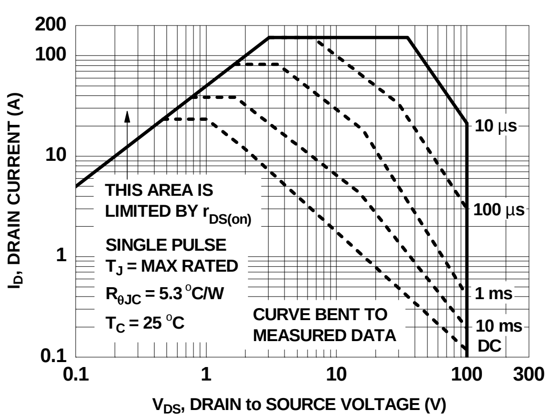


Figure 11. Forward Bias Safe Operating Area

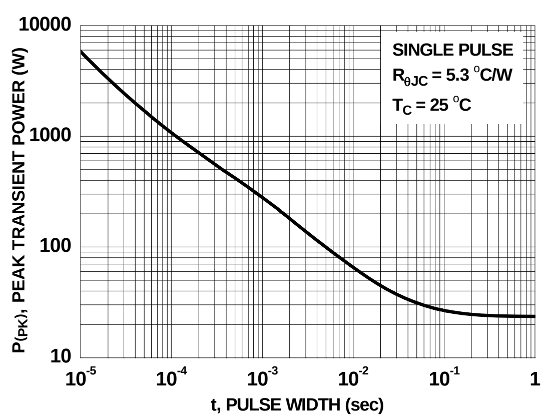


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

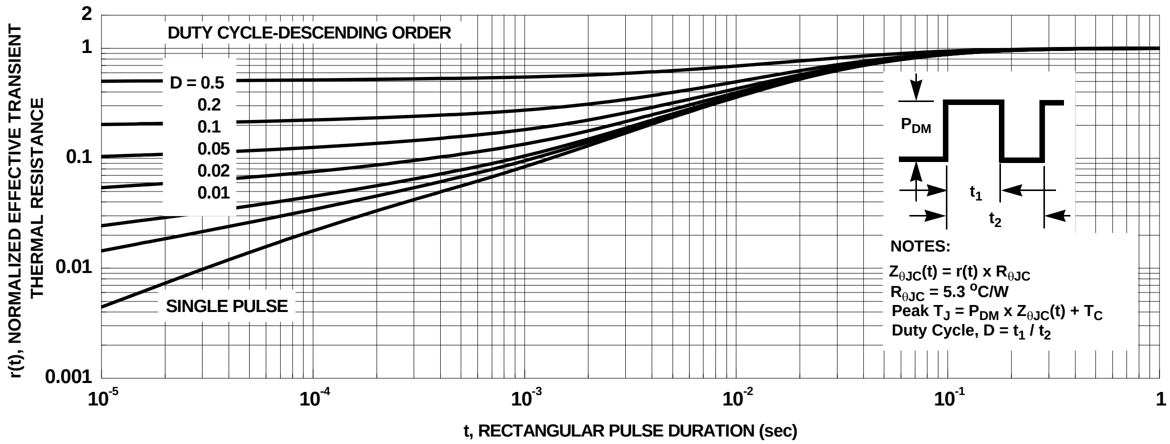
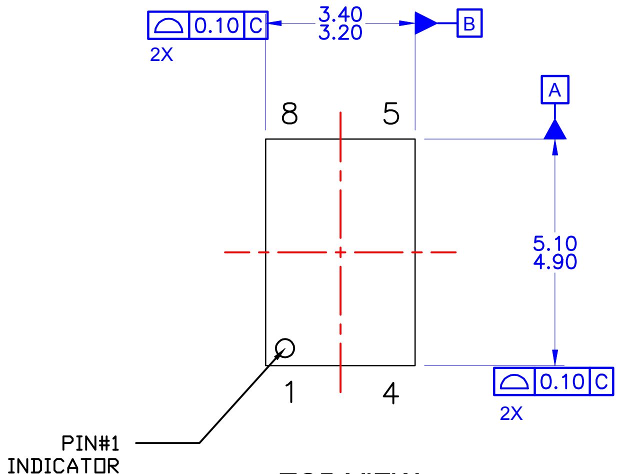
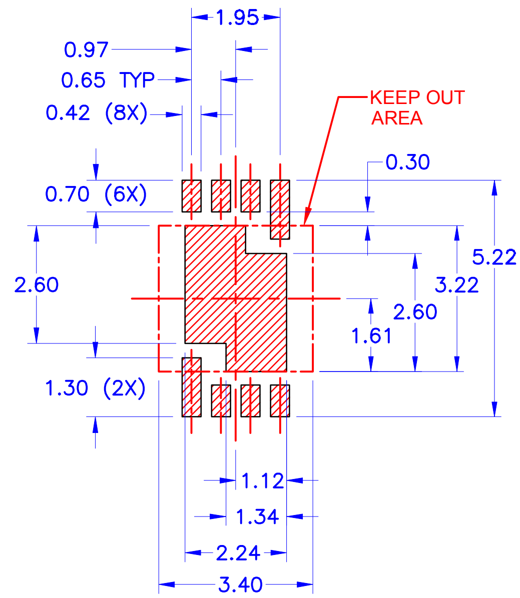


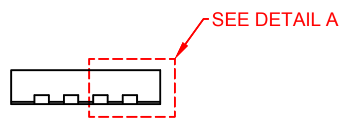
Figure 13. Junction-to-Case Transient Thermal Response Curve



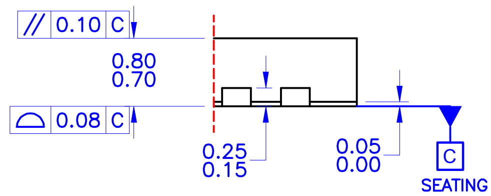
TOP VIEW



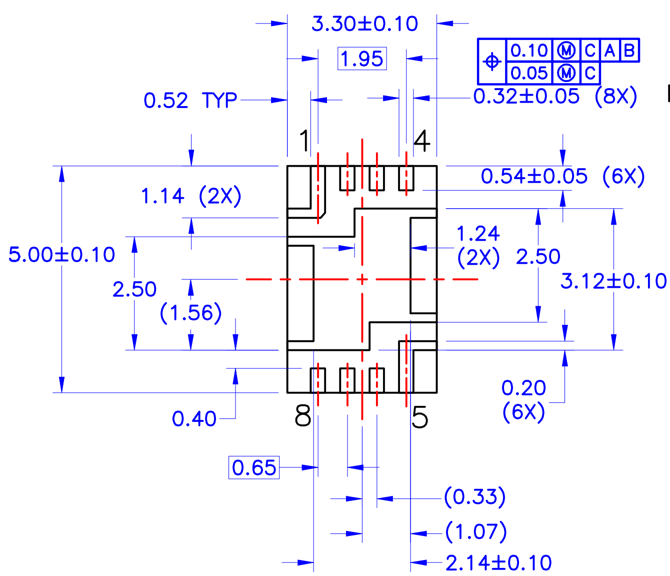
LAND PATTERN
RECOMMENDATION



FRONT VIEW



DETAIL A
SCALE: 2X



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO229 DATED 8/2012.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: MKT–PQFN08NREV1.

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