

MC100LVEP111

2.5V / 3.3V 1:10 Differential ECL/PECL/HSTL Clock Driver

Description

The MC100LVEP111 is a low skew 1-to-10 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP111 is operating under PECL conditions.

The LVEP111 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure tightest skew, both sides of differential outputs identically terminate into $50\ \Omega$ even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The MC100LVEP111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVEP111 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single-ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in NECL mode. Designers can take advantage of the LVEP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Application Note AN1406/D.

Features

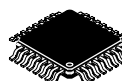
- 85 ps Typical Device-to-Device Skew
- 20 ps Typical Output-to-Output Skew
- Jitter Less than 1 ps RMS
- Maximum Frequency > 3 Ghz Typical
- V_{BB} Output
- 430 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode Operating Range: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Open Input Default State
- LVDS Input Compatible
- Fully Compatible with MC100EP111
- Pb-Free Packages are Available



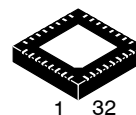
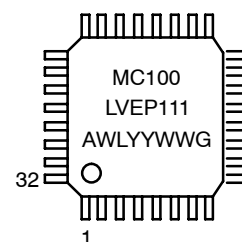
ON Semiconductor®

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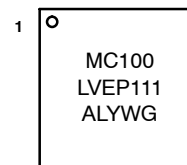
MARKING DIAGRAM*



LQFP-32
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM



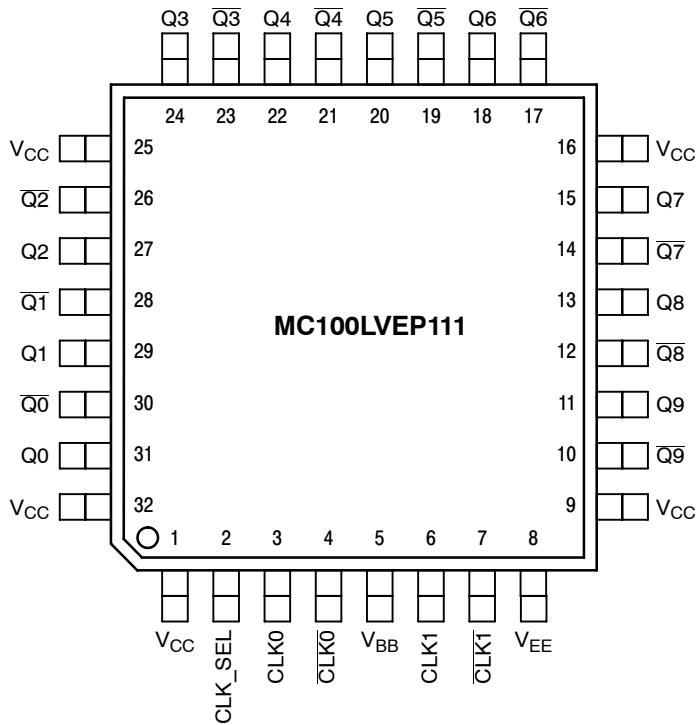
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP-32 Pinout (Top View)

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|--------------------------------------|--|
| CLK0*, $\overline{\text{CLK0}}^{**}$ | ECL/PECL/HSTL CLK Input |
| CLK1*, $\overline{\text{CLK1}}^{**}$ | ECL/PECL/HSTL CLK Input |
| Q0:9, $\overline{\text{Q0}}:9$ | ECL/PECL Outputs |
| CLK_SEL* | ECL/PECL Active Clock Select Input |
| V _{BB} | Reference Voltage Output |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |
| EP | The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to V _{EE} . |

* Pins will default LOW when left open.

** Pins will default to V_{CC}/2 when left open.

Table 2. FUNCTION TABLE

| CLK_SEL | Active Input |
|---------|--------------------------------|
| L | CLK0, $\overline{\text{CLK0}}$ |
| H | CLK1, $\overline{\text{CLK1}}$ |

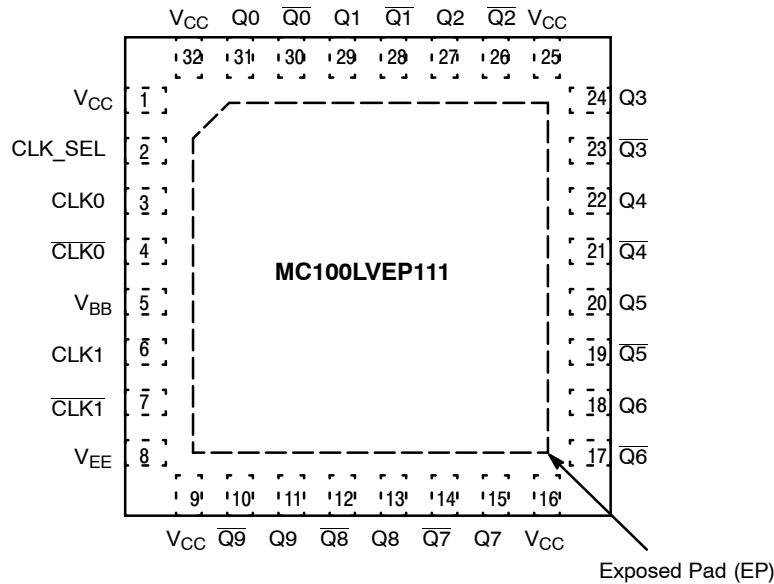


Figure 2. QFN-32 Pinout (Top View)

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Table 3. ATTRIBUTES

| Characteristics | | Value | |
|--|---|-----------------------------|--------------|
| Internal Input Pulldown Resistor | | 75 k Ω | |
| Internal Input Pullup Resistor | | 37.5 k Ω | |
| ESD Protection | Human Body Model Machine Model Charged Device Model | > 2 kV > 100 V > 2 kV | |
| Moisture Sensitivity (Note 1) | | Pb Pkgs | Pb-Free Pkgs |
| | | LQFP Level 2 | Level 2 |
| | | QFN Level 1 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 602 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, refer to Application Note AND8003/D.

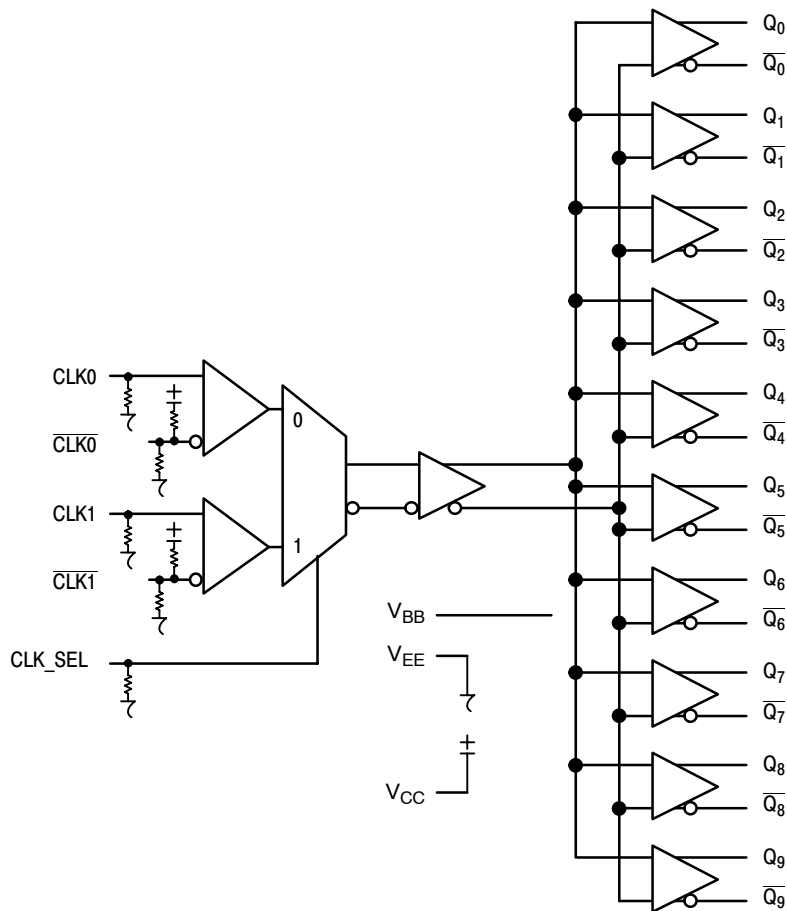


Figure 3. Logic Diagram

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Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|------------------|--|------------------------------------|----------------------------------|-------------|-------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | PECL Mode Input Voltage | V _{EE} = 0 V | V _I ≤ V _{CC} | 6 | V |
| | NECL Mode Input Voltage | V _{CC} = 0 V | V _I ≥ V _{EE} | -6 | V |
| I _{out} | Output Current | Continuous Surge | | 50 | mA |
| | | | | 100 | mA |
| I _{BB} | V _{BB} Sink/Source | | | ± 0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | LQFP-32 | 80 | °C/W |
| | | 500 lfpm | LQFP-32 | 55 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | LQFP-32 | 12 to 17 | °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | QFN-32 | 31 | °C/W |
| | | 500 lfpm | QFN-32 | 27 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | 2S2P | QFN-32 | 12 | °C/W |
| T _{sol} | Wave Solder | < 3 sec @ 248°C < 3 sec @ 260°C | | 265 | °C |
| | Pb Pb-Free (QFN-32 Only) | | | 265 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 5. PECL DC CHARACTERISTICS $V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--|------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 60 | 90 | 120 | 60 | 90 | 120 | 60 | 90 | 120 | mA |
| V_{OH} | Output HIGH Voltage (Note 3) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| V_{OL} | Output LOW Voltage (Note 3) | 555 | 730 | 900 | 555 | 730 | 900 | 555 | 730 | 900 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) (Note 4) | 1335 | | 1620 | 1335 | | 1620 | 1275 | | 1620 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) (Note 4) | 555 | | 875 | 555 | | 875 | 555 | | 875 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | $\frac{\text{CLK}}{\text{CLK}}$ 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.125 V to -1.3 V.
- All loading with 50 Ω to V_{EE} .
- Do not use V_{BB} at $V_{CC} < 3.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. PECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 6)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--|------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 60 | 90 | 120 | 60 | 90 | 120 | 60 | 90 | 120 | mA |
| V_{OH} | Output HIGH Voltage (Note 7) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage (Note 7) | 1355 | 1530 | 1700 | 1355 | 1530 | 1700 | 1355 | 1530 | 1700 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| V_{BB} | Output Reference Voltage (Note 8) | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | $\frac{\text{CLK}}{\text{CLK}}$ 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.925 V to -0.5 V.
- All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
- Single ended input operation is limited $V_{CC} \geq 3.0\text{ V}$ in PECL mode.
- V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 7. NECL DC CHARACTERISTICS $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V}$ to -3.8 V (Note 10)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|--|-------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 60 | 90 | 120 | 60 | 90 | 120 | 60 | 90 | 120 | mA |
| V_{OH} | Output HIGH Voltage (Note 11) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 11) | -1945 | -1770 | -1600 | -1945 | -1770 | -1600 | -1945 | -1770 | -1600 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1945 | | -1625 | -1945 | | -1625 | -1945 | | -1625 | mV |
| V_{BB} | Output Reference Voltage (Note 12) | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | $V_{EE} + 1.2$ | | 0.0 | $V_{EE} + 1.2$ | | 0.0 | $V_{EE} + 1.2$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | $\frac{\text{CLK}}{\text{CLK}}$ 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with V_{CC} .

11. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

12. Single ended input operation is limited $V_{EE} \leq -3.0\text{ V}$ in NECL mode.

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. HSTL DC CHARACTERISTICS $V_{CC} = 2.375$ to 3.8 V , $V_{EE} = 0\text{ V}$

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|-------------------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{IH} | Input HIGH Voltage | 1200 | | | 1200 | | | 1200 | | | mV |
| V_{IL} | Input LOW Voltage | | | 400 | | | 400 | | | 400 | mV |
| V_x | Input Crossover Voltage | 680 | | 900 | 680 | | 900 | 680 | | 900 | mV |
| I_{CC} | Power Supply Current | 70 | 100 | 120 | 70 | 100 | 120 | 70 | 100 | 120 | mA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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Table 9. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -2.375\text{ to }-3.8\text{ V}$ or $V_{CC} = 2.375\text{ to }3.8\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 14)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------------------|---|-------|--|--|------|--|--|------|--|--|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{maxPECL/HSTL}}$ | Maximum Frequency (Figure 4) | | 3 | | | 3 | | | 3 | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay (Differential Configuration) | 325 | 400 | 475 | 350 | 430 | 500 | 440 | 510 | 590 | ps |
| t_{skew} | Within-Device Skew (Note 15) Within-Device Skew @ 2.5 V (Note 15) Device-to-Device Skew (Note 16) | | 20 20 85 | 25 25 150 | | 20 20 85 | 25 25 150 | | 25 20 85 | 35 25 150 | ps |
| t_{JITTER} | CLOCK Random Jitter (RMS) @ $\leq 0.5\text{ GHz}$ @ $\leq 1.0\text{ GHz}$ @ $\leq 1.5\text{ GHz}$ @ $\leq 2.0\text{ GHz}$ @ $\leq 2.5\text{ GHz}$ @ $\leq 3.0\text{ GHz}$ | | 0.209 0.200 0.197 0.220 0.232 0.348 | 0.5 0.5 0.4 0.5 0.4 0.6 | | 0.204 0.214 0.213 0.224 0.290 0.545 | 0.5 0.6 0.5 0.5 0.5 0.8 | | 0.221 0.229 0.243 0.292 0.522 0.911 | 0.5 0.5 0.4 0.6 0.8 1.3 | ps |
| V_{PP} | Minimum Input Swing | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| $t_{\text{r}}/t_{\text{f}}$ | Output Rise/Fall Time (20%–80%) | 105 | 200 | 255 | 125 | 200 | 275 | 150 | 230 | 320 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured with 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

15. Skew is measured between outputs under identical transitions and conditions on any one device.

16. Device-to-Device skew for identical transitions at identical V_{CC} levels.

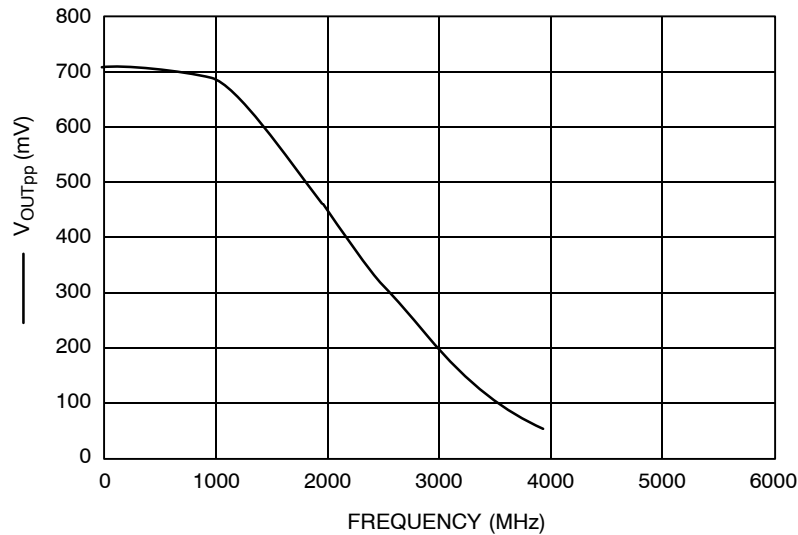


Figure 4. F_{max} Typical

MC100LVEP111

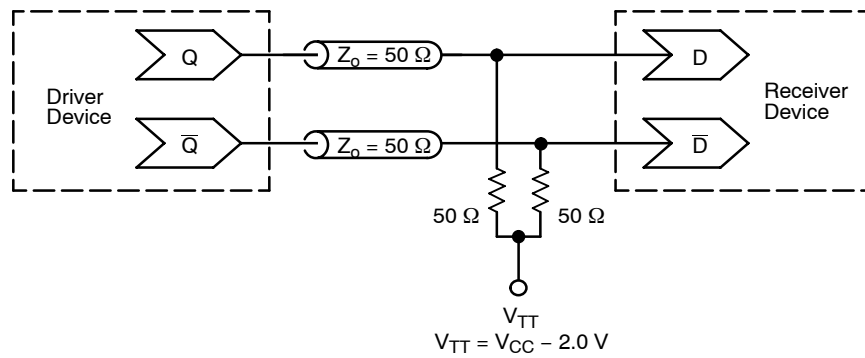


Figure 5. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|----------------------|--------------------|
| MC100LVEP111FA | LQFP-32 | 250 Units / Tray |
| MC100LVEP111FAG | LQFP-32 (Pb-Free) | 250 Units / Tray |
| MC100LVEP111FAR2 | LQFP-32 | 2000 / Tape & Reel |
| MC100LVEP111FARG | LQFP-32 (Pb-Free) | 2000 / Tape & Reel |
| MC100LVEP111MNG | QFN-32 (Pb-Free) | 74 Units / Rail |
| MC100LVEP111MNRG | QFN-32 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

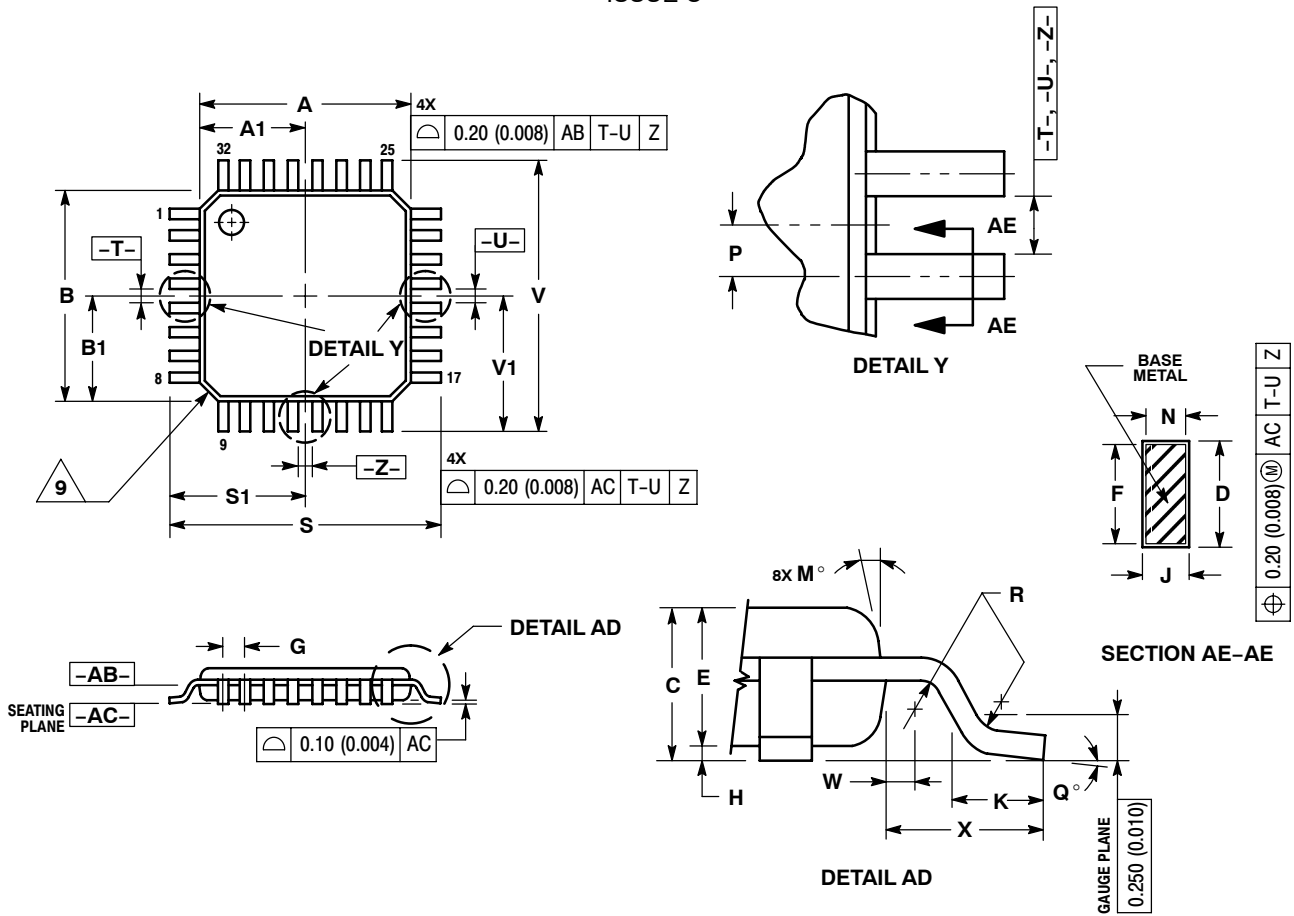
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A-02
ISSUE C



NOTES:

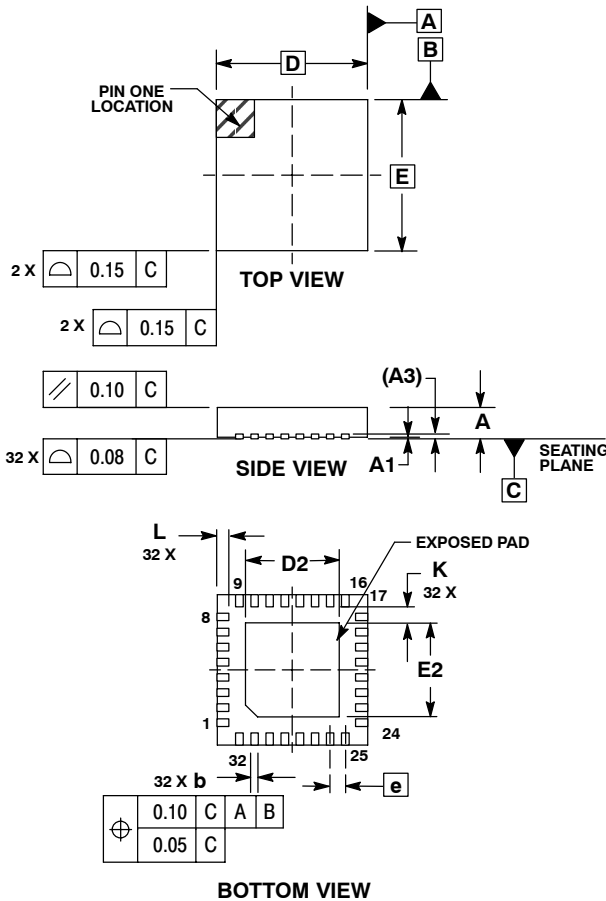
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
- MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
- EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 7.000 | BSC | 0.276 | BSC |
| A1 | 3.500 | BSC | 0.138 | BSC |
| B | 7.000 | BSC | 0.276 | BSC |
| B1 | 3.500 | BSC | 0.138 | BSC |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 | BSC | 0.031 | BSC |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.450 | 0.750 | 0.018 | 0.030 |
| M | 12° | REF | 12° | REF |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 | BSC | 0.016 | BSC |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 | BSC | 0.354 | BSC |
| S1 | 4.500 | BSC | 0.177 | BSC |
| V | 9.000 | BSC | 0.354 | BSC |
| V1 | 4.500 | BSC | 0.177 | BSC |
| W | 0.200 | REF | 0.008 | REF |
| X | 1.000 | REF | 0.039 | REF |

MC100LVEP111

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P
CASE 488AM-01
ISSUE 0

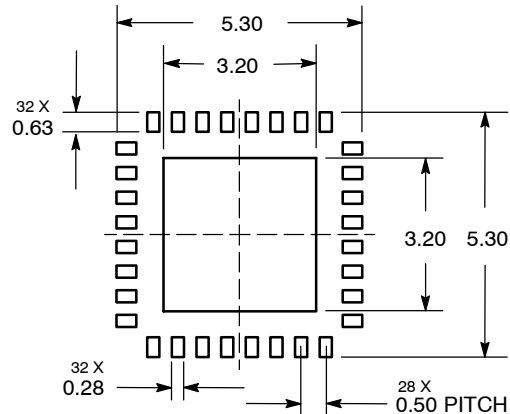


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | 0.200 REF | | |
| b | 0.180 | 0.250 | 0.300 |
| D | 5.00 BSC | | |
| D2 | 2.950 | 3.100 | 3.250 |
| E | 5.00 BSC | | |
| E2 | 2.950 | 3.100 | 3.250 |
| e | 0.500 BSC | | |
| K | 0.200 | --- | --- |
| L | 0.300 | 0.400 | 0.500 |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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