DS1386/DS1386P
RAMified Watchdog Timekeeper

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1386 is a nonvolatile static RAM with a full-function real-time clock (RTC), alarm, watchdog timer, and interval timer that are all accessible in a byte-wide format. The DS1386 contains a lithium energy source and a quartz crystal, which eliminates the need for any external circuitry. Data contained within 8k or 32k by 8-bit memory and the timekeeping registers can be read or written in the same manner as byte-wide static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMified timekeeper by intelligent control circuitry, which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V_{CC}. Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year.

The RAMified timekeeper operates in either 24-hour or 12-hour format with an AM/PM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real-time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC operate when the system is powered down. Either can provide system "wake-up" signals.

FEATURES

- **8kB or 32kB of User NV RAM**
- **Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit, and Lithium Energy Source**
- **Totally Nonvolatile With Over 10 Years of Operation in the Absence of Power**
- **Watchdog Timer Restarts an Out-Of-Control Processor**
- **Alarm Function Schedules Real-Time Related Activities such as System Wakeup**
- **Programmable Interrupts and Square-Wave Output**
- **All Registers are Individually Addressable via the Address and Data Bus**
- **Interrupt Signals are Active in Power-Down Mode**

Pin Configurations appear at end of data sheet.

ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK
DS1386-8-120	0°C to +70°C	5.0	32 EMOD (0.740″)	DS1386-8K-120
DS1386-8-120+	0°C to +70°C	5.0	32 EMOD (0.740″)	DS1386-8K+120
DS1386-32-120	0°C to +70°C	5.0	32 EMOD (0.740″)	DS1386-32K-120
DS1386-32-120+	0°C to +70°C	5.0	32 EMOD (0.740″)	DS1386-32K+120
DS1386P-8-120	0°C to +70°C	5.0	34 PowerCap*	DS1386P-8K-120
DS1386P-8-120+	0°C to +70°C	5.0	34 PowerCap*	DS1386P+8K-120
DS1386P-32-120	0°C to +70°C	5.0	34 PowerCap*	DS1386P-32K-120
DS1386P-32-120+	0°C to +70°C	5.0	34 PowerCap*	DS1386P+32K-120

+ Denotes a lead-free/RoHS-compliant device.

** DS9034PCX PowerCap required (must be ordered separately).*

PIN DESCRIPTION

PIN				NAME	FUNCTION
EMOD		PowerCap			
8k x 8	32k x 8	8k x 8	32k x 8		
1	1	34	34	$\overline{INTA}$	Active-Low Interrupt Output A (Open Drain)
2	2	1	1	$\overline{INTB}$	Active-Low Interrupt Output B (Open Drain)
3, 28	—	2, 3, 31, 32	2, 3	N.C.	No Connection
12	12	18	18	A0	Address Inputs
11	11	19	19	A1	
10	10	20	20	A2	
9	9	21	21	A3	
8	8	22	22	A4	
7	7	23	23	A5	
6	6	24	24	A6	
5	5	25	25	A7	
27	27	26	26	A8	
26	26	27	27	A9	
23	23	28	28	A10	
25	25	29	29	A11	
4	4	30	30	A12	
—	28	—	31	A13	
—	3	—	32	A14	
16	16	17	17	GND	Ground
13, 14, 15, 17–21	13, 14, 15, 17–21	16–9	16–9	DQ0, DQ1, DQ2, DQ3–DQ7	Data Input/Output
22	22	8	8	$\overline{CE}$	Active-Low Chip Enable
24	24	7	7	$\overline{OE}$	Active-Low Output Enable
29	29	6	6	$\overline{WE}$	Active-Low Write Enable
30, 32	30, 32	—	—	V_{CC}	+5V Power Supply
31	31	33	33	SQW	Square-Wave Output
—	—	4	4	$\overline{PFO}$	Active-Low Power-Fail Output
—	—			X1, X2	Crystal Connections
—	—			V_{BAT}	Battery Connection

PACKAGES

The DS1386 is available in two packages (32-pin encapsulated DIP module and 34-pin PowerCap module). The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1386P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

OPERATION—READ REGISTERS

The DS1386 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High), $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A14) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address-input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION—WRITE REGISTERS

The DS1386 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION

The RAMified Timekeeper provides full functional capability when V_{CC} is greater than 4.5V and write-protects the register contents at 4.25V typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1386 constantly monitors V_{CC}. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become "don't care." The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. However, it is important to insure that the pull-up resistors used with the interrupt pins are never pulled up to a value that is greater than V_{CC} + 0.3V. As V_{CC} falls below approximately 3.0V, a power-switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. It is also required to insure that during this time (battery backup mode), the voltage present at $\overline{INTA}$ and $\overline{INTB}$ (INTB) never exceeds 3.0V. During power-up, when V_{CC} rises above approximately 3.0V, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5V for a period of 200ms.

RAMIFIED TIMEKEEPER REGISTERS

The RAMified Timekeeper has 14 registers, which are 8 bits wide that contain all of the timekeeping, alarm, and watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations, which contain external (user-accessible) copies of the timekeeping data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 8 or 32kbytes of RAM and the 14 external timekeeping registers are accessed from the external address and data bus. Registers 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information, which is stored in these two registers, is in BCD. Registers E through 1FFF or 7FFF are user bytes and can be used to maintain data at the user's discretion.

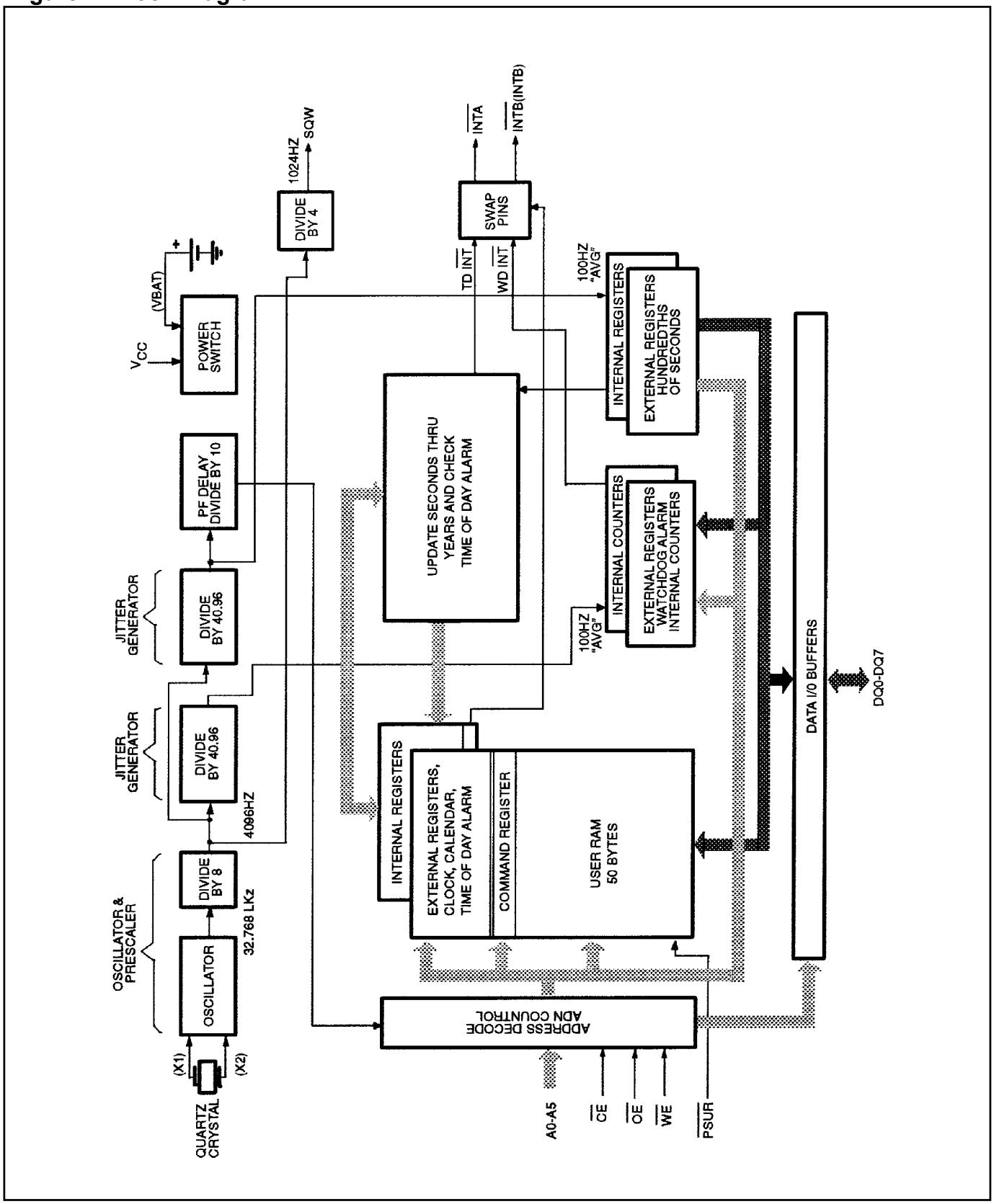
CLOCK ACCURACY (DIP MODULE)

The DS1386 is guaranteed to keep time accuracy to within ±1 minute per month at +25°C.

CLOCK ACCURACY (POWERCAP MODULE)

The DS1386P and DS9034PCX are each individually tested for accuracy. Once mounted together, the module is guaranteed to keep time accuracy to within ±1.53 minutes per month (35ppm) at +25°C.

Figure 1. Block Diagram



TIME-OF-DAY REGISTERS

Registers 0 through A contain time, date, and alarm data in BCD. Fifteen bits within these 11 registers are not used and will always read 0 regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic 0, $\overline{EOSC}$ (Bit 7) enables the RTC oscillator. This bit is set to logic 1 as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment (DIP Module only). This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the square wave output. When set to logic 0, the square wave output pin will output a 1024Hz square wave signal. When set to logic 1 the square wave output pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12- or 24-hour select bit. When set to logic 1, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). The Time of Day Registers are updated every 0.01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (transfer enable bit) to a logic 0. This will freeze the External Time of Day Registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic 1, will put the Time of Day Registers back to being updated every 0.01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the time of day alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

TIME-OF-DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read 0 regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Table 1). When all of the mask bits are logic 0, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic 1. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt are always cleared when Alarm Registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the watchdog alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the watchdog alarm to reinitialize and clears the watchdog flag bit and the watchdog interrupt output. When a new value is entered or the Watchdog Registers are read, the watchdog timer will start counting down from the entered value to zero. When zero is reached, the watchdog interrupt output will go to the active state. The watchdog timer countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the watchdog timer can prevent the watchdog alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual countdown register is internal and is not readable. Writing registers C and D to 0 will disable the watchdog alarm feature.

Figure 2. DS1386 RAMified Watchdog Timekeeper Registers

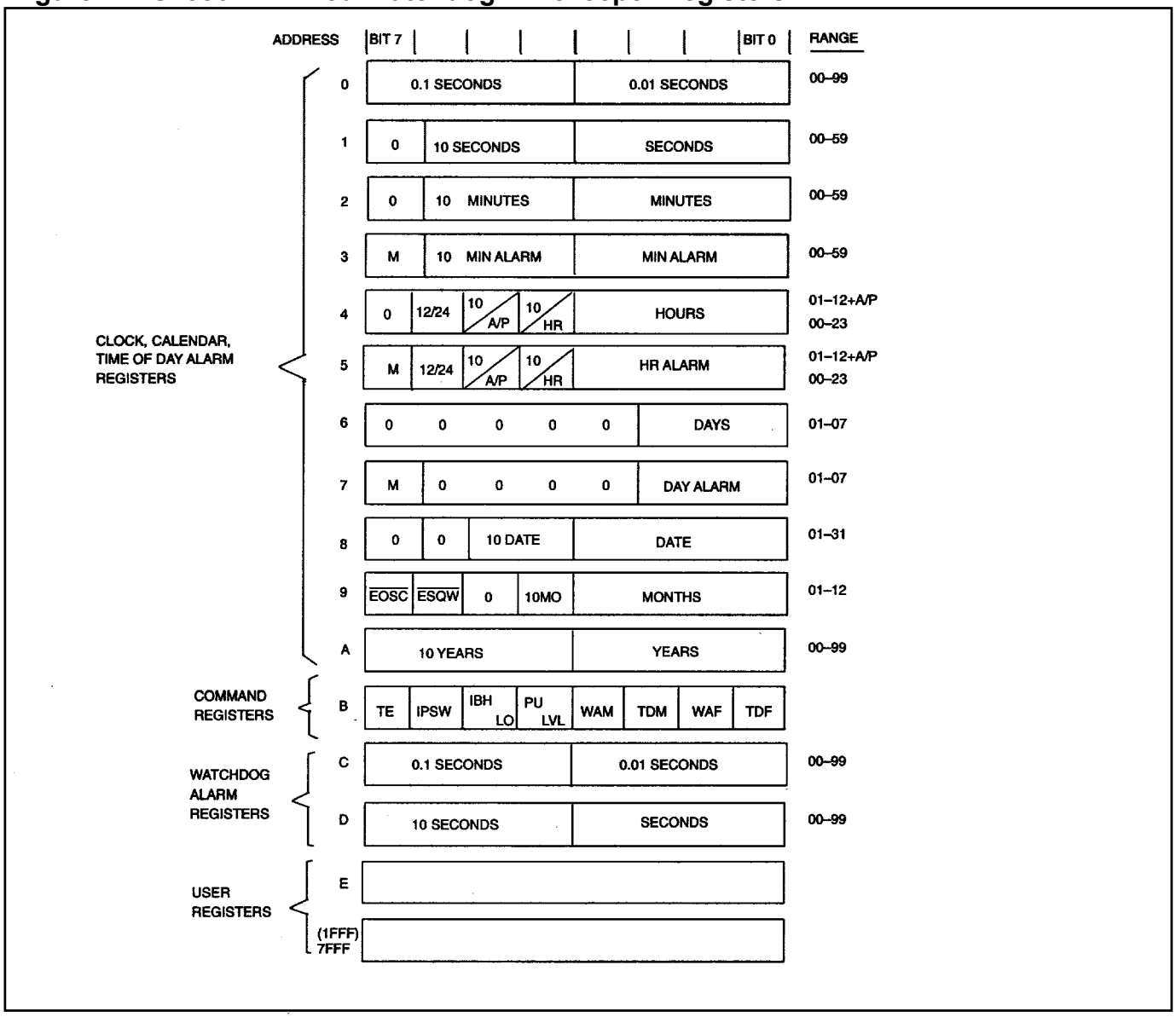


Table 1. Time-of-Day Alarm Mask Bits

REGISTER			DESCRIPTION
(3) MINUTES	(5) HOURS	(7) DAYS	
1	1	1	Alarm Once Per Minute
0	1	1	Alarm When Minutes Match
0	0	1	Alarm When Hours and Minutes Match
0	0	0	Alarm When Hours, Minutes and Days Match

Note: *Any other bit combinations of mask bit settings produce illogical operation.*

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

Bit 7: TE (Transfer Enable). This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

Bit 6: IPSW (Interrupt Switch). When set to a logic 1, $\overline{\text{INTA}}$ is the Time of Day Alarm and INTB/($\overline{\text{INTB}}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{\text{INTA}}$ is now the watchdog alarm output and INTB/($\overline{\text{INTB}}$) is the time of day alarm output.

Bit 5: IBH/LO (Interrupt B Sink or Source Current). When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{\text{INTB}}$) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

Bit 4: PU/LVL (Interrupt Pulse Mode or Level Mode). This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{\text{INTA}}$ and INTB/($\overline{\text{INTB}}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3ms and then release. INTB/($\overline{\text{INTB}}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3ms and then release. INTB will only source current when there is a voltage present on V_{CC}.

Bit 3: WAM (Watchdog Alarm Mask). When this bit is set to a logic 0, the watchdog interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the Command Register. When this bit is set to a logic 1, the watchdog interrupt output is deactivated.

Bit 2: TDM (Time-of-Day Alarm Mask). When this bit is set to a logic 0, the time of day alarm interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the Command Register. When this bit is set to a logic 1, the time of day alarm interrupt output is deactivated.

Bit 1: WAF (Watchdog Alarm Flag). This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only. The bit is reset when any of the watchdog alarm registers are accessed.
When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

Bit 0: TDF (Time-of-Day Flag). This is a read-only bit. This bit is set to a logic 1 when a time of day alarm has occurred. The time the alarm occurred can be determined by reading the time of day alarm registers. This bit is reset to a logic 0 state when any of the time of day alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +7.0V
Operating Temperature Range……...0°C to +70°C
Storage Temperature Range……...-40°C to +70°C
Soldering Temperature……..See IPC/JEDEC J-STD-020 Specification (See Note 14)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}			2.1	mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5	I_{CCS2}		2.0	4.0	mA	
Active Current	I_{CC}			85	mA	
Write Protection Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE

(T_A = 25°C)

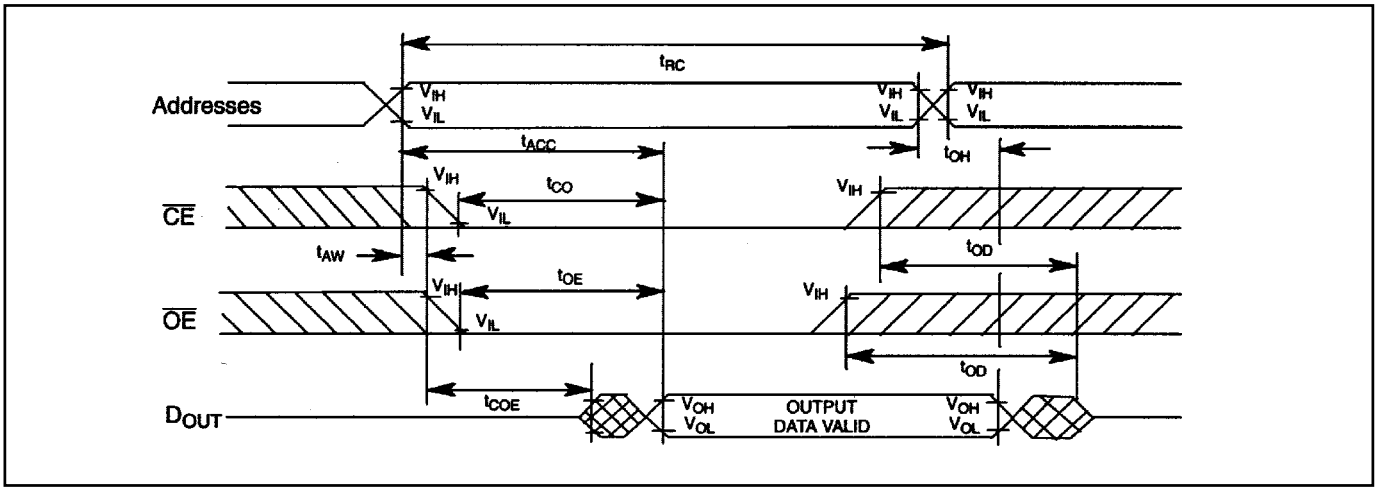
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	15	pF	
Output Capacitance	C_{OUT}		7	15	pF	
Input/Output Capacitance	$C_{I/O}$		7	15	pF	

AC ELECTRICAL CHARACTERISTICS

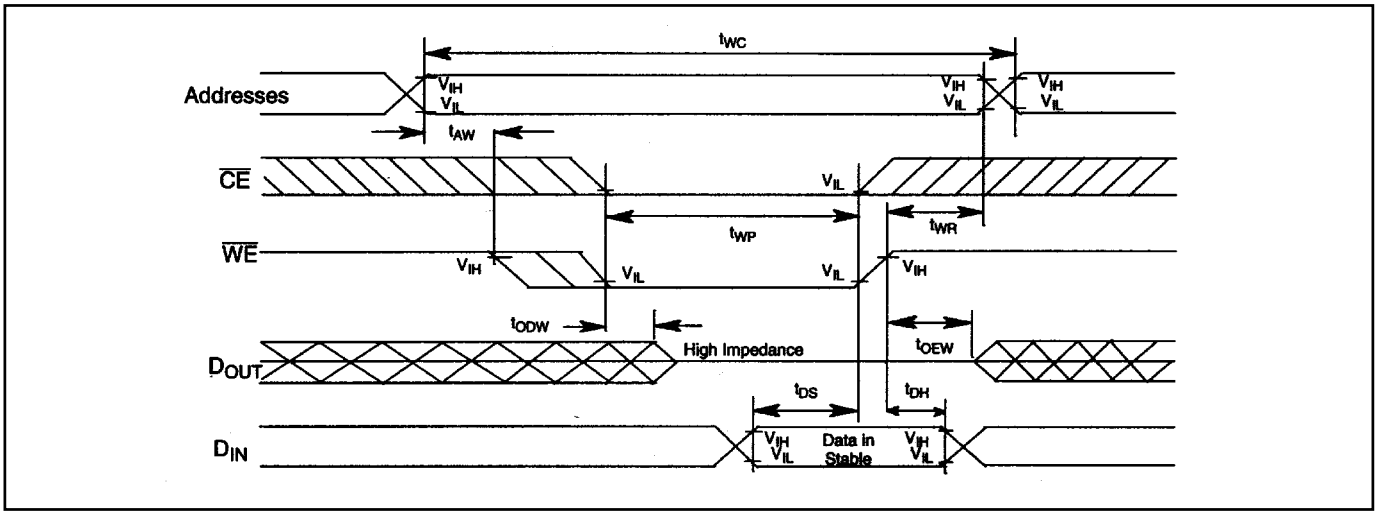
(V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	DS1386XX-120		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	120		ns	1
Address Access Time	t_{ACC}		120	ns	
$\overline{CE}$ Access Time	t_{CO}		120	ns	
$\overline{OE}$ Access Time	t_{OE}		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		ns	
Output High-Z from Deselect	t_{OD}		40	ns	
Output Hold from Address Change	t_{OH}	10		ns	
Write Cycle Time	t_{WC}	120		ns	
Write Pulse Width	t_{WP}	110		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	10		ns	
Output High-Z from $\overline{WE}$	t_{ODW}		40	ns	
Output Active from $\overline{WE}$	t_{OEW}	10		ns	
Data Setup Time	t_{DS}	85		ns	4
Data Hold Time	t_{DH}	10		ns	4, 5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3		ms	11, 12

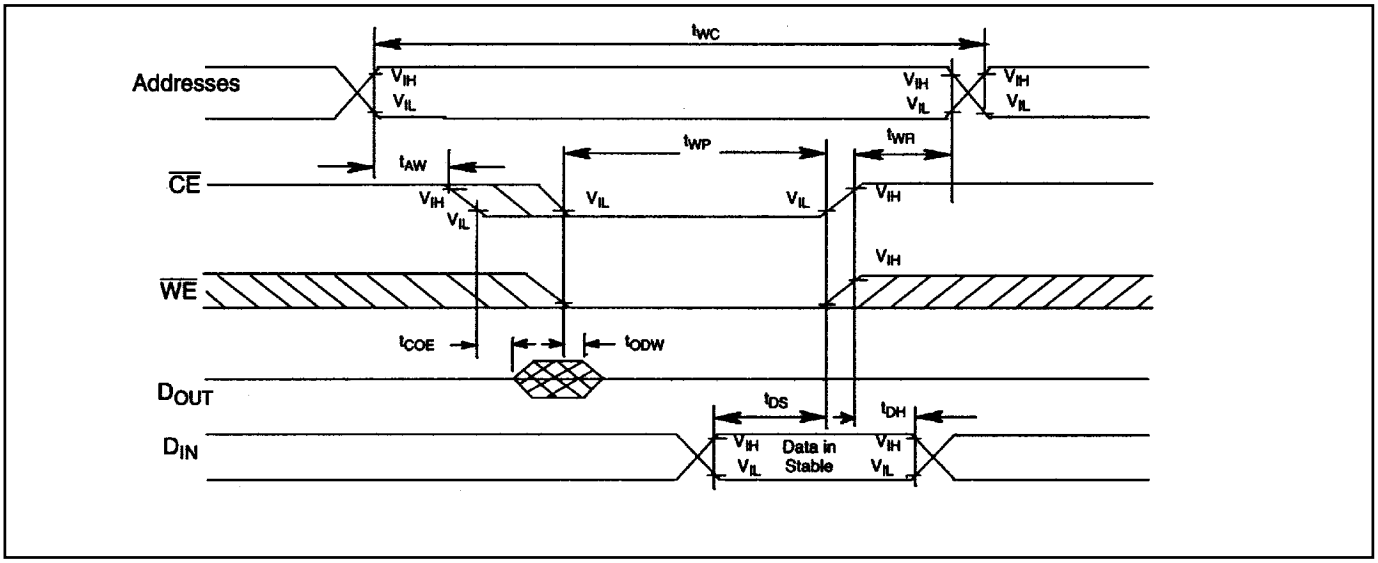
READ CYCLE (Note 1)



WRITE CYCLE 1 (Notes 2, 6, 7)

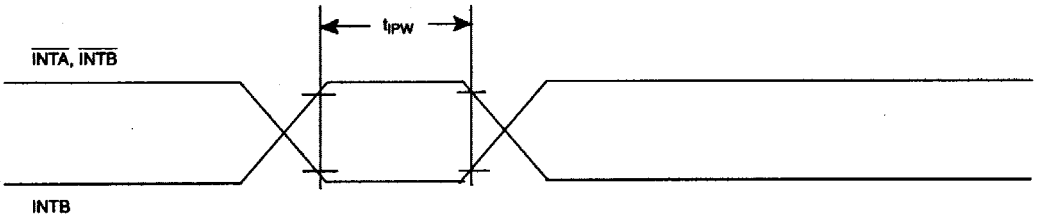


WRITE CYCLE 2 (Notes 2, 8)

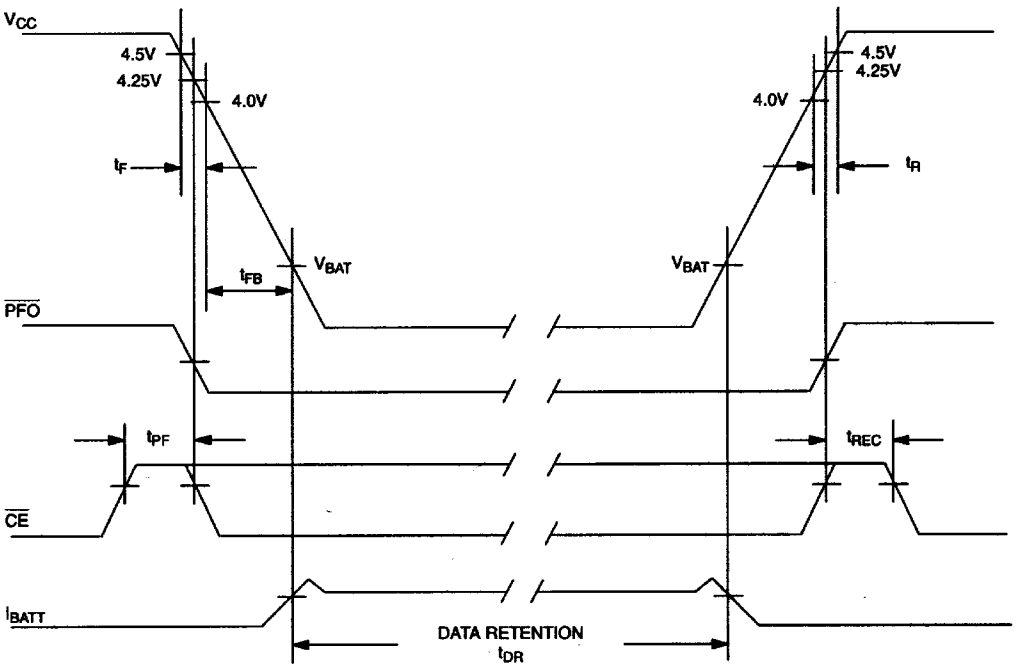


TIMING DIAGRAM—INTERRUPT OUTPUTS PULSE MODE

(See Notes 11 and 12)



POWER-DOWN/POWER-UP TIMING



AC ELECTRICAL CHARACTERISTICS POWER-UP/POWER-DOWN TIMING

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}		0	ns	
Recovery at Power-Up	t_{REC}		200	ms	
V_{CC} Slew Rate Power-Down	t_F $4.0 \le V_{CC} \le 4.5V$	300		µs	
V_{CC} Slew Rate Power-Down	t_{FB} $3.0 \le V_{CC} \le 4.25V$	10		µs	
V_{CC} Slew Rate Power-Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0		µs	
Expected Data Retention	t_{DR}	10		Years	9

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

NOTES:

1) $\overline{WE}$ is high for a read cycle.
2) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3) t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4) t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5) t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20ns for -120 parts and t_{DH} = 25ns for -150 parts.
6) If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9) Each DS1386 is marked with a four-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined for DIP modules as starting at the date of manufacture.
10) All voltages are referenced to ground.
11) Applies to both interrupt pins when the alarms are set to pulse.
12) Interrupt output occurs within 100ns on the alarm condition existing.
13) Both $\overline{INTA}$ and INTB ($\overline{INTB}$) are open-drain outputs.
14) Real-Time Clock modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

    In addition, for the PowerCap version:
    a. Dallas Semiconductor recommends that PowerCap module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
    b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.

AC TEST CONDITIONS

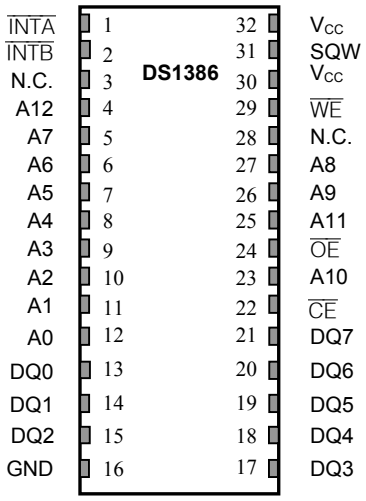
Input Levels: 0V to 3V
Transition Times: 5ns

AC TEST CONDITIONS

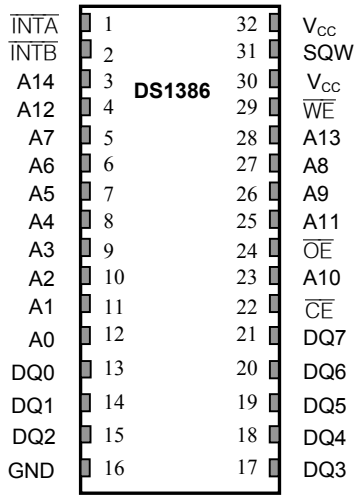
Output Load: 50pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

PIN CONFIGURATIONS

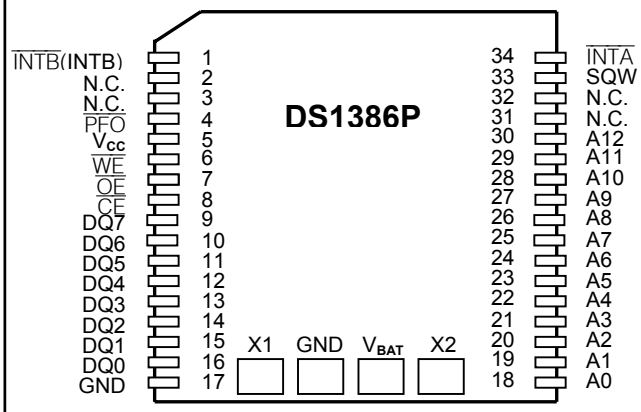
TOP VIEW



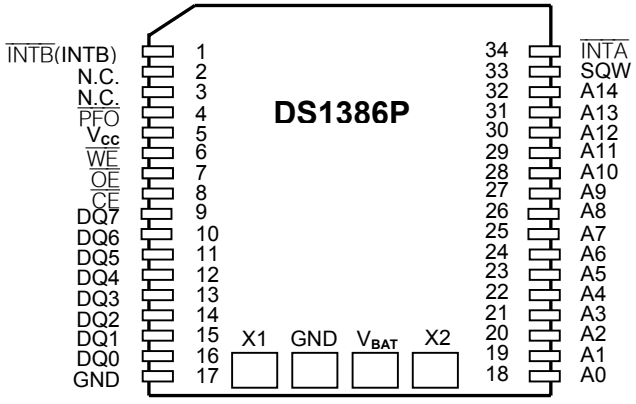
8k x 8
Encapsulated Module



32k x 8
Encapsulated Module



8k x 8
PowerCap® Module Board
(Uses DS9034PCX PowerCap)

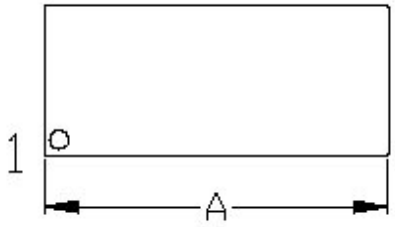


32k x 8
PowerCap Module Board
(Uses DS9034PCX PowerCap)

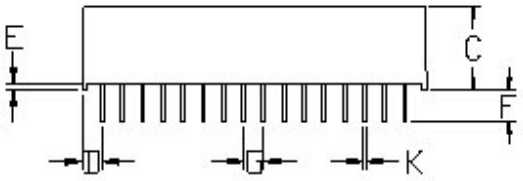
PACKAGE INFORMATION

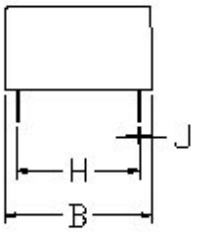
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECN 35439		



Some pins may be missing by design





ALL DIMENSIONS ARE IN INCHES. See page 2 for dimensions in mm

	24 PIN 720		28 PIN 720,740		32 PIN 740		36 PIN 740		40 PIN 740	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	1.100	1.500	1.460	1.550	1.650	1.740	2.070	2.120	2.070	2.120
C	0.320	0.420	0.320	0.420	0.350	0.430	0.370	0.430	0.370	0.430
D	0.080	0.130	0.080	0.130	0.080	0.130	0.180	0.210	0.080	0.130

	MIN	MAX	
B	0.680	0.720	ALL 720 PACKAGES
B	0.720	0.740	ALL 740 PACKAGES

	ALL PACKAGES	
	MIN	MAX
E	0.010	0.040
F	0.120	0.160
G	0.090	0.110
H	0.590	0.630
J	0.008	0.012
K	0.015	0.021

SIGNATURE	DATE
RMA	2/03

DIP_ModulesPCB.SLDDRW

DALLAS SEMICONDUCTOR MAXIM

TITLE: Marketing Outline
Encapsulated Modules and Clocks

CODE	PROD NO	PART NO.	REV.
A		56-G0002-001	A

SCALE: N/A SHEET 1 of 2

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECN 35439		

ALL DIMENSIONS ARE IN MM

	24 PIN 720		28 PIN 720,740		32 PIN 740		36 PIN 740		40 PIN 740	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	27.94	38.10	37.08	39.37	41.91	44.20	52.58	53.85	52.58	53.85
C	8.13	10.67	8.13	10.67	8.89	10.92	9.40	10.92	9.40	10.92
D	2.03	3.30	2.03	3.30	2.03	3.30	4.57	5.33	2.03	3.30

	MIN	MAX	
B	17.27	18.29	ALL 720 PACKAGES
B	18.29	18.80	ALL 740 PACKAGES

	ALL PACKAGES	
	MIN	MAX
E	0.25	1.02
F	3.05	4.06
G	2.29	2.79
H	14.99	16.00
J	0.20	0.30
K	0.38	0.53

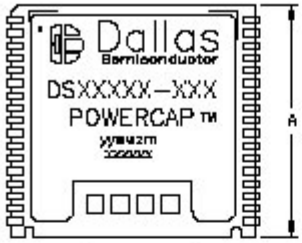
DALLAS MAXIM	SIZE A	FSCM NO	DWG NO. 56-G0002-001	REV A
	SCALE N/A		SHEET 2 OF 2	

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

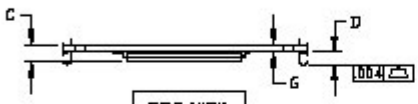
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	New drawing	11/04	JW

PowerCap™ Module Base

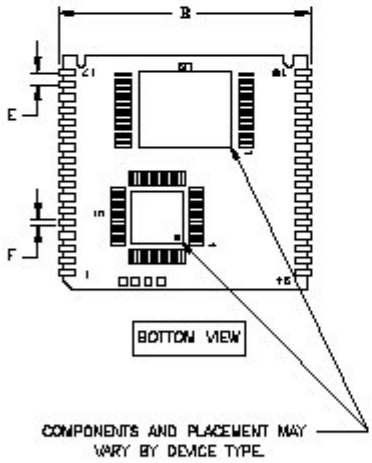


TOP VIEW

PKG	INCHES		
DIM	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.980	0.985	0.995
C	—	—	0.080
D	0.050	0.055	0.060
E	0.047	0.050	0.053
F	0.015	0.020	0.025
G	0.024	0.027	0.032



SIDE VIEW



BOTTOM VIEW

Notes:

1. Dallas Semiconductor recommends that PowerCap module bases experience one pass through solder reflow, oriented with the label side up ('live bug').
2. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad, and apply solder.
3. To remove the part, apply flux, heat the lead frame pad until the solder melts, then use solder wick to remove the solder.

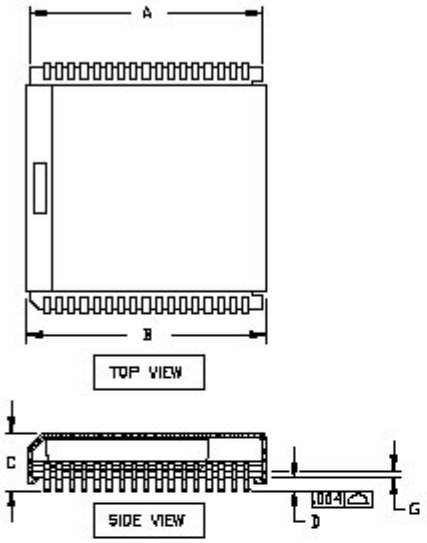
SIGNATURE	DATE	DALLAS SEMICONDUCTOR MAXIM
DOC. CONTROL:		
ENGR. MGR:		TITLE PowerCap™ .990 34 Pin PowerCap™ Module
MFG. ENGR:		
CHECKED BY:		
DRAWN BY: M.ZUCCO	11/04	SIZE A · FSCM NO · DWG NO. 56-G0003-001 · REV A
DIP_Modules1C.GL.00PW		SCALE N/A · SHEET 1 OF 3

PACKAGE INFORMATION (continued)

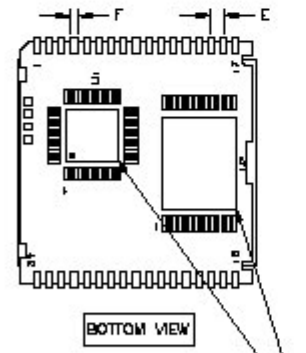
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

DWG 56-G0003-001 ZH REV 2 A

PowerCap™ Base with DS9034PCX Attached



PKG	INCHES		
DIM	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.950	0.960	0.970
C	0.240	0.255	0.270
D	0.050	0.055	0.060
E	0.047	0.050	0.053
F	0.015	0.020	0.025
G	0.024	0.027	0.032



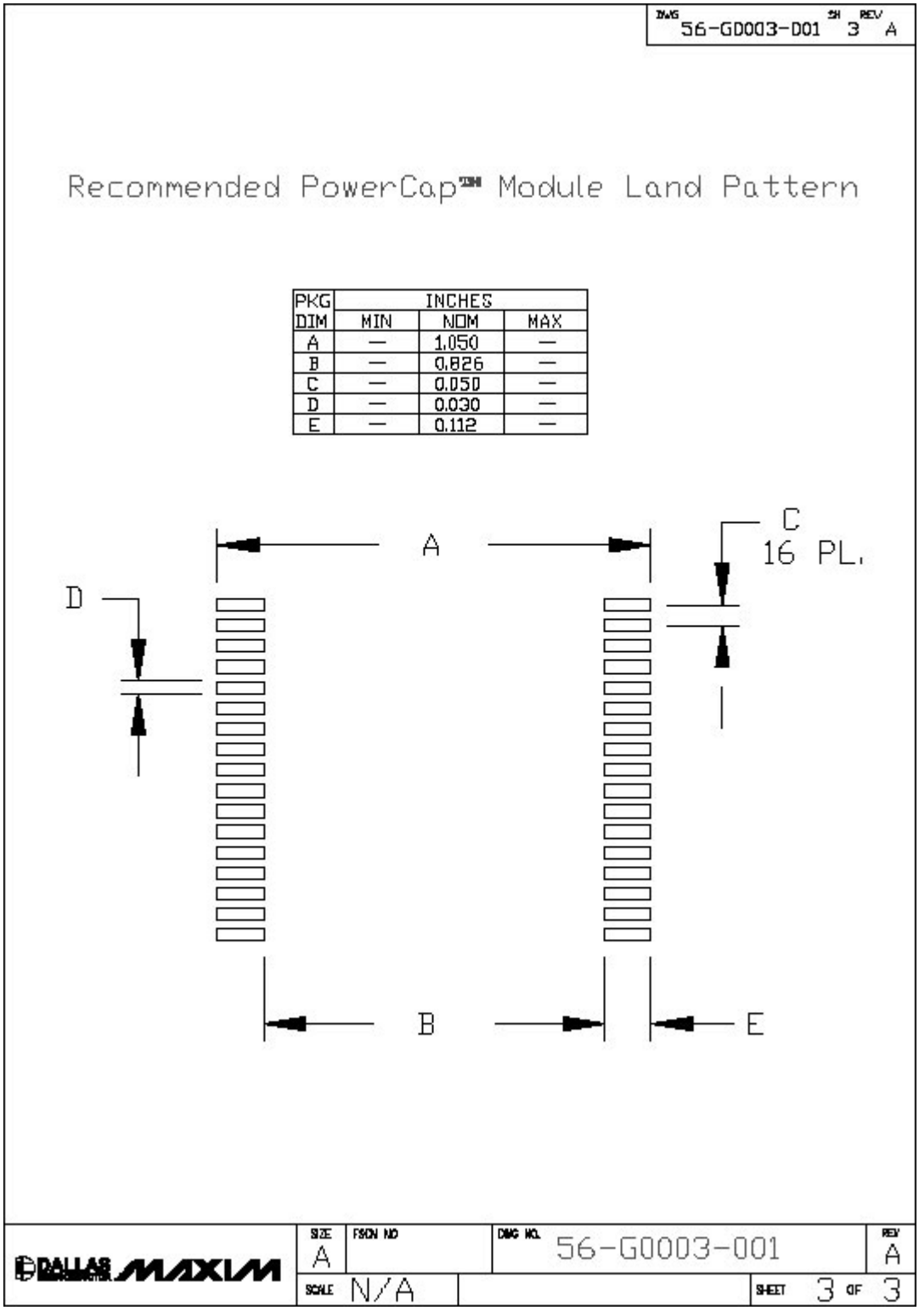
COMPONENTS AND PLACEMENT MAY VARY BY DEVICE TYPE.

Notes:
1. The DS9034PCX cap contains a lithium battery. Do not exceed 80°C.
2. Remove the cap before touching up the base.
3. If the base is washed, remove the cap before washing
4. If the base is washed, make sure it is dry before attaching the cap

DALLAS MAXIM	SIZE A	FSCM NO	DWG NO. 56-G0003-001	REV A
	SCALE N/A		SHEET 2 OF 3	

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



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- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А