

N-channel 25 V 0.99 m Ω logic level MOSFET in LFPAK using NextPower technology

Rev. 2 — 4 July 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD and QOSS for high system efficiencies at low and high loads
- Ultra low Rdson and low parasitic inductance

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching

- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	25	V
I_D	drain current	T _{mb} = 25 °C; see <u>Figure 1</u>	[1]	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	272	W
Tj	junction temperature			-55	-	175	°C
Static chara	acteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{}$		-	0.95	1.25	mΩ
		$V_{GS} = 10 \text{ V; } I_{D} = 25 \text{ A;}$ $T_{j} = 25 \text{ °C; see } \frac{\text{Figure 12}}{\text{ or } 12}$		-	0.75	0.99	mΩ



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Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic c	haracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 12 \text{ V}; \text{ see } \frac{\text{Figure 14}}{\text{see } \frac{\text{Figure 15}}{\text{Figure 15}}};$	-	14	-	nC
Q _{G(tot)}	total gate charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 12 \text{ V}; \text{ see } \frac{\text{Figure 15}}{\text{Figure 14}};$	-	51	-	nC

^[1] Continuous current is limited by package

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		5
2	S	source	mb	D
3	S	source		
4	G	gate	9	
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S S

SOT669 (LFPAK; Power-SO8)

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN0R9-25YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669		

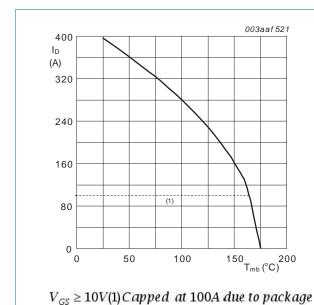
Limiting values

Limiting values Table 4.

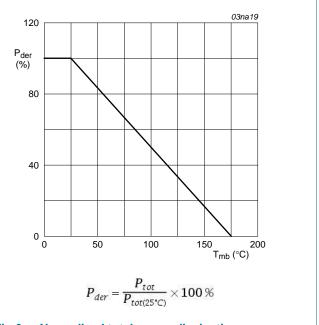
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	25	V
V_{DGR}	drain-gate voltage	$25 \text{ °C} \le T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	25	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	T _{mb} = 25 °C; see <u>Figure 1</u>	[1]	-	100	Α
		T _{mb} = 100 °C; see <u>Figure 1</u>	[1]	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 4		-	1563	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	272	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		920	-	V
Source-drain	n diode					
Is	source current	T _{mb} = 25 °C	<u>[1]</u>	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1563	Α
Avalanche r	uggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 25 V; unclamped; R_{GS} = 50 Ω; see <u>Figure 3</u>		-	342	mJ

[1] Continuous current is limited by package



Continuous drain current as a function of mounting base temperature



Normalized total power dissipation as a function of mounting base temperature

PSMN0R9-25YLC

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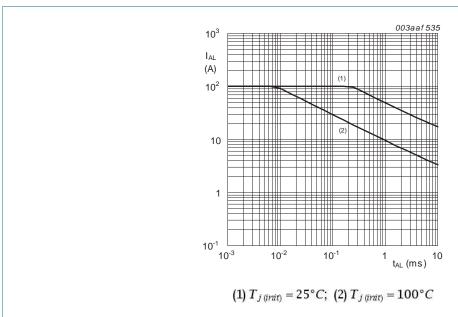
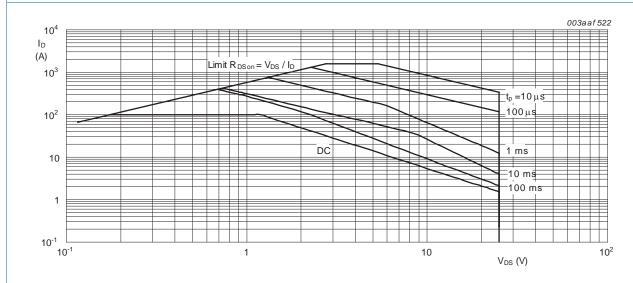


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



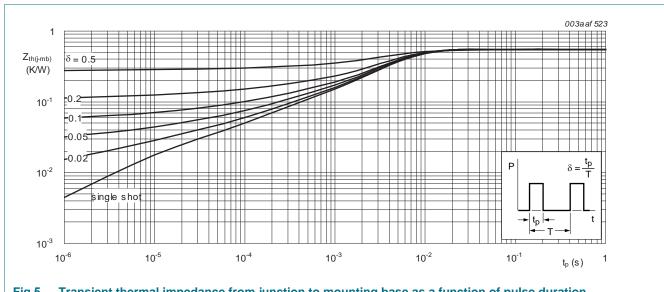
 $T_{mb} = 25$ °C; I_{DM} is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Thermal characteristics

Table 5. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.45	0.55	K/W



Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics	Canditions	N#!	T	Marr	1114
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	racteristics					
$V_{(BR)DSS}$	drain-source breakdown	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	25	-	-	V
	voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 10</u>	1.05	1.41	1.95	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; see <u>Figure 11</u>	-	-	2.25	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C}$	0.5	-	-	V
l _{DSS} drain leakage current	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μA
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 12	-	0.95	1.25	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 °C;$ see Figure 12; see Figure 13	-	-	2.125	mΩ
	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12	-	0.75	0.99	mΩ	
	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 ^{\circ}\text{C};$ see Figure 12; see Figure 13	-	-	1.68	mΩ	
R_{G}	internal gate resistance (AC)	f = 1 MHz	-	1.1	2.2	Ω
Dynamic o	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	110	-	nC
		I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 15; see Figure 14	-	51	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	104	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V;	-	14.8	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see Figure 14; see Figure 15	-	10.5	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	4.4	-	nC
Q_{GD}	gate-drain charge		-	14	-	nC
V _{GS(pl)}	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; see Figure 14; see Figure 15	-	2.4	-	V
C _{iss}	input capacitance	$V_{DS} = 12 \text{ V; } V_{GS} = 0 \text{ V; } f = 1 \text{ MHz;}$	-	6775	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	1437	-	pF

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Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{d(on)}	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 4.5 \text{ V};$	-	42.5	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	74	-	ns
t _{d(off)}	turn-off delay time		-	103.5	-	ns
t _f	fall time		-	55	-	ns
Q _{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 12 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	31.57	-	nC
Source-drain	n diode					
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 17	-	8.0	1.1	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	48	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 12 \text{ V}$	-	60	-	nC
ta	reverse recovery rise time	$V_{GS} = 0 \text{ V; } I_S \text{ 25 A;}$ $dI_S/dt = -100 \text{ A/}\mu\text{s; } V_{DS} = 12 \text{ V;}$ see Figure 18	-	26.3	-	ns
t _b	reverse recovery fall time	$V_{GS} = 0 \text{ V; } I_S = 25 \text{ A;}$ $dI_S/dt = -100 \text{ A/µs; } V_{DS} = 12 \text{ V;}$ see Figure 18	-	21.7	-	ns

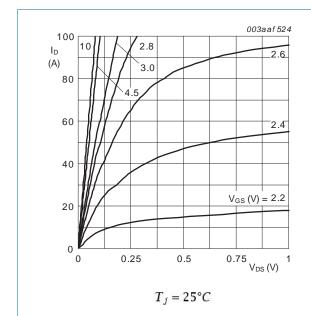
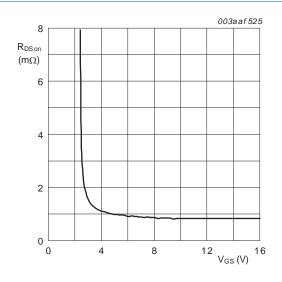


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



 $T_j = 25^{\circ}C; I_D = 25A$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

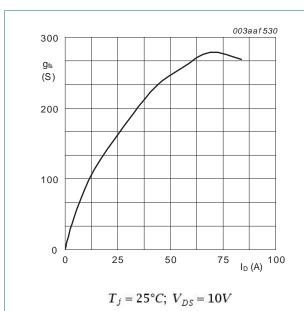


Fig 8. Forward transconductance as a function of drain current; typical values

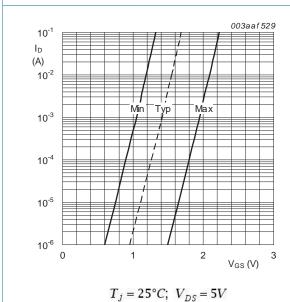


Fig 10. Sub-threshold drain current as a function of gate-source voltage

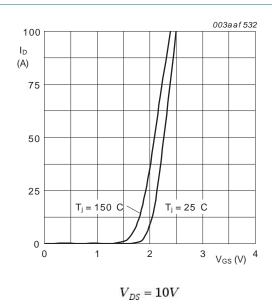


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

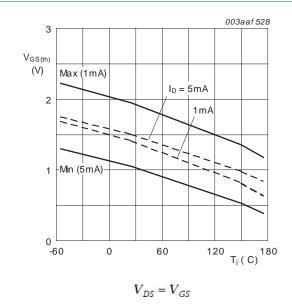


Fig 11. Gate-source threshold voltage as a function of junction temperature

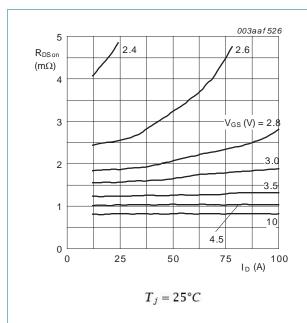


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

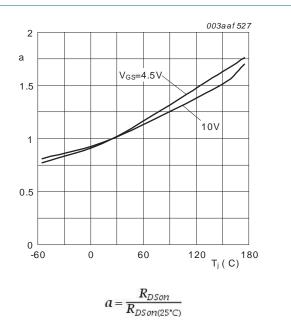


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

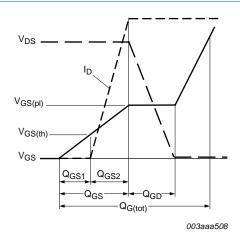


Fig 14. Gate charge waveform definitions

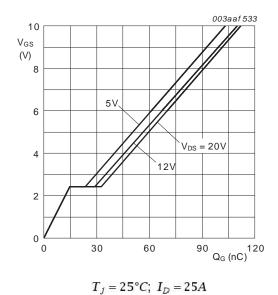


Fig 15. Gate-source voltage as a function of gate charge; typical values

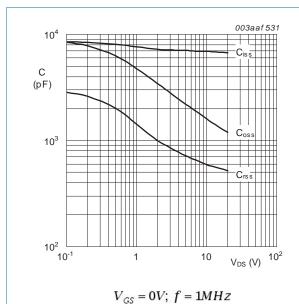


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

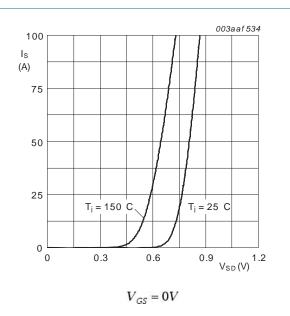


Fig 17. Source current as a function of source-drain voltage; typical values

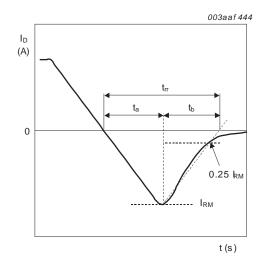
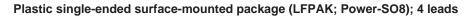
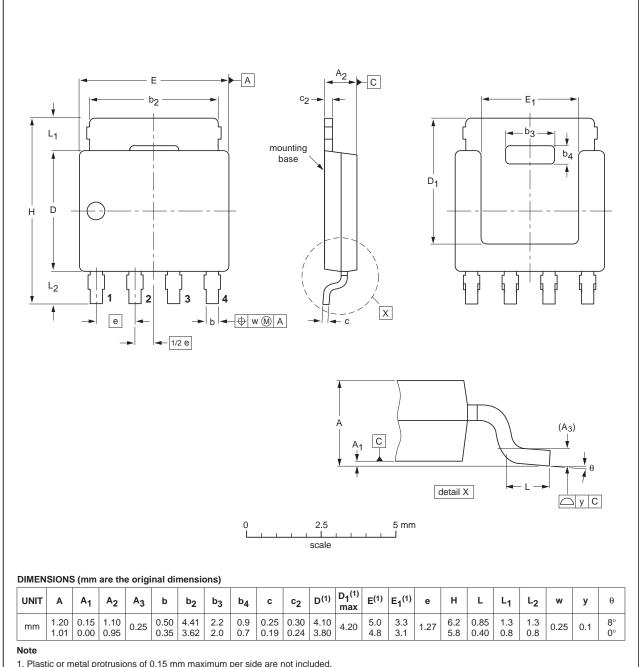


Fig 18. Reverse recovery timing definition

Package outline



SOT669



1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT669		MO-235			06-03-16 11-03-25

Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

PSMN0R9-25YLC

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N-channel 25 V 0.99 mΩ logic level MOSFET in LFPAK using NextPower technology

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN0R9-25YLC v.2	20110704	Product data sheet	-	PSMN0R9-25YLC v.1
Modifications:	 Various changes to 	content.		
PSMN0R9-25YLC v.1	20101202	Product data sheet	-	-

N-channel 25 V 0.99 mΩ logic level MOSFET in LFPAK using NextPower technology

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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Nexperia

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- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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