GENERAL DESCRIPTION

The XRT75VL00 is a single-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/ DS3/STS-1 applications. It incorporates an independent Receiver, Transmitter and Jitter Attenuator in a single 52 pin TQFP package.

The XRT75VL00 can be configured to operate in either E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) modes. The transmitter can be turned off (tri-stated) for redundancy support and for conserving power.

The XRT75VL00's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75VL00 incorporates an advanced crystal-less jitter attenuator that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75VL00 provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75VL00 supports local, remote and digital loop-backs. The XRT75VL00 also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements.
- Detects and Clears LOS as per G.775.
- Meets Bellcore GR-499 CORE Jitter Transfer Requirements.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards.
- Meets ETSI TBR 24 Jitter Transfer Requirements.
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled.
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock.
- Provides low jitter output clock.

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitter can be turned on or off.

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuator can be selected in Receive or Transmit paths.
- 16 or 32 bits selectable FIFO size.
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards.
- Jitter Attenuator can be disabled.

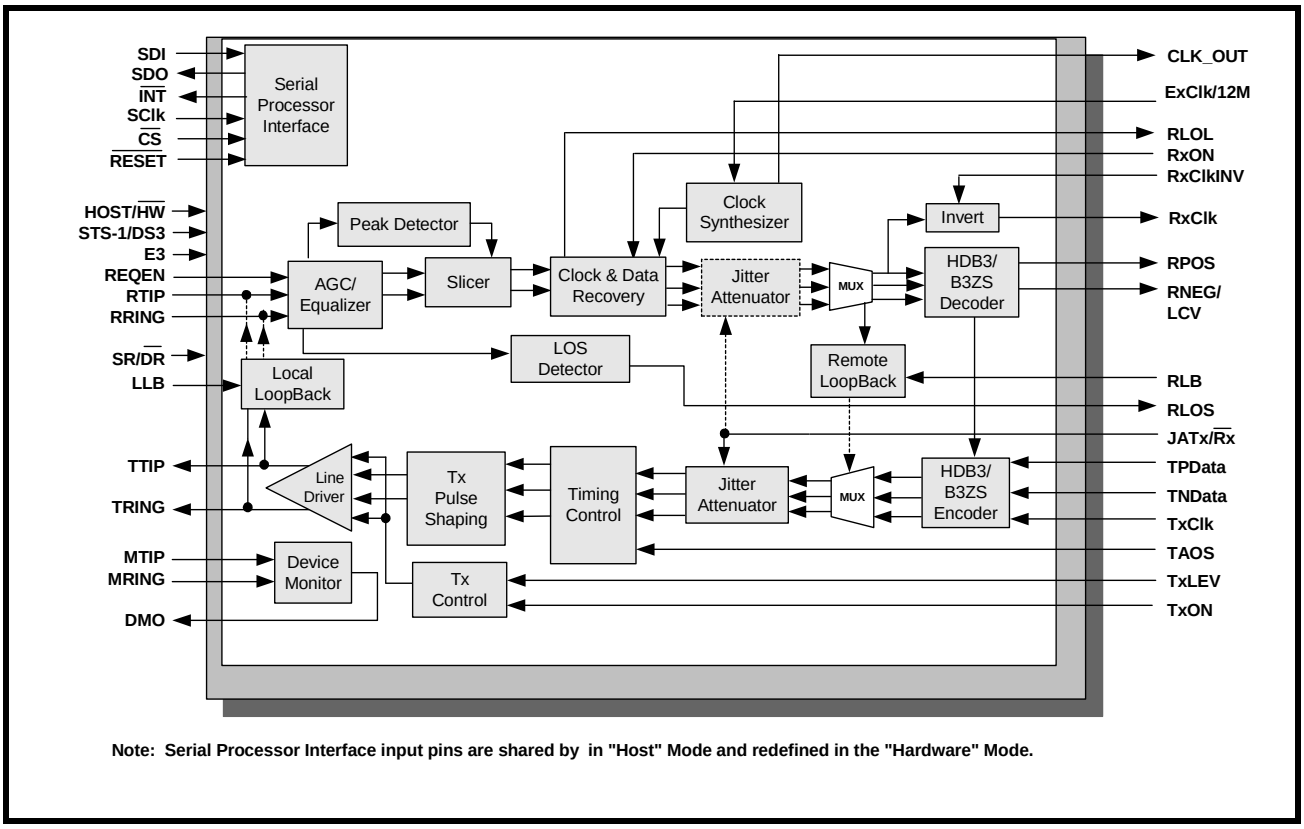
CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration.
- Supports optional internal Transmit Driver Monitoring.
- PRBS error counter register to accumulate errors.
- Hardware Mode for control and configuration.
- Supports Local, Remote and Digital Loop-backs.
- Single 3.3 V ± 5% power supply.
- 5 V Tolerant I/O.
- Available in 52 pin TQFP.
- -40℃ to 85℃ Industrial Temperature Range.

APPLICATIONS

- E3/DS3 Access Equipment.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.
- Fiber Optic Terminals.

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75VL00



Note: Serial Processor Interface input pins are shared by in "Host" Mode and redefined in the "Hardware" Mode.

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled).
- Accepts Transmit Clock with duty cycle of 30%-70%.
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications.
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993.
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE.
- Transmitter can be turned off in order to support redundancy designs.

RECEIVE INTERFACE CHARACTERISTICS

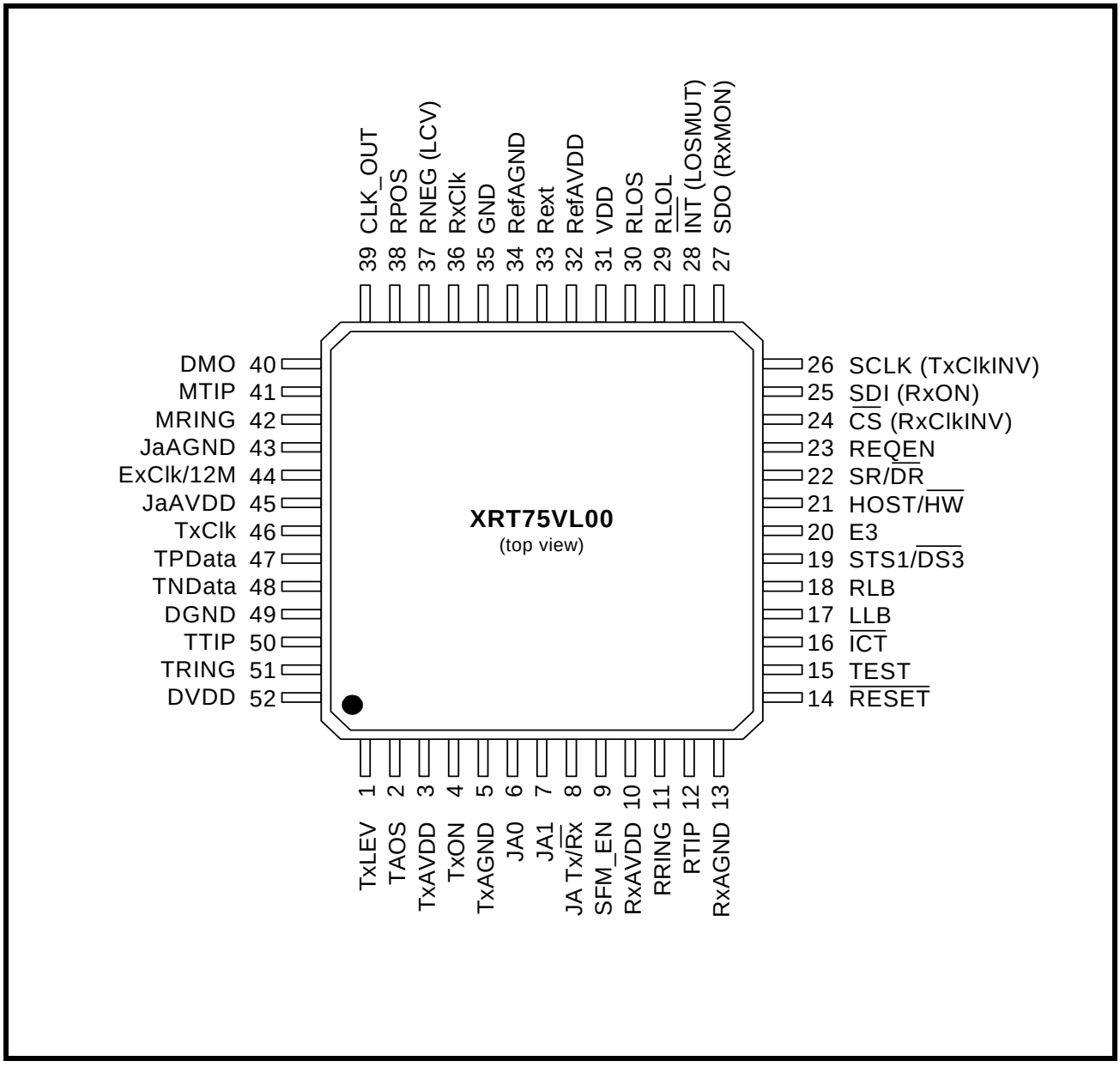
- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery.
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications.
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications.
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications.
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms.
- Built-in B3ZS/HDB3 Decoder (which can be disabled).
- Recovered Data can be muted while the LOS Condition is declared.

- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment.

JITTER ATTENUATORS

The XRT75VL00 includes a Jitter Attenuator that meets the Jitter requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards. In addition, the jitter attenuator also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards.

FIGURE 2. PIN OUT OF THE XRT75VL00



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75VL00IV	52 Pin TQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
4	TxON	I	**Transmitter ON Input** Setting this input pin "High" turns on the Transmitter. ***NOTES:*** *1. Even when the XRT75VL00 is configured in HOST mode, this pin still controls the TTIP and TRING outputs* *2. When the Transmitter is turned off either in Host or Hardware mode,the TTIP and TRING outputs are Tri-stated.* *3. This pin is internally pulled down*
46	TxClk	I	**Transmit Clock Input for TPData and TNData** The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%. The XRT75VL00 samples the TPData and TNData pins on the falling or rising edge of TxClk signal based on the status of TxClkINV pin (in Hardware mode) or the status of the bit in the Channel Register (in HOST mode).
26	TxClkINV/ SClk	I	**Transmit Clock Invert or Serial Clock Input:** Function of this depends on whether the XRT75VL00 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin “High” configures the Transmitter to sample the TPData and TNData data on the rising edge of the TxClk. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as SClk input pin (please refer to the pin description for Microprocessor interface).*
48	TNData	I	**Transmit Negative Data Input** If the XRT75VL00 is configured in Dual-rail mode, this pin is sampled on the falling or rising edge of TxClk based on the status of the TClkINV pin (in Hardware mode) or the status of the control bit in the Channel Register (in HOST mode). ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.*
47	TPData	I	**Transmit Positive Data Input** The XRT75VL00 samples this pin on the falling or rising edge of TxClk based on the status of the TClkINV pin (in Hardware mode) or the status of the control bit in the Channel Register (in HOST mode).
50	TTIP	O	**Transmit TTIP Output** The XRT75VL00 uses this pin along with TRING to transmit a bipolar signal to the line using a 1:1 transformer.

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
51	TRING	O	**Transmit Ring Output** The XRT75VL00 uses this pin along with TTIP to transmit a bipolar signal to the line using a 1:1 transformer.
1	TxLEV	I	**Transmit Line Build-Out Enable/Disable Select** This input pin is used to enable or disable the Transmit Line Build-Out circuit. Setting this pin to "High" disables the Line Build-Out circuit. In this mode, partially-shaped pulses are output onto the line via the TTIP and TRING output pins. Setting this pin to "Low" enables the Line Build-Out circuit. In this mode, shaped pulses are output onto the line via the TTIPand TRING output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this pin to "1" if the cable length between the Cross-Connect and the transmit output is greater than 225 feet. 2. Set this pin to "0" if the cable length between the Cross-Connect and the transmit output is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT75VL00 is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT75VL00 is configured to operate in the Hardware Mode. ***NOTES:*** *1. This pin is internally pulled down.* *2. If the XRT75VL00 is configured in HOST mode, this pin may be tied to GND.*

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
25	RxON/ SDI	I	**Receiver Turn ON Input or Serial Data Input:** Function of this pin depends on whether the XRT75VL00 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" turns on and enables the Receiver.. ***NOTES:*** *1. If the XRT75VL00 is configured in HOST mode, this pin functions as SDI input pin (please refer to the pin description for Microprocessor Interface)* *2. This pin is internally pulled down.*
23	REQEN	I	**Receive Equalization Enable Input** Setting this input pin "High" enables the Internal Receive Equalizer. Setting this pin "Low" disables the Internal Receive Equalizer. ***NOTES:*** *1. This input pin is ignored and may be connected to GND if the XRT75VL00 is operating in the HOST Mode* *2. This pin is internally pulled down.*
36	RxClk	O	**Receive Clock Output** The Recovered Clock signal from the incoming line signal is output through this pin.By default, the Receiver Section outputs data via RPOS and RNEG pins on the rising edge of this clock signal. Configure the Receiver Section to update data on the RPOS and RNEG pins on the falling edge of RxClk by doing the following: a) **Operating in Hardware mode**, pull the RxClkINV pin to "High". b) **Operating in Host mode**, write a "1" to RxClkINV bit field within the Receive Control Register.
24	RxClkINV/ $\overline{CS}$	I	**RxClk INVERT or Chip Select**: Function of this pin depends on whether the XRT75VL00 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures the Receiver Section to invert the RxClk output signals and outputs the recovered data via RPOS and RNEG on the falling edge of RxClk. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as CS input pin (please refer to the pin description for Microprocessor Interface).*
38	RPOS	O	**Receive Positive Data Output** This output pin pulses "High" whenever the XRT75VL00 has received a Positive Polarity pulse in the incoming line signal at the RTIP/RRing inputs.

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
37	RNEG/LCV	O	**Receive Negative Data Output/Line Code Violation Indicator** **Function of these pins depends on whether the XRT75VL00 is configured in Single Rail or Dual Rail mode.** If the XRT75VL00 is configured in Dual Rail mode, a negative pulse is output through RNEG. **In Hardware mode:** Tie the pin SR/$\overline{DR}$ (pin 22) "High" to configure the XRT75VL00 in Single Rail mode and tie "Low" to configure in Dual Rail mode. **In HOST mode:** XRT75VL00 can be configured in Single Rail or Dual Rail by setting or clearing the bit in the block control register. **Line Code Violation Indicator** If the XRT75VL00 is configured in Single Rail mode then: Whenever the Receiver Section detects a Line Code violation, it pulses this output pin "High". This output pin remains "Low" at all other times. It is advisable to sample this output pin using the RxClk output signal.
11	RRING	I	**Receive Ring Input** This input pin along with RTIP is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
12	RTIP	I	**Receive TIP Input** This input pin along with RRNG is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
27	RxMON/ SDO	I	**Receive Monitoring Mode or Serial Data Output:** In Hardware mode, when this pin is tied "High" XRT75VL00 configures into monitoring channel. In the monitoring mode, the Receiver is capable of monitoring the signals with 20 dB flat loss plus 6 dB cable attenuation. This allows to monitor very weak signal before declaring LOS. In HOST Mode, XRT75VL00 can be configured to be a monitoring channel by setting the bits in the receive control register. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as SDO pin (please refer to the pin description for the Microprocessor Interface).*

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
44	ExClk/12M	I	**Clock Input (34.368 MHz or 44.736 MHz or 51.84 MHz ± 20 ppm):** Based on the mode selected, provide the appropriate reference clock signal. If the XRT75VL00 is configured for Single Frequency Mode with the SFM_EN tied "High", then provide a 12.288 MHz ± 20 ppm clock and depending on the mode, the correct frequency is generated internally by the clock synthesizer..
9	SFM_EN	I	**Single Frequency Enable:** Tie this pin "High" to select the single frequency mode. When enabled, a single frequency clock, 12.288 MHz is input through the ExClk input pin and the internal clock synthesizer generates the appropriate clock frequency. ***NOTE:*** *This pin is internally pulled down.*
39	CLK_OUT	O	**Clock out put:** When the Single Frequency Mode is selected, a low jitter clock will be out put. The frequency of this clock depends on whether the XRT75VL00 is configured in E3 or DS3 or STS-1 mode.

OPERATING MODE SELECT

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
21	HOST/($\overline{HW}$)	I	**HOST/Hardware Mode Select:** Tie this pin "High" to configure the XRT75VL00 in HOST mode. Tie this "Low" to configure in Hardware mode. When the XRT75VL00 is configured in HOST mode, the states of many discrete input pins are ignored. ***NOTE:*** *This pin is internally pulled up.*
20	E3	I	**E3 Mode Select Input** A "High" on this pin configures to operate in the E3 mode. A "Low" on this pin configures to operate in either STS-1 or DS3 mode depending on the setting on pin 19. ***NOTES:*** 1. *This pin is internally pulled down* 2. *This pin is ignored and may be tied to GND if the XRT75VL00 is configured to operate in HOST mode.*
19	STS-1/$\overline{DS3}$	I	**STS-1/DS3 Select Input** A "High" on this pin configures to operate in STS-1 mode. A "Low" on this pin configures to operate in DS3 mode. This pin is ignored if the E3 pin is set to "High". ***NOTES:*** 1. *This pin is internally pulled down* 2. *This pin is ignored and may be tied to GND if the XRT75VL00 is configured to operate in HOST mode.*
22	SR/$\overline{DR}$	I	**Single-Rail/Dual-Rail Select:** Setting this "High" configures both the Transmitter and Receiver to operate in Single-rail mode and also enables the B3ZS/HDB3 Encoder and Decoder. In Single-rail mode, Transmit input at TNData should be grounded. Setting this "Low" configures both the Transmitter and Receiver to operate in Dual-rail mode and disables the B3ZS/HDB3 Encoder and Decoder. ***NOTE:*** *This pin is internally pulled down.*

CONTROL AND ALARM INTERFACE

42	MRING	I	**Monitor Ring Input** The bipolar line output signal from TRING is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled down.*
41	MTIP	I	**Monitor Tip Input** The bipolar line output signal from TTIP is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled down.*
40	DMO	O	**Drive Monitor Output** If MTIP and MRING has no transition pulse for 128 ± 32 TxClk cycles, DMO goes "High" to indictae the driver failure. DMO output stays "High" until the next AMI signal is detected.

CONTROL AND ALARM INTERFACE

30	RLOS	O	**Receive Loss of Signal Output Indicator** This output pin toggles "High" if Receiver has detected a Loss of Signal Condition in the incoming line signal. The criteria for declaring/clearing an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode and is described in Section 2.04.
29	RLOL	O	**Receive Loss of Lock Output Indicator:** This output pin toggles "High" if the XRT75VL00 has detected a Loss of Lock Condition. LOL (Loss of Lock) condition is declared if the recovered clock frequency deviates from the Reference Clock frequency (available at ExClk input pin) by more than 0.5%.
33	Rext	****	**External Bias control Resistor of 3.3 KΩ ±1%.** Should be connected to RefAGND via 3.3 KΩ resistor.
15	TEST	I	**Test Mode:** Connect this pin “High” to configure the XRT75VL00 in test mode. ***NOTE:*** *This pin is internally pulled Down.*
16	$\overline{\text{ICT}}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled “High".*
2	TAOS	I	**Transmit All Ones Select** A “High" on this pin causes the Transmitter Section to generate and transmit a continuous AMI all “1’s” pattern onto the line. The frequency of this “1’s” pattern is determined by TxClk. ***NOTES:*** 1. *This input pin is ignored if the XRT75VL00 is operating in the HOST Mode and should be tied to GND.* 2. *Analog Loopback and Remote Loopback have priority over request.* 3. *This pin is internally pulled down.*
28	LOSMUT/ $\overline{\text{INT}}$	I/O	**MUTE-upon-LOS Enable Input or Interrupt Ouput:** In Hardware Mode, setting this pin “High” configures the XRT75VL00 to Mute the recovered data on the RPOS and RNEG whenever an LOS condition is declared. RPOS and RNEG outputs are pulled “Low”. ***NOTE:*** *If the XRT75VL00 is configured in HOST mode, this pin functions as $\overline{\text{INT}}$ pin (please refer to the pin description for the Microprocessor Interface).*

CONTROL AND ALARM INTERFACE

17	LLB	I	**Local Loop-back** This input pin along with RLB configures different Loop-Back modes. **RLB / LLB / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Analog Local** **1 / 0 / Remote** **1 / 1 / Digital** ***NOTE:*** *This input pin is ignored and may be connected to GND if the XRT75VL00 is operating in the HOST Mode.*
18	RLB	I	**Remote Loop-back** This input pin along with LLB configures different Loop-Back modes. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT75VL00 is operating in the HOST Mode.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
24	$\overline{CS}$/RxClkINV	I	**Microprocessor Serial Interface - Chip Select** Tie this "Low" to enable the communication with Serial Microprocessor Interface. ***NOTE:*** *If the XRT75VL00 is configured in Hardware Mode,this pin functions as RxClkINV.*
26	SCLK/TxClkINV	I	**Serial Interface Clock Input** The data on the SDI pin is sampled on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. ***NOTE:*** *If the XRT75VL00 is configured in Hardware Mode, this pin functions as TxClkINV.*
25	SDI/RxON	I	**Serial Data Input:** Data is serially input through this pin. The input data is sampled on the rising edge of the SCLK pin (pin 26). ***NOTES:*** 1. *This pin is internally pulled down* 2. *If the XRT75VL00 is configured in Hardware Mode, this pin functions as RxON.*
27	SDO/RxMON	O	**Serial Data Output:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SCLK and this pin is tri-stated upon completion of data transfer. ***NOTE:*** *If the XRT75VL00 is configured in Hardware Mode, this pin functions as RxMON.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
14	$\overline{\text{RESET}}$	I	**Register Reset:** Setting this input pin "Low" causes the XRT75VL00 to reset the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*
28	$\overline{\text{INT}}$/LOSMUT	I/O	**INTERRUPT Output:** This pin functions as Interrupt Output for Serial Interface. A transition to “Low” indicates that an interrupt has been generated by the Serial Interface. The interrupt function can be disabled by setting the interrupt enable bit to “0” in the Channel Control Register. ***NOTE:*** *If the XRT75VL00 is in Hardware mode, this pin functions as LOSMUT.*

JITTER ATTENUATOR INTERFACE

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>JA0</td><td>I</td><td>Disable Jitter Attenuator/FIFO Size Select::
In Hardware Mode, this pin along with JA1 pin provides the following functions in the table below.

<table><tr><th>JA0</th><th>JA1</th><th>Operation</th></tr><tr><td>0</td><td>0</td><td>16 bit FIFO</td></tr><tr><td>0</td><td>1</td><td>32 bit FIFO</td></tr><tr><td>1</td><td>0</td><td>Disable Jitter Attenuator</td></tr><tr><td>1</td><td>1</td><td>Disable Jitter Attenuator</td></tr></table>
NOTE: This pin is internally pulled down.</td></tr>
<tr><td>7</td><td>JA1</td><td>I</td><td>Disable Jitter Attenuator/FIFO Size Select:
In Hardware Mode, this pin along with JA0 pin provides the functions in the table above.
NOTE: This pin is internally pulled down.</td></tr>
<tr><td>8</td><td>JA Tx/$\overline{\text{Rx}}$</td><td>I</td><td>Jitter Attenuator Select:
In Hardware Mode setting this pin “High” selects the Jitter Attenuator in the Transmit path and setting “Low” selects in Receive path.
NOTE: This pin is internally pulled down.</td></tr>
</table>

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
3	TxAVDD	****	**Transmitter Analog VDD 3.3 V ± 5%**
10	RxAVDD	****	**Receiver Analog VDD 3.3 V ± 5%**
32	RefAVDD	****	**Reference Analog VDD 3.3 V ± 5%**
5	TxAGND	****	**Transmitter Analog GND**
13	RxAGND	****	**Receiver Analog GND**
34	RefAGND	****	**Reference Analog GND**
45	JaAVDD	****	**Jitter Attenuator Analog VDD 3.3 V ± 5%**
43	JaAGND	****	**Jitter Attenuator Analog GND**

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
31	DVDD	****	**VDD 3.3 V ± 5% Receiver Digital**
35	DGND	****	**GND**
52	DVDD	****	**VDD 3.3 V ± 5% Transmitter Digital**
49	DGND	****	**GND**

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5+0.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
ThetaJA	Thermal Resistance		20	$^0C/W$	linear air flow 0ft/min
ThetaJC			6	$^0C/W$	
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating		2000	V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current (Measured while transmitting and receiving all 1's)	65	120	175	mA
P_{DD}	Power Dissipation	210	395	610	mW
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs and outputs are TTL 5V compliant.*

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75VL00 (DUAL-RAIL DATA)

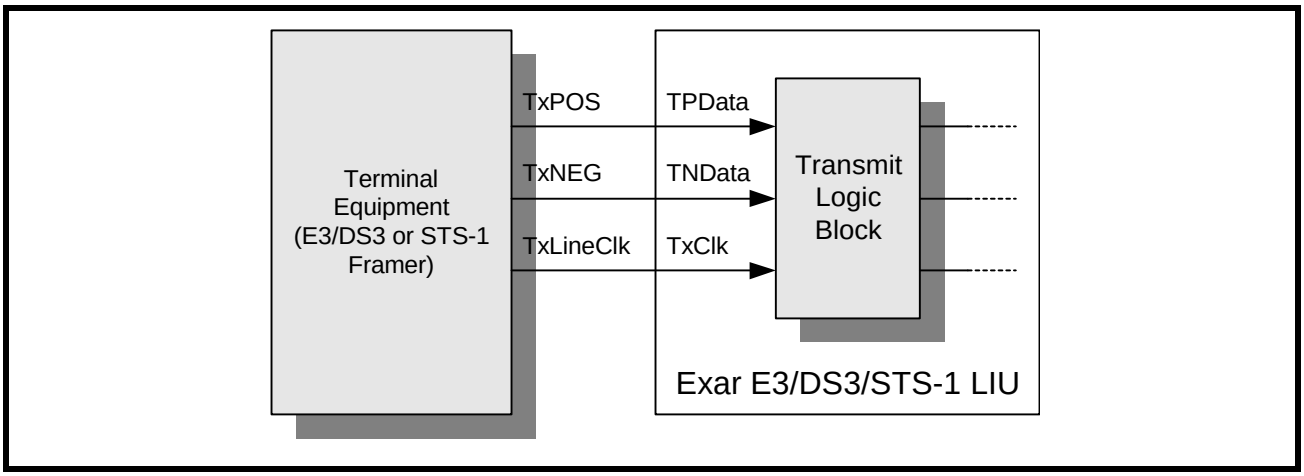
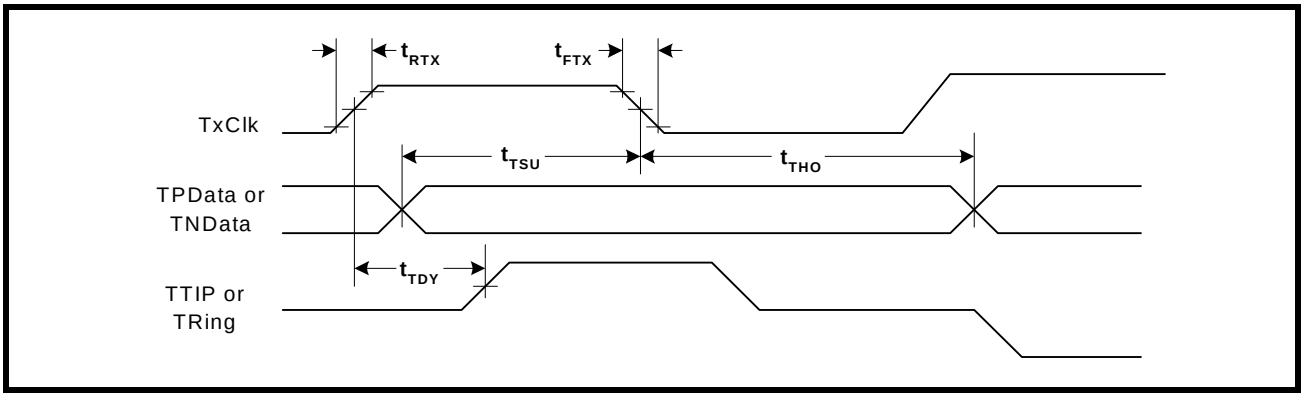
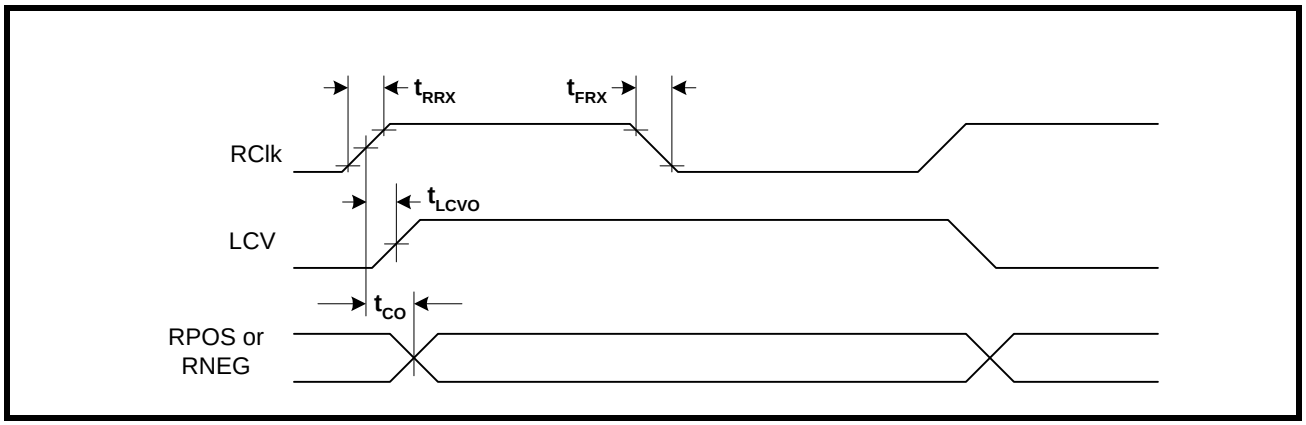


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



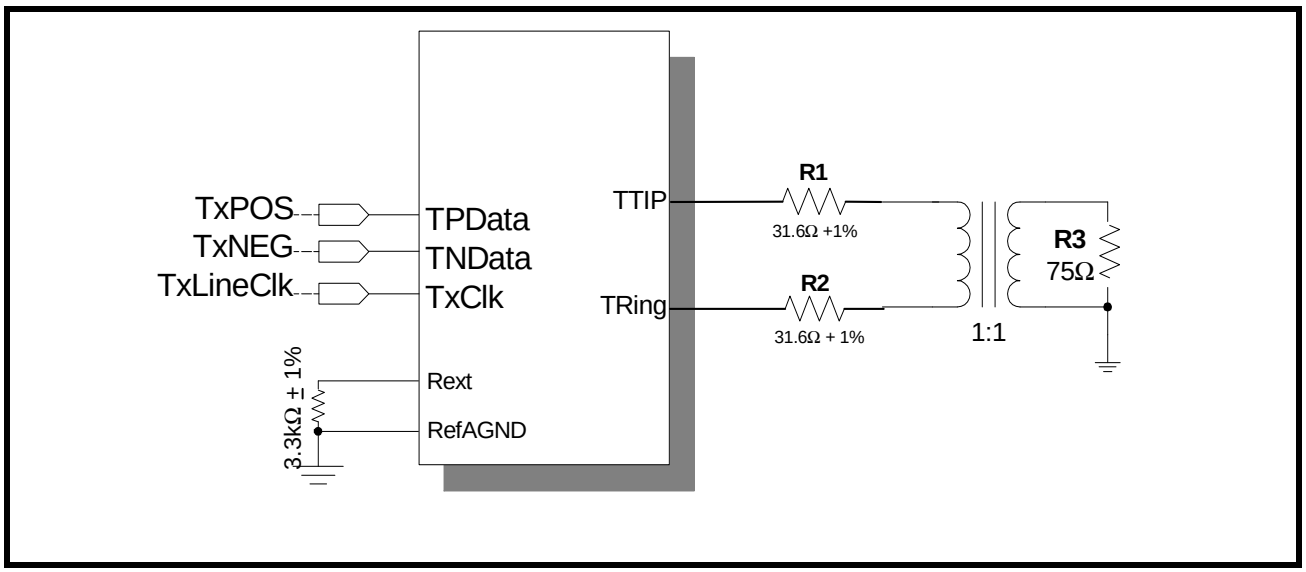
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle E3 DS3 STS-1	30	50 34.368 44.736 51.84	70	% MHz MHz MHz
t_{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t_{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t_{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t_{THO}	TPData/TNData to TxClk falling hold time	3			ns
t_{TDY}	TTIP/TRing to TxClk rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle E3 DS3 STS-1	45	50 34.368 44.736 51.84	55	% MHz MHz MHz
t_{RRX}	RxClk rise time (10% o 90%)		2	4	ns
t_{FRX}	RxClk falling time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES



3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75VL00 meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation at the secondary of the transformer. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

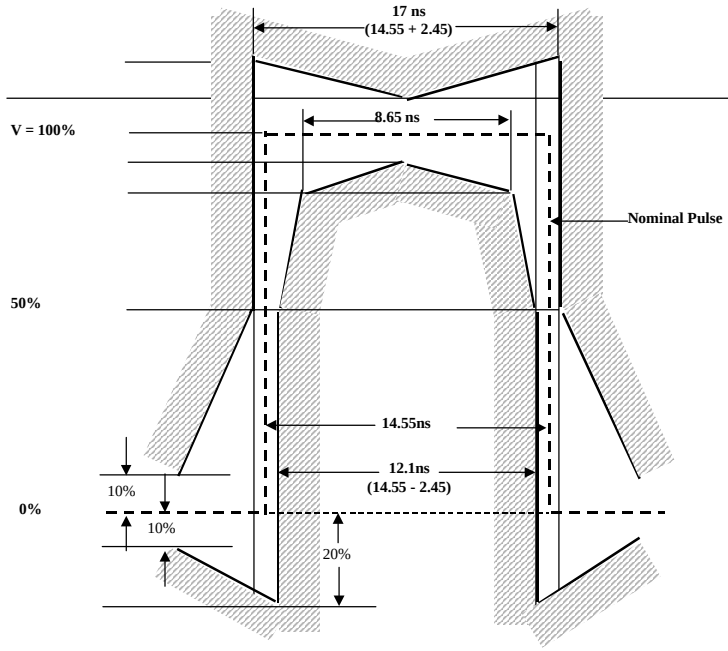


TABLE 3: E3 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS (T_A = 25^{0}C AND VDD = 3.3 V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Intrinsic Jitter		0.02	0.05	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)		1200		feet
Interference Margin	-20	-15		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

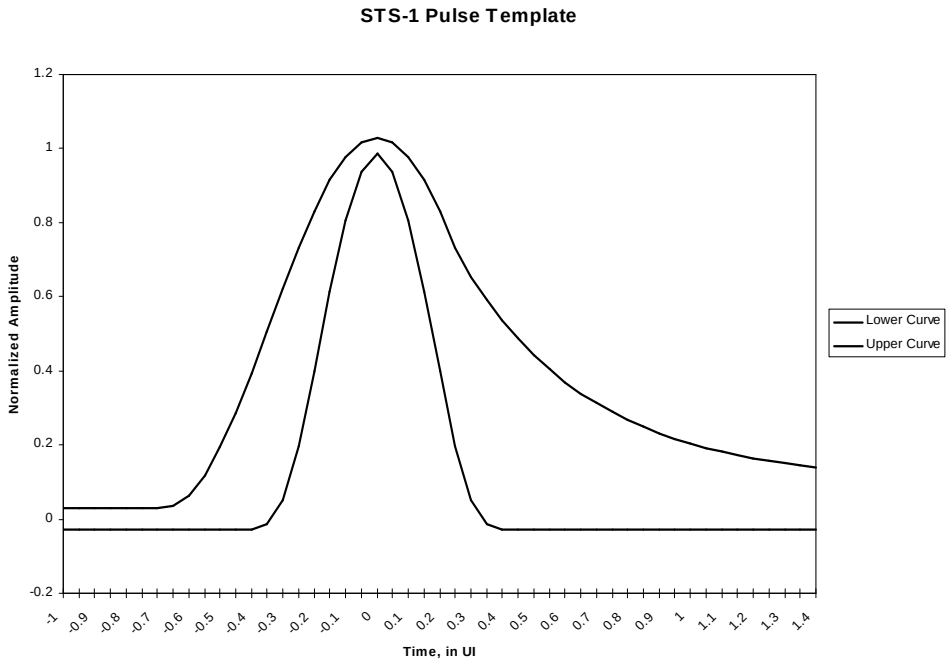


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \text{ x } e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS (TA = 25^{0}C AND VDD =3.3V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15	0.60		UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

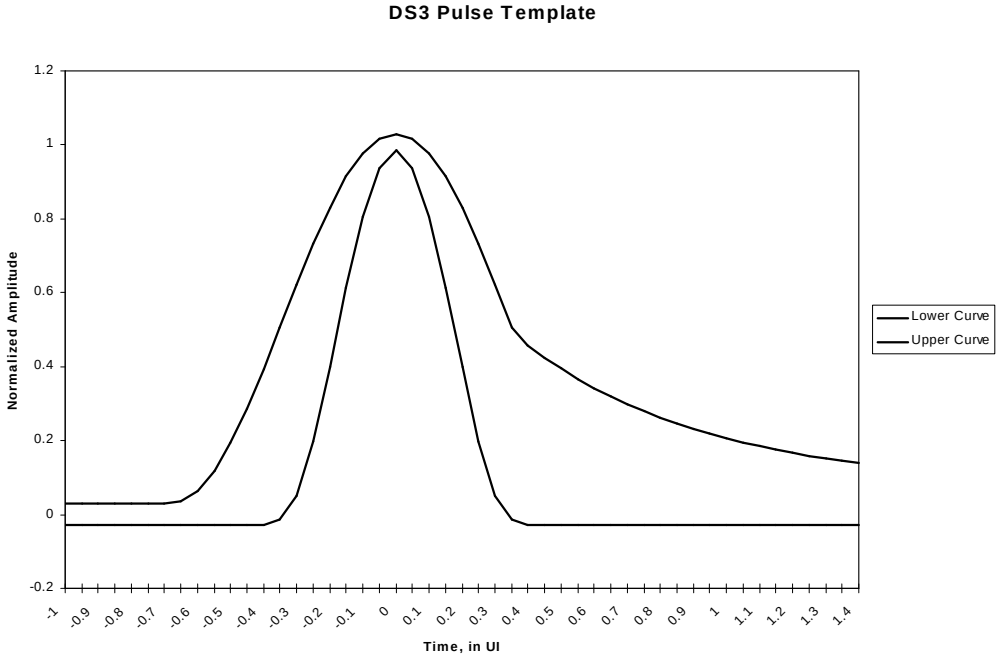


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS ($T_A = 25^0C$ AND VDD = 3.3V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15	0.60		UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE

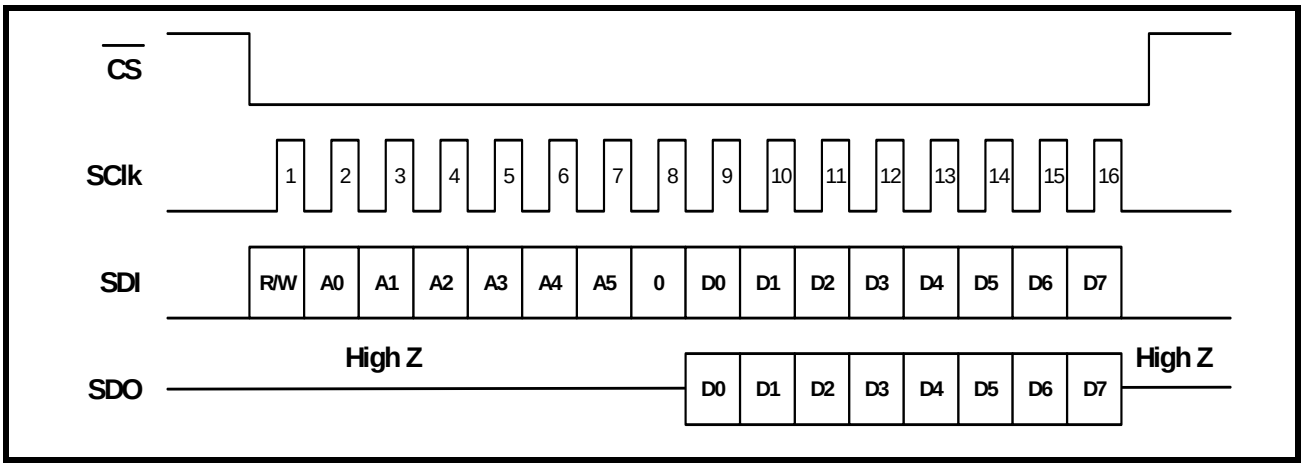


FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

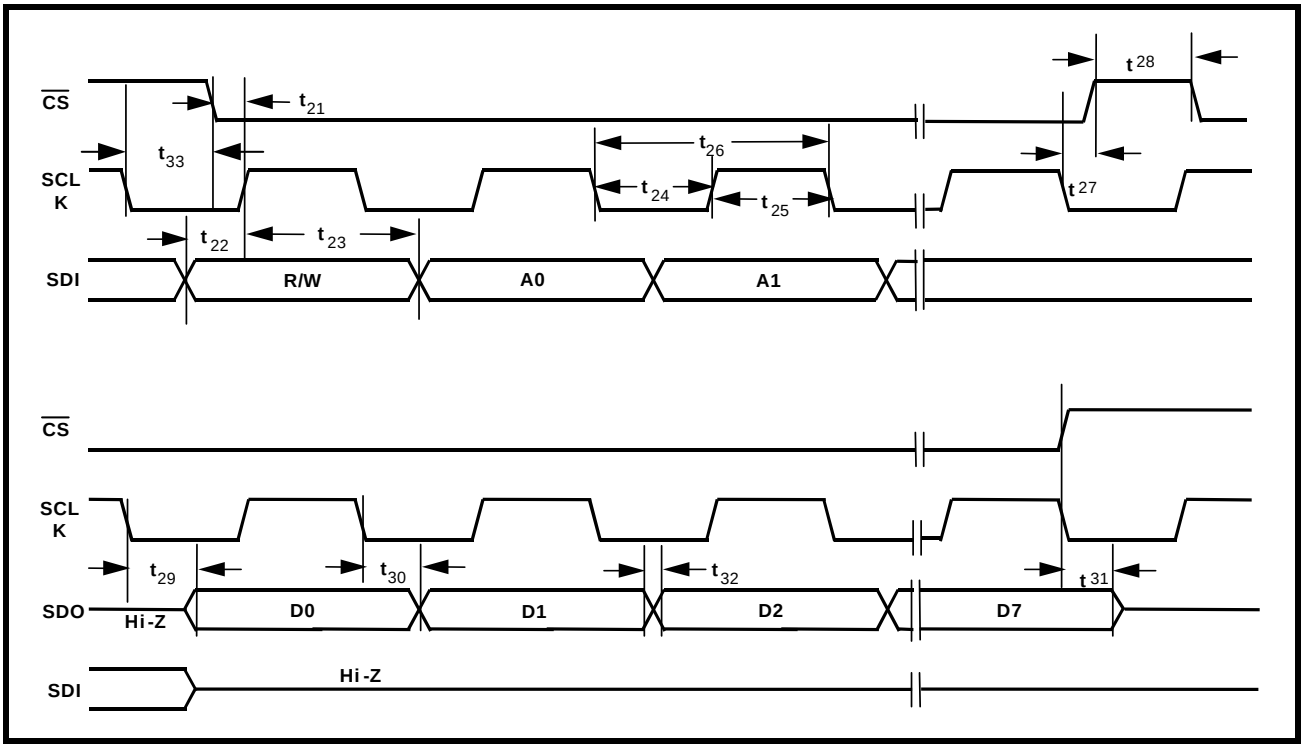


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (T_A = 25^{0}C, V_{DD}=3.3V± 5% AND LOAD = 10PF)

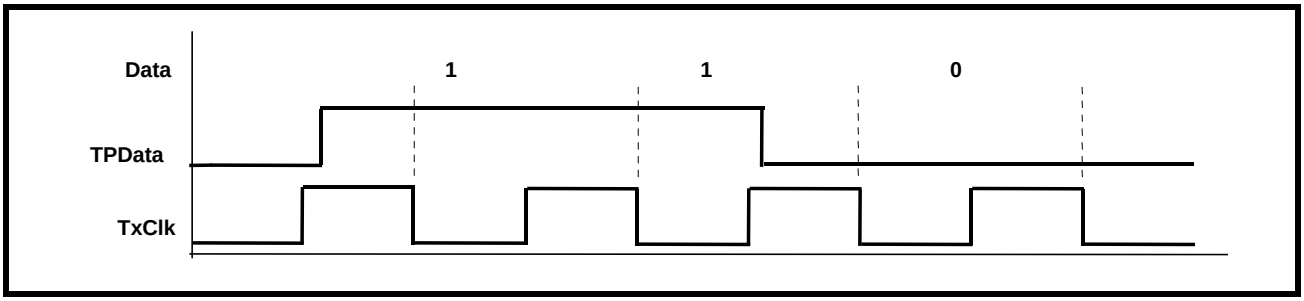
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time		25		ns
t_{25}	SClk "High" Time		25		ns
t_{26}	SClk Period		50		ns
t_{27}	Falling Edge of SClk to rising edge of $\overline{CS}$	0			ns
t_{28}	$\overline{CS}$ "Inactive" Time	50			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			20	ns
t_{30}	Falling Edge of SClk to SDO Invalid Time			10	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z		10		ns
t_{32}	Rise/Fall time of SDO Output			5	ns
t_{33}	SCLK Falling Edge to $\overline{CS}$ Low Assertion Time	5			ns

4.0 THE TRANSMITTER SECTION:

The Transmitter Section accepts TTL/CMOS level signals from the Terminal Equipment in the selectable data formats.

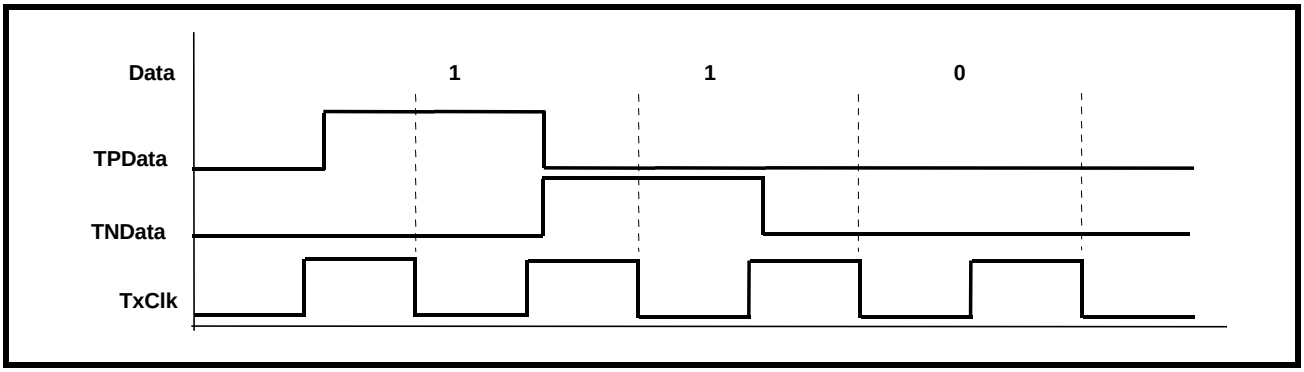
- In Single-Rail or un-encoded Non-Return-to-Zero (NRZ) input data via TPData pin while the TNData pin must be grounded. The NRZ or Single-Rail mode is selected when the SR/$\overline{DR}$ input pin is “High” (in Hardware Mode) or bit 0 of the control register is “1” (in Host Mode). Figure 12 illustrates the Single-Rail or NRZ format.

FIGURE 12. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)



- In Dual-Rail mode, data is input via TPData and TNData pins. TPData contains positive data and TNData contains negative data. The SR/$\overline{DR}$ input pin = “Low” (in Hardware Mode) or bit 0 of the control register = “0” (in Host Mode) enables the Dual-Rail mode. Figure 13 illustrates the Dual-Rail data format.

FIGURE 13. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements. Figure 7, Figure 8 and Figure 9 illustrate the pulse template requirements.
- Encode the un-encoded NRZ data into either B3ZS format (for DS3 or STS-1) or HDB3 format (for E3) and convert to pulses with shapes and width that are compliant with industry standard pulse template requirements. Figure 7,Figure 8 and Figure 9 illustrate the pulse template requirements.

4.1 TRANSMIT CLOCK:

The Transmit Clock applied via TxClk pin, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock be supplied and thus eliminates the need to use an expensive oscillator.

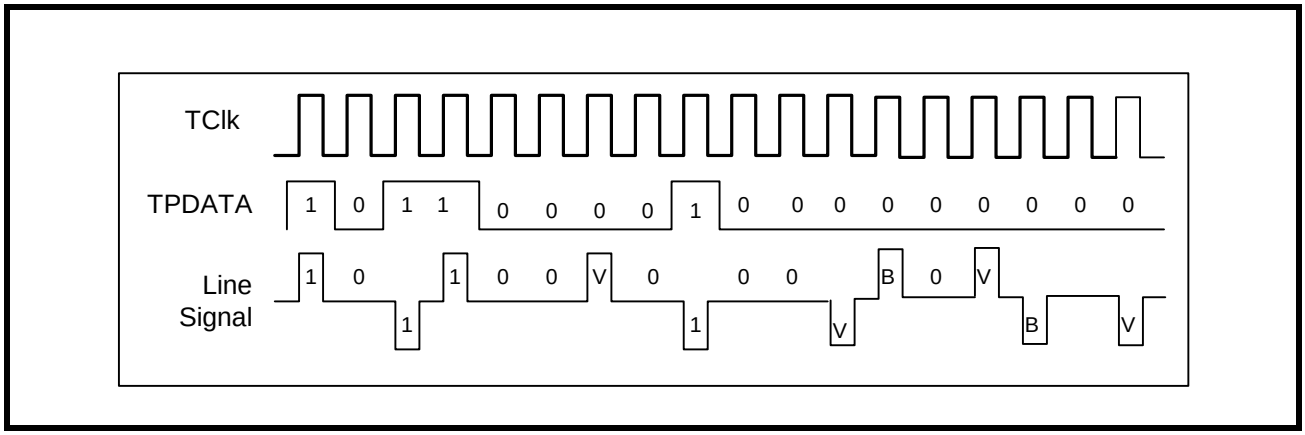
4.2 B3ZS/HDB3 ENCODER:

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.2.1 B3ZS Encoding:

An example of B3ZS encoding is shown in Figure 14. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of DC component into the line signal.

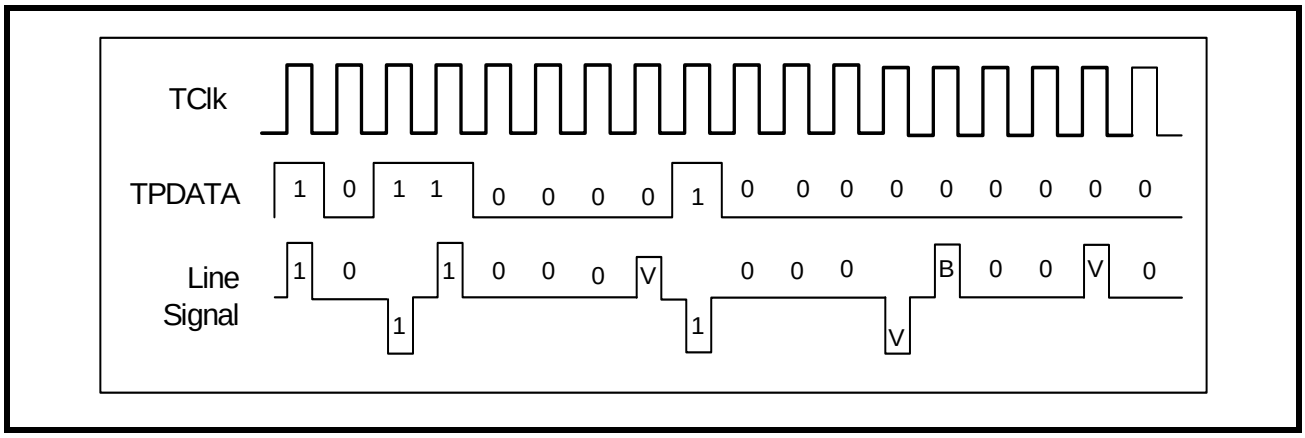
FIGURE 14. B3ZS ENCODING FORMAT



4.2.2 HDB3 Encoding:

An example of the HDB3 encoding is shown in Figure 15.If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of bipolar (B) pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

FIGURE 15. HDB3 ENCODING FORMAT



NOTES:

1. *When Dual-Rail data format is selected, the B3ZS/HDB3 Encoder is automatically disabled.*
2. *In Dual-Rail format, the Bipolar Violations in the incoming data stream is converted to valid data pulses.*
3. *Encoder and Decoder is enabled only in Single-Rail mode.*

4.3 TRANSMIT PULSE SHAPER:

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meet the industry standard mask template requirements for STS-1 and DS3. See Figure 8 and Figure 9.

For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. This is illustrated in Figure 7.

The Pulse Shaper Block also consists of a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV input pin “High” or “Low” (in Hardware Mode) or setting the TxLEV bit to “1” or “0” in the control register (in Host Mode).

For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet.

For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled.

4.3.1 Guidelines for using Transmit Build Out Circuit:

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV input pin “Low” (in Hardware Mode) or setting the TxLEV control bit to “0” (in Host Mode).

If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.3.2 Interfacing to the line:

The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 6.

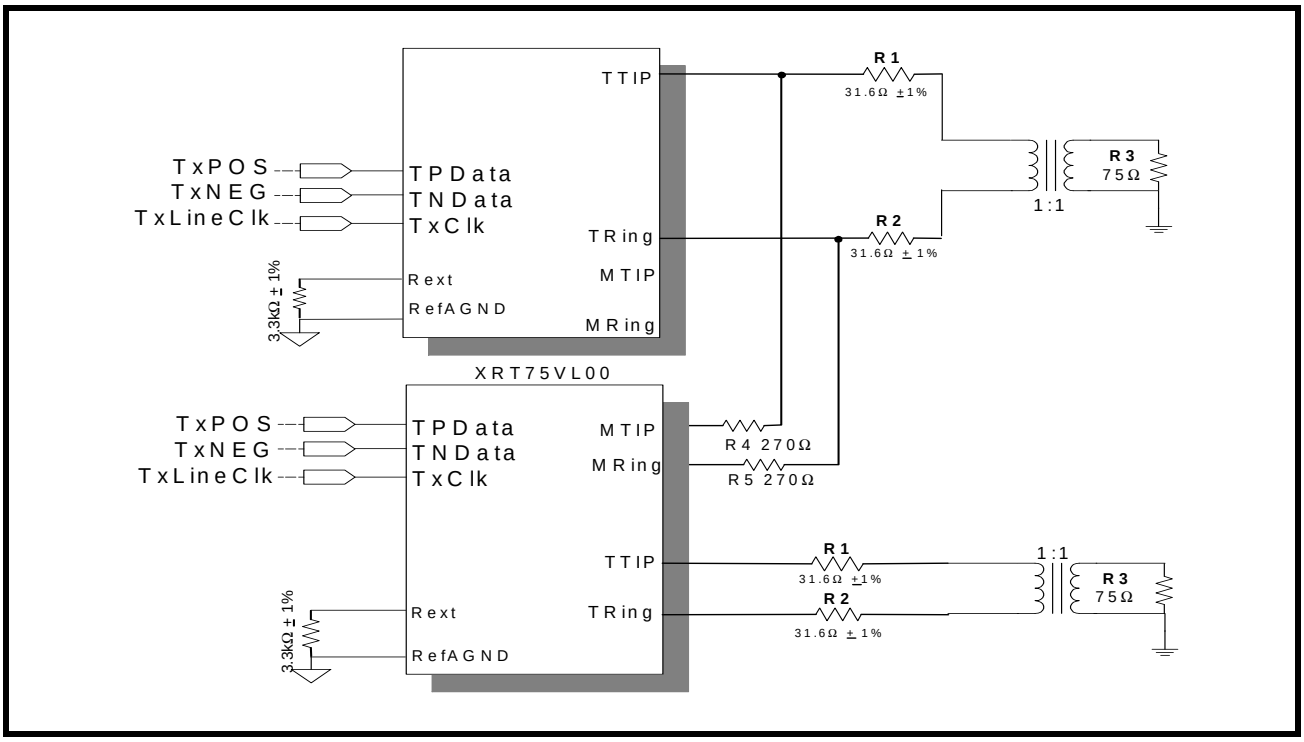
4.4 Transmit Drive Monitor:

This feature is used for monitoring the transmit line for occurrence of fault conditions such as short circuit on the line or defective line driver.The device can also be configured for internal tranmit driver monitoring.

To monitor the transmitter output of another chip, connect MTIP pin to the TTIP line via a 270 Ω resistor and MRing pins to TRing line via 270 Ω resistor as shown in Figure 16

In order to configure the device for internal transmit driver monitoring, set the TxMON bit to “1” in the transmit control register.

FIGURE 16. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP and MRing are connected to the TTIP and TRing lines, the drive monitor circuit monitors the line for transitions. The DMO (Drive Monitor Output) will be asserted “Low” as long as the transitions on the line are detected via MTIP and MRing.

If no transitions on the line are detected for 128 ± 32 TxClk periods, the DMO output toggles “High” and when the transitions are detected again, DMO toggles “Low”.

NOTE: *The Drive Monitor Circuit is only for diagnostic purposes and does not have to be used to operate the transmitter.*

4.5 Transmitter Section On/Off:

The transmitter section can be turned on or off. To turn on the transmitter in the Hardware mode, pull TxON pin “High”. In the Host mode, write a “1” to the TxON control bit AND pull the TxON pin “High” to turn on the transmitter.

When the transmitter is turned off, the TTIP and TRing are tri-stated.

NOTES:

1. *This feature provides support for Redundancy.*
2. *If the XRT75VL00 is configured in Host mode, to permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a “1” to the TxON control bit transfers the control to TxON pin.*

5.0 THE RECEIVER SECTION:

This section describes the detailed operation of the various blocks in the receiver. The receiver recovers the TTL/CMOS level data from the incoming bipolar B3ZS or HDB3 encoded input pulses.

5.1 AGC/Equalizer:

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB.

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce the Inter-Symbol Interference (ISI) so that, the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data.

The Equalizer can either be “IN” or “OUT” by setting the REQEN pin “High” or “Low” (in Hardware Mode) or setting the REQEN control bit to “1” or “0” (in Host Mode).

RECOMMENDATIONS FOR EQUALIZER SETTINGS:

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/ STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be left “IN” by setting the REQEN pin to “High” (in Hardware Mode) or setting the REQEN control bit to “1” (in Host Mode).

However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be left “OUT” for cable length less than 300 feet by setting the REQEN pin “Low” (in Hardware Mode) or by setting the REQEN control bit to “0” (in Host Mode).This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics.

NOTE: *The results of extensive testing indicates that even when the Equalizer was left “IN” (REQEN = “HIGH”), regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.*

The Equalizer also contain an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. This capability can be turned on by writing a “1” to the RxMON bits in the control register or by setting the RxMON pin (pin 27) “High”.

5.1.1 Interference Tolerance:

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error-free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same

recommendation is being used. Figure 17 shows the configuration to test the interference margin for DS3/ STS1. Figure 18 shows the set up for E3.

FIGURE 17. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

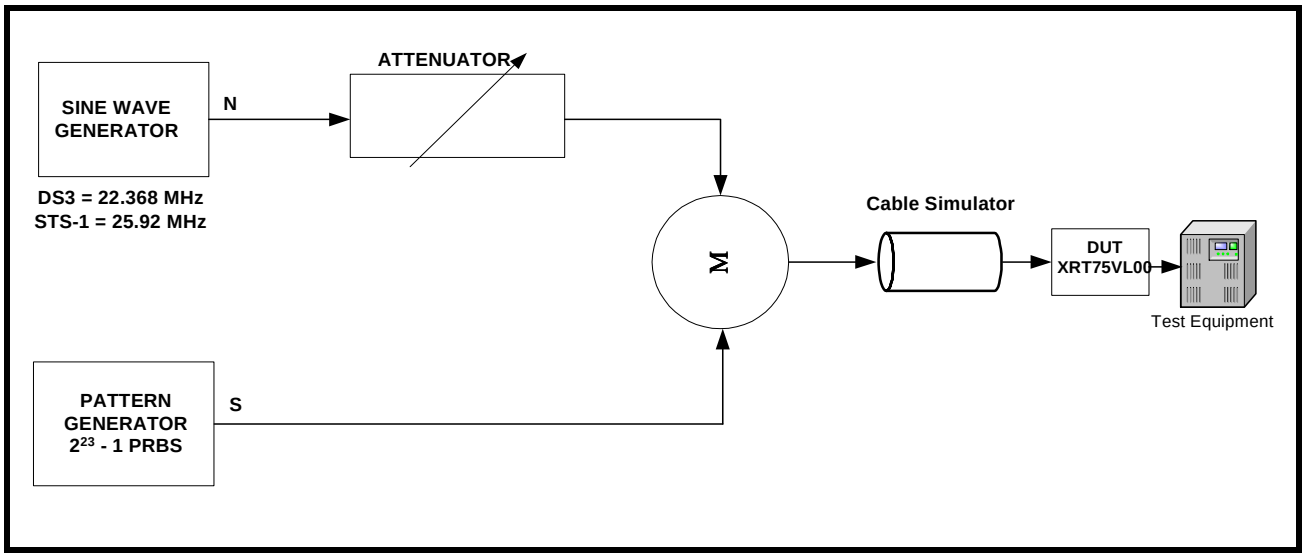


FIGURE 18. INTERFERENCE MARGIN TEST SET UP FOR E3.

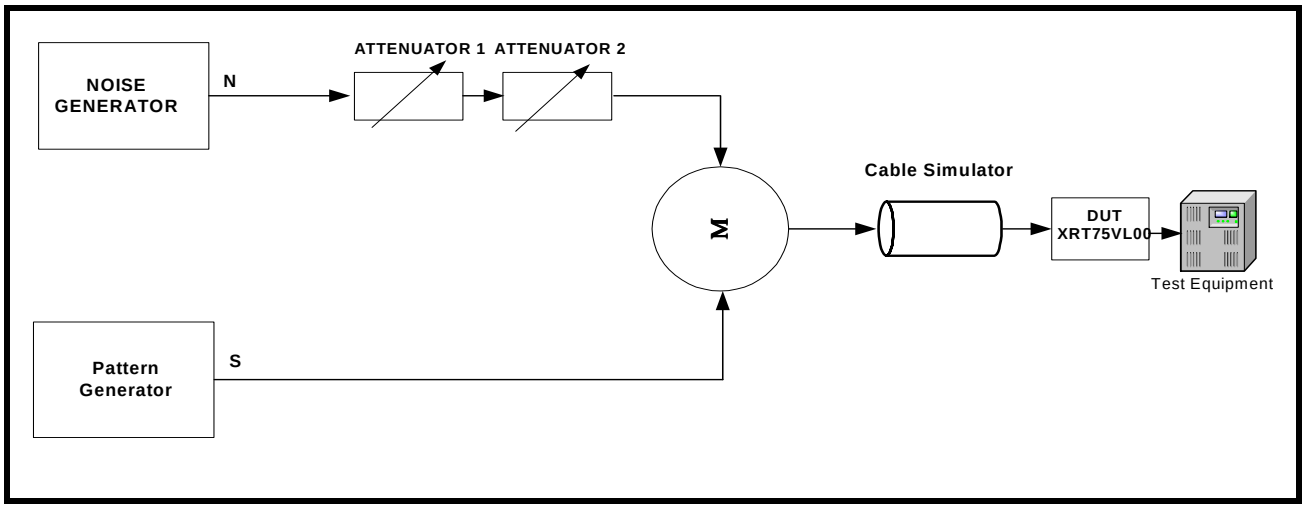


TABLE 9: INTERFERENCE MARGIN TEST RESULTS

MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	-14 dB
	12 dB	-18 dB
DS3	0 feet	-17 dB
	225 feet	-16 dB
	450 feet	-16 dB
STS-1	0 feet	-16 dB
	225 feet	-15 dB
	450 feet	-15 dB

5.2 Clock and Data Recovery:

The Clock and Data Recovery Circuit extracts the embedded clock, from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder.

The Clock Recovery PLL can be in one of the following two modes:

TRAINING MODE:

In the absence of input signals at RTIP and RRing pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk input pin exceed 0.5%, the clock recovery unit enters into Training Mode and a Loss of Lock condition is declared by toggling RLOL output pin “High” (in Hardware Mode) or setting the RLOL bit to “1” in the control registers (in Host Mode). Also, the clock output on the RxClk pin is the same as the reference clock applied on ExClk pin.

DATA/CLOCK RECOVERY MODE:

In the presence of input line signals on the RTIP and RRing input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk out pin is the Recovered Clock signal.

5.3 B3ZS/HDB3 Decoder:

The decoder block takes the output from clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream.

Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active “High” pulse is generated on the RLCV output pins to indicate line code violation.

NOTE: *In Single- Rail (NRZ) mode, the decoder is bypassed.*

5.4 LOS (Loss of Signal) Detector:

5.4.1 DS3/STS-1 LOS Condition:

A Digital Loss of Signal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS bit is set to “1” in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses.

Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 10.The status of the ALOS condition is reflected in the ALOS status control register.

RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS output pin is toggled “High” and the RLOS bit is set to “1” in the status control register.

TABLE 10: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS
DS3	1	≤20mV	≥90mV
STS-1	1	≤25mV	≥115mV

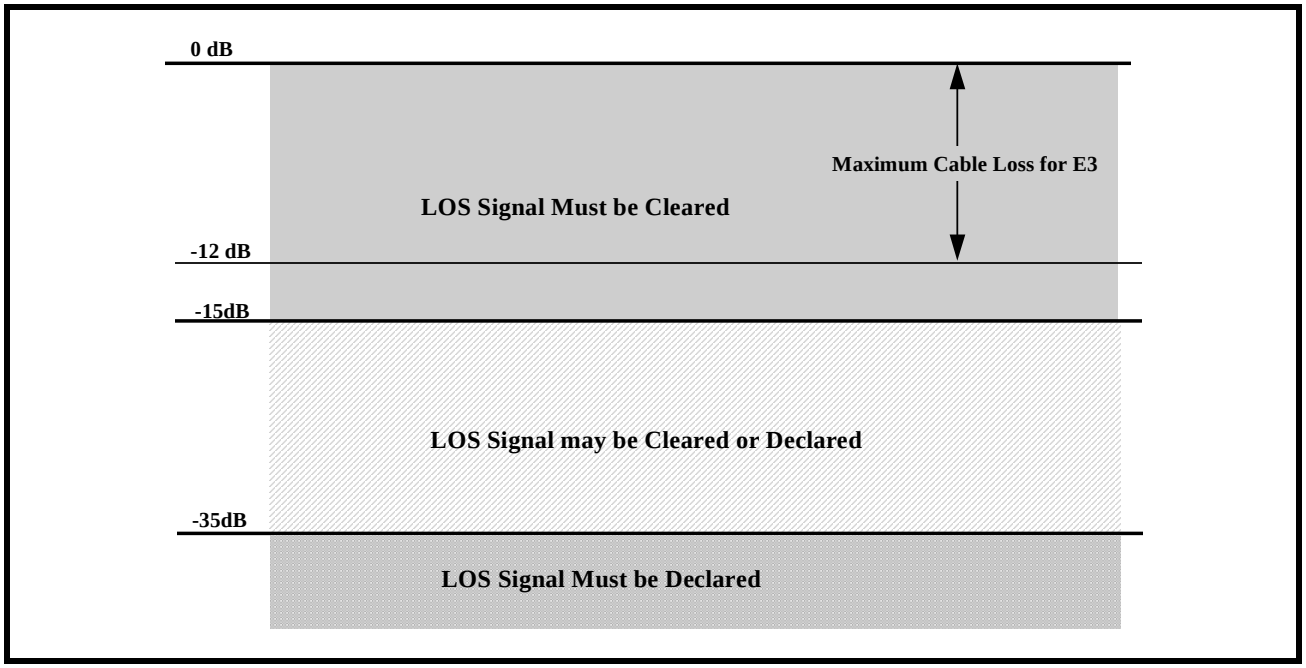
DISABLING ALOS/DLOS DETECTOR:

For debugging purposes it is useful to disable the ALOS/DLOS detector. Writing a “1” to the ALOS and DLOS bits disables the LOS detector on a per channel basis.

5.4.2 E3 LOS Condition:

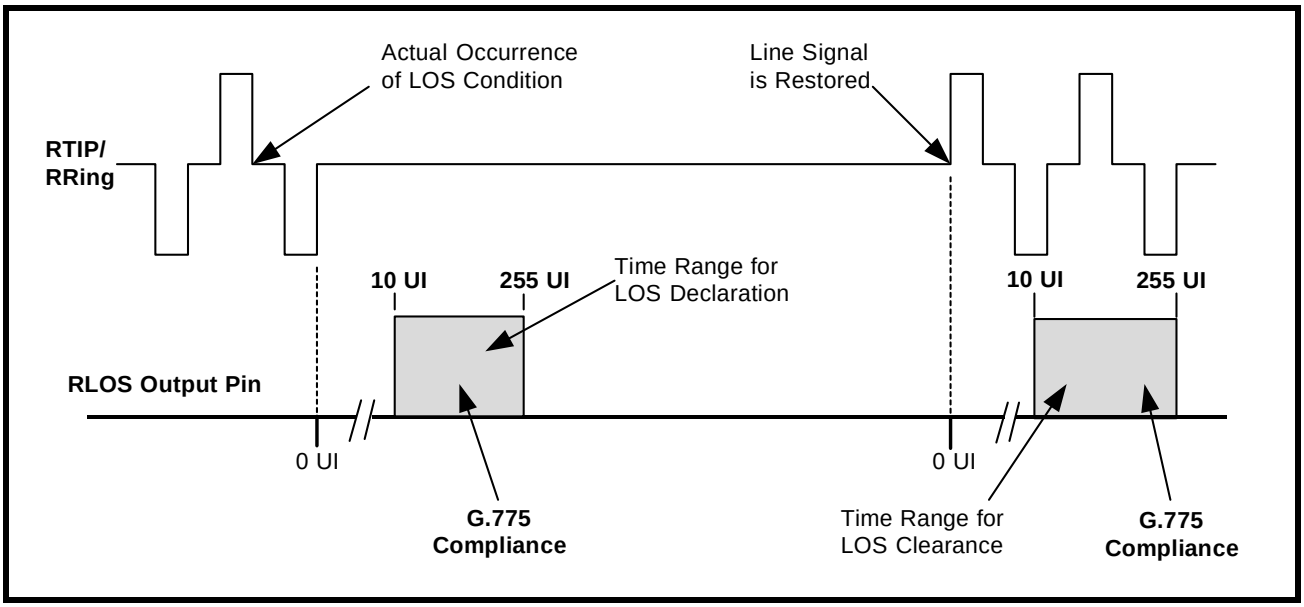
If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal level is defined to be between 15 and 35 dB below the normal level. If the signal drops below 35 dB for 175 ± 75 consecutive pulse periods, LOS condition is declared. This is illustrated in Figure 19.

FIGURE 19. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775



As defined in ITU-T G.775, an LOS condition is also declared between 10 and 255 UI (or E3 bit periods) after the actual time the LOS condition has occurred. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 20 shows the LOS declaration and clearance conditions.

FIGURE 20. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



5.4.3 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the ExClk pin and output this clock on the RxClk output. The data on the RPOS and RNEG pins can be forced to zero by pulling the LOSMUT pin “High” (in Hardware Mode) or by setting the LOSMUT bits in the individual channel control register to “1” (in Host Mode).

NOTE: When the LOS condition is cleared, the recovered data is output on RPOS and RNEG pins.

6.0 JITTER:

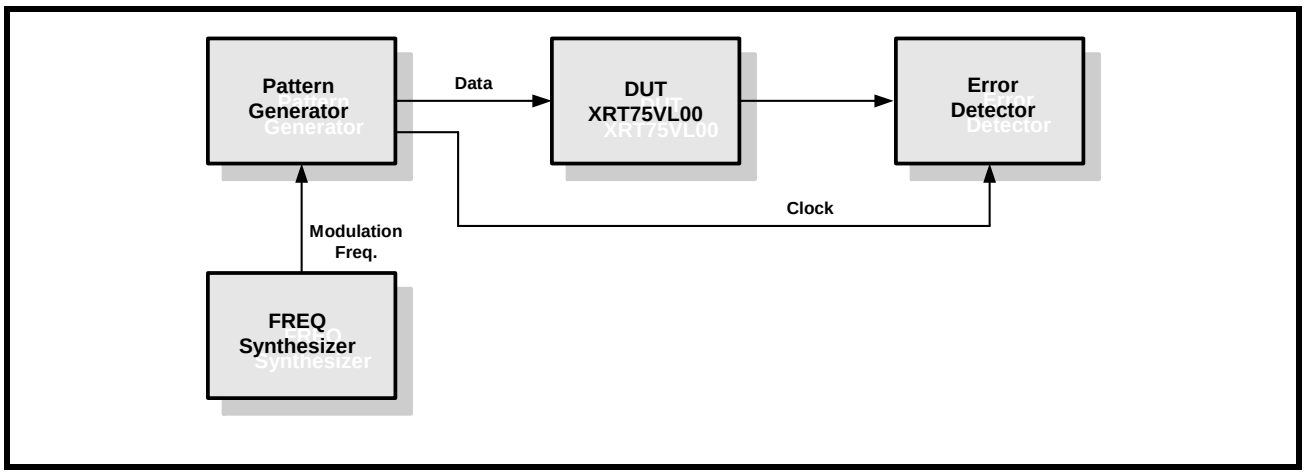
There are three fundamental parameters that describe circuit performance relative to jitter:

- **Jitter Tolerance (Receiver)**
- **Jitter Transfer (Receiver/Transmitter)**
- **Jitter Generation**

6.1 JITTER TOLERANCE - RECEIVER:

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 21, jitter is introduced by the sinusoidal modulation of the serial data bit sequence.

FIGURE 21. JITTER TOLERANCE MEASUREMENTS

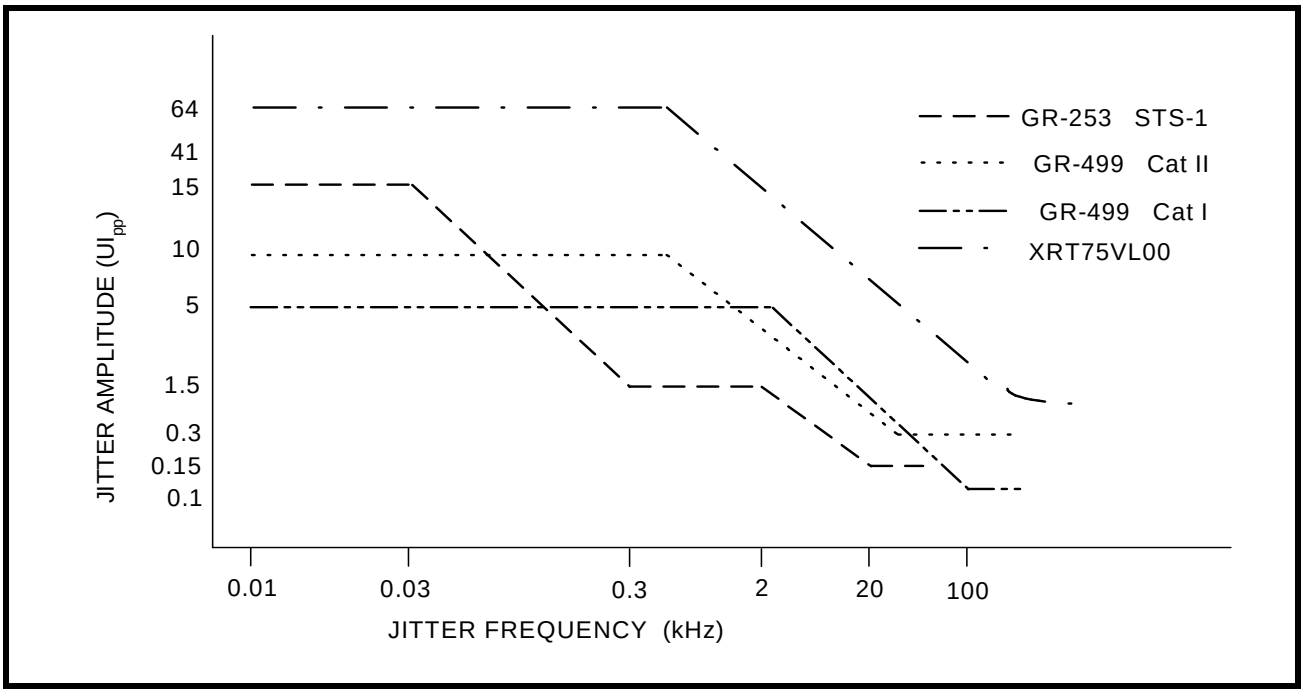


Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points.Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

6.1.1 DS3/STS-1 Jitter Tolerance Requirements:

Bellcore GR-499 CORE, Issue 1, December 1995 specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 22 shows the jitter tolerance curve as per GR-499 specification along with the measured performance for the device.

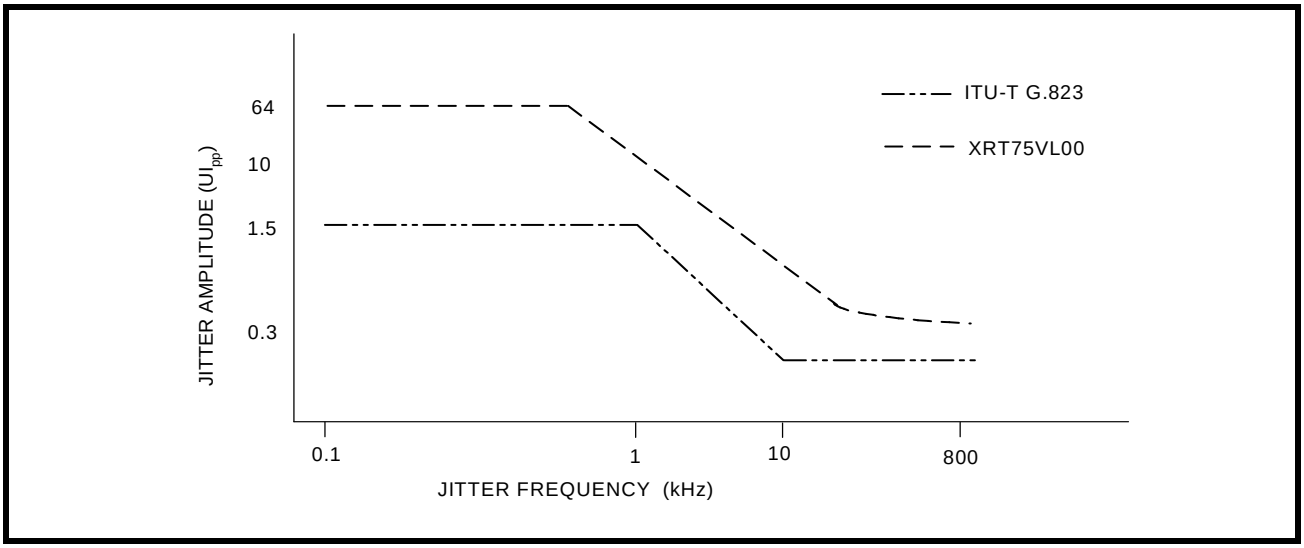
FIGURE 22. INPUT JITTER TOLERANCE FOR DS3/STS-1



6.1.2 E3 Jitter Tolerance Requirements:

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to accommodate and tolerate jitter up to certain specified limits. Figure 23 shows the tolerance curve and the actual measured data for the device.

FIGURE 23. INPUT JITTER TOLERANCE FOR E3



The Figure 11 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 11: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE (KB/S)	STANDARD	INPUT JITTER AMPLITUDE (UI P-P)			MODULATION FREQUENCY				
		A1	A2	A3	F1(HZ)	F2(HZ)	F3(KHZ)	F4(KHZ)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

6.2 JITTER TRANSFER - RECEIVER/TRANSMITTER:

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency.

There are two distinct characteristics in jitter transfer: jitter gain (jitter peaking) defined as the highest ratio above 0 dB; and jitter transfer bandwidth.The overall jitter transfer bandwidth is controller by a low bandwidth loop,which is part of the XRT75VL00..

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter.A zero dB jitter transfer indicates the element had no effect on jitter.

Table 12 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 12: JITTER TRANSFER SPECIFICATIONS

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

The XRT75VL00 meets the above Jitter Specifications.

6.3 JITTER GENERATION:

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

6.4 Jitter Attenuator:

An advanced crystal-less jitter attenuator is included in the XRT75VL00. The jitter attenuator uses the internal reference clock.

In Host mode, by clearing or setting the JATx/$\overline{Rx}$ bit in the control register selects the jitter attenuator either in the Receive or Transmit path. In Hardware mode, JATx/$\overline{Rx}$ pin selects the jitter attenuator in Receive or Transmit path.

The FIFO is either a 16-bit or 32-bit register. In Host mode, the bits JA0 and JA1can be set to appropriate combination to select the different FIFO sizes or to disable the jitter attenuator. In Hardware mode, appropriate setting of the pins JA0 and JA1 selects the different FIFO sizes or disable the jitter attenuator. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered

clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL is set to “1” in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

NOTE: *It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter.*

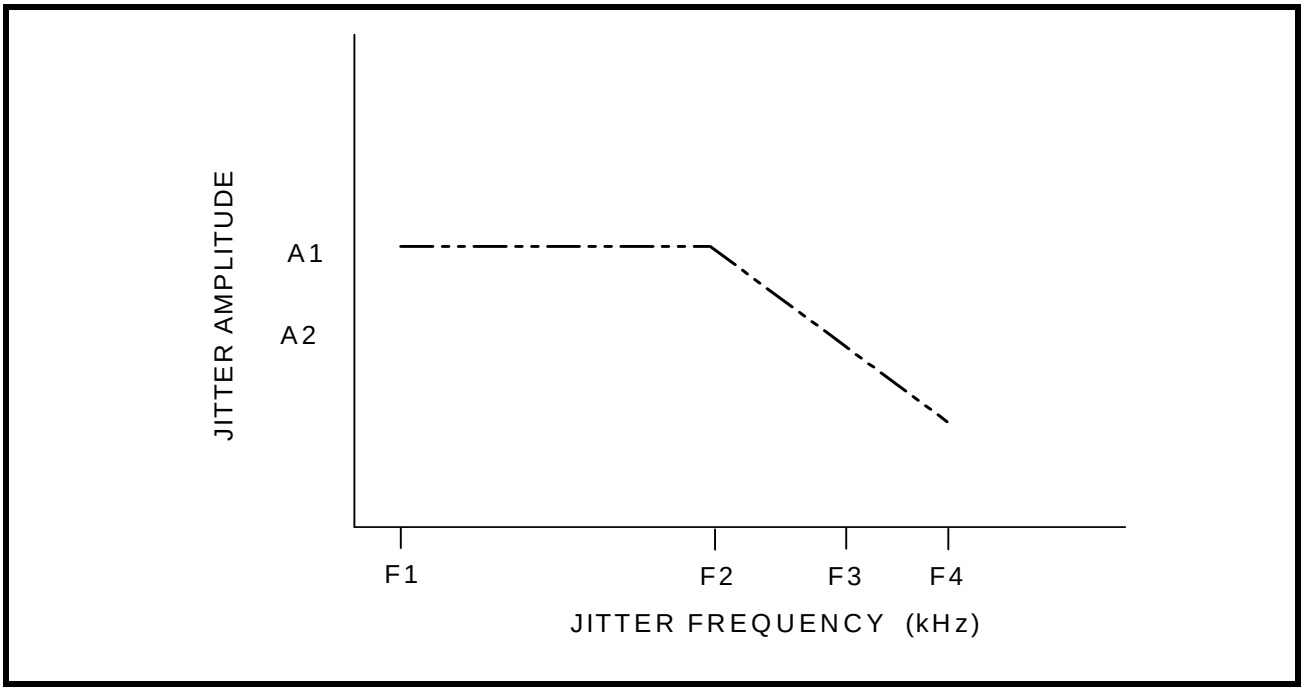
Table 13 specifies the jitter transfer mask requirements for various data rates:

TABLE 13: JITTER TRANSFER PASS MASKS

RATE (KBITS)	MASK	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (KHZ)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3K	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75VL00 meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 24.

FIGURE 24. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



7.0 SERIAL HOST INTERFACE:

A flexible serial microprocessor interface is incorporated in the XRT75VL00. The interface is generic and is designed to support the common microprocessors/microcontrollers. The XRT75VL00 operates in Host mode when the HOST/$\overline{HW}$ pin is tied "High". The serial interface includes a serial clock (SClk), serial data input (SDI), serial data output (SDO), chip select (CS) and interrupt output (INT). The serial interface timing is shown in Figure 11.

The active low interrupt output signal ($\overline{INT}$ pin) indicates alarm conditions like LOS, DMO and FL to the processor.

When the XRT75VL00 is configured in Host mode, the following input pins,TxLEV, TAOS, RLB, LLB, E3, STS-1/DS3, REQEN, JATx/Rx, JA0 and JA1 are disabled and must be connected to ground.

Table 14 below illustrates the functions of the shared pins in either Host mode or in Hardware mode.

TABLE 14: FUNCTIONS OF SHARED PINS

PIN NUMBER	IN HOST MODE	IN HARDWARE MODE
24	$\overline{CS}$	RxClkINV
26	SClk	TxClkINV
25	SDI	RxON
27	SDO	RxMON
28	$\overline{INT}$	LOSMUT

NOTE: *While configured in Host mode, the TxON input pin will be active if the TxON bit in the control register is set to "1", and can be used to turn on and off the transmit output drivers. This permits a system designed for redundancy to quickly switch out a defective line card and switch-in the backup line card.*

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x00	APS/Redundancy (read/write)	Reserved	Reserved	Reserved	RxON	Reserved	Reserved	Reserved	TxON
0x01	Interrupt Enable (read/write)	Reserved		CNT_SATIE	PRBSIE	FLIE	RLOLIE	RLOSIE	DMOIE
0x02	Interrupt Status (reset on read)	Reserved		CNT_SATIS	PRBSIS	FLIS	RLOLIS	RLOSIS	DMOIS
0x03	Alarm Status (read only)	Reserved	PRBSLS	DLOS	ALOS	FL	RLOL	RLOS	DMO
0x04	Transmit Control (read/write)	Reserved		TxMON	INSPRBS	Reserved	TAOS	TxClkINV	TxLEV
0x05	Receive Control (read/write)	Reserved		DLOSDIS	ALOSDIS	RxClkINV	LOSMUT	RxMON	REQEN
0x06	Block Control (read/write)	Reserved		PRBSEN	RLB	LLB	E3	STS1/$\overline{DS3}$	SR/$\overline{DR}$
0x07	Jitter Attenuator (read/write)	Reserved				PNTRST	JA1	JATx/$\overline{Rx}$	JA0

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x08-0x1F	Reserved								
0x20	Interrupt Enable-Global (read/write)	Reserved					Reserved	Reserved	INTEN
0x21	Interrupt Status (read only)	Reserved					Reserved	Reserved	INTST
0x22-0x2F	Reserved	Reserved							
0x30	PRBS Error Count (MSB)	MSB							LSB
0x31	PRBS Error Count (LSB)	MSB							LSB
0x32-0x37	Reserved								
0x38	PRBS Holding	MSB							LSB
0x39-0x3D	Reserved								
0x3E	Chip_id (read only)	Device part number (7:0)							
0x3F	Chip_version (read only)	Chip revision number (7:0)							

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x00	R/W	D0	RxON	Bit 4 = RxON, Receiver Turn On. Writing a “1” to the bit field turns on the Receiver and a “0” turn off the Receiver.	0
		D4	TxON	Bit 0 = TxON, Transmitter Turn On. Writing a “1” to the bit field turn on the Transmitter. Writing a “0” turns off the transmitter and tri-state the transmitter output (TTIP/TRing).	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x01	R/W	D0	DMOIE	Writing a "1" to this bit field enables the DMO interrupt and triggers an interrupt when the transmitter driver fails. Writing a "0" disables the interrupt.	0
		D1	RLOSIE	Writing a "1" to this bit field enables the RLOS interrupt and triggers an interrupt when the RLOS condition occurs. Writing a "0" disables the interrupt.	0
		D2	RLOLIE	Writing a "1" to this bit field enables the RLOL interrupt and triggers an interrupt when RLOL condition occurs. Writing a "0" disables the interrupt.	0
		D3	FLIE	Writing a "1" to this bit field enables the FL interrupt and triggers an interrupt when the FIFO Limit of the Jitter Attenuator is within 2 bits of overflow/underflow condition. Writing a "0" disables the interrupt. ***NOTE:*** *This bit field is ignored when the Jitter Attenuator is disabled.*	0
		D4	PRBSIE	Writing a "1" to this bit enables the PRBS bit error interrupt.	0
		D5	CNT_SATIE	Writing a "1" to this bit enables the PRBS error-counter saturation interrupt. When the PRBS error counter reaches 0xFFFF, an interrupt will be generated.	0
0x02	Reset Upon Read	D0	DMOIS	This bit is set to "1" every time a DMO status change has occurred since the last cleared interrupt.This bit is cleared when read.	0
		D1	RLOSIS	This bit is set to "1" every time a RLOS status change has occurred since the last cleared interrupt. This bit is cleared when read.	0
		D2	RLOLIS	This bit is set to "1" every time a RLOL status change has occurred since the last cleared interrupt. This bit is cleared when read.	0
		D3	FLIS	This bit is set to "1" every time a FIFO Limit status change has occurred since the last cleared interrupt. This bit is cleared when read.	0
		D4	PRBSIS	This bit is set to "1" when a PRBS bit error is detected. This bit is cleared when read.	0
		D5	CNT_SATIS	This bit is set to "1" when the PRBS error counter has saturated (0xFFFF). This bit is cleared when read.	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x03	Read Only	D0	DMO	This bit is set to "1" every time the MTIP/MRing input pins have not detected any bipolar pulses for 128 consecutive bit periods.	0
		D1	RLOS	This bit is set to "1" every time the receiver declares an LOS condition.	0
		D2	RLOL	This bit is set to "1" every time when the receiver declares a Loss of Lock condition.	0
		D3	FL	This bit is set to "1" every time the FIFO in the Jitter Attenuator is within 2 bit of underflow/overflow condition.	0
		D4	ALOS	This bit is set to "1" every time the receiver declares Analog LOS condition.	0
		D5	DLOS	This bit is set to "1" every time the receiver declares Digital LOS condition.	0
		D6	PRBSLS	This bit is set to "1" every time the PRBS detects a bit error.	0
0x04	R/W	D0	TxLEV	Writing a "1" to this bit disables the Transmit Build-out circuit and writing a "0" enables the Transmit Build-out circuit. ***NOTE:*** *See section 4.03 for detailed description.*	0
		D1	TxClkINV	Writing a "1" to this bit configures the transmitter to sample the data on TPData/TNData input pins on the rising edge of TxClk.	0
		D2	TAOS	Setting this bit to "1" causes a continuous stream of marks to be sent out at the TTIP and TRing pins.	0
		D3	Reserved	This Bit Location is Not Used.	
		D4	INSPRBS	Writing a "1" to this bit causes the PRBS generator to insert a single-bit error onto the transmit PRBS data stream. ***NOTE:*** *PRBS Generator/Detector must be enabled for this bit to have any effect.*	0
		D5	TxMON	When this bit is set to "1", the driver monitor is connected to its own transmit channel and monitors the transmit driver. When a transmit failure is detected, the DMO output will go high. When this bit is "0", MTIP and MRing can be connected to other transmit channel for monitoring.	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x05	R/W	D0	REQEN	Setting this bit to "1" enables the Receive Equalizer . ***NOTE:*** *See section 2.01 for detailed description.*	0
		D1	RxMON	Writing a "1" to this bit configures the Receiver into monitoring mode. In this mode, the Receiver can monitor a signal at the RTIP/RRing pins that be attenuated up to 20dB flat loss.	0
		D2	LOSMUT	Writing a "1" to this bit causes the RPOS/RNEG outputs to be grounded while the LOS condition is declared. ***NOTE:*** *If this bit has ben set, it will remain set evan after LOS condition is cleared.*	0
		D3	RxClkINV	Writing a "1" to this bit configures the Receiver to output RPOS/RNEG data on the falling edge of RxClk.	0
		D4	ALOSDIS	Writing a "1" to this bit disables the ALOS detector.	0
		D5	DLOSDIS	Writing a "1" to this bit disables the DLOS detector.	0
0x06	R/W	D0	SR/$\overline{DR}$	Writing a "1" to this bit configures the Receiver and Transmitter into Single-Rail (NRZ) mode.	0
		D1	STS-1/$\overline{DS3}$	Writing a "1" to this bit configures the channel 0 into STS-1 mode. ***NOTE:*** *This bit field is ignored if the chip is configured to operate in E3 mode.*	0
		D2	E3	Writing a "1" to this bit configures the chip in E3 mode.	0
		D3	LLB	Writing a "1" to this bit configures the chip in Local Loopback mode.	0
		D4	RLB	Writing a "1" to this bit configures the chip in Remote Loopback mode. **RLB / LLB / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Analog Local** **1 / 0 / Remote** **1 / 1 / Digital**	0
		D5	PRBSEN	Writing a "1" to this bit enables the PRBS generator/detector.PRBS generator generate and detect either 2^{15}-1 (DS3 or STS-1) or 2^{23}-1 (for E3). The pattern generated and detected are unframed pattern.	0

TABLE 16: REGISTER MAP DESCRIPTION

<table>
<tr><th>ADDRESS (HEX)</th><th>TYPE</th><th>BIT LOCATION</th><th>SYMBOL</th><th>DESCRIPTION</th><th>DEFAULT VALUE(BIN)</th></tr>
<tr><td>0x07</td><td>R/W</td><td>D0</td><td>JA0</td><td>This bit along with JA1 bit configures the Jitter Attenuator as shown in the table below.

<table><tr><th>JA0</th><th>JA1</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>16 bit FIFO</td></tr><tr><td>0</td><td>1</td><td>32 bit FIFO</td></tr><tr><td>1</td><td>0</td><td>Disable Jitter Attenuator</td></tr><tr><td>1</td><td>1</td><td>Disable Jitter Attenuator</td></tr></table></td><td>0</td></tr>
<tr><td></td><td></td><td>D1</td><td>JATx/$\overline{Rx}$</td><td>Writing a “1” to this bit selects the Jitter Attenuator in the Transmit Path. A “0” selects in the Receive Path.</td><td>0</td></tr>
<tr><td></td><td></td><td>D2</td><td>JA1</td><td>This bit along with the JA0 configures the Jitter Attenuator as shown in the table.</td><td>0</td></tr>
<tr><td></td><td></td><td>D3</td><td>PNTRST</td><td>Setting this bit to “1” resets the Read and Write pointers of the jitter attenuator FIFO.</td><td>0</td></tr>
<tr><td>0x08</td><td colspan="5">Reserved</td></tr>
</table>

TABLE 17: REGISTER MAP DESCRIPTION - GLOBAL

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x20	R/W	D0	INTEN	Bit 0 = INTEN Writing a “1” to this bit enables the interrupts.	0
0x21	Read Only	D0	INTST	Bit 0 = INTST bit is set to “1” if an interrupt service is required. The source level interrupt status register is read to determine the cause of interrupt.	0
0x22 - 0x2F	Reserved				
0x30	Reset Upon Read	D[7:0]	PRBSmsb	PRBS error counter MSB [15:8]	
0x31	Reset Upon Read	D[7:0]	PRBSlsb	PRBS error counter LSB [7:0]	
0x32-0x37	Reserved				
0x38	Read Only	D[7:0]	PRBShold	PRBS Holding Register	
0x39-0x3D	Reserved				

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x3E	Read Only	D[7:0]	Chip_id	This read only register contains device id.	01110001
0x3F	Read Only	D[7:0]	Chip_version	This read only register contains chip version number	1xxxxxxx

8.0 DIAGNOSTIC FEATURES:

8.1 PRBS Generator and Detector:

The XRT75VL00 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. This feature is only available in Host mode. With the PRBSEN bit = "1", the transmitter will send out PRBS of 2^{23}-1 in E3 rate or 2^{15}-1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for half RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

When PRBS mode is enabled, the PRBS counter starts counting each single bit error. The PRBS counter is 16 bits wide. The current value in the counter can be read via two readback operations of the Serial I/O registers.

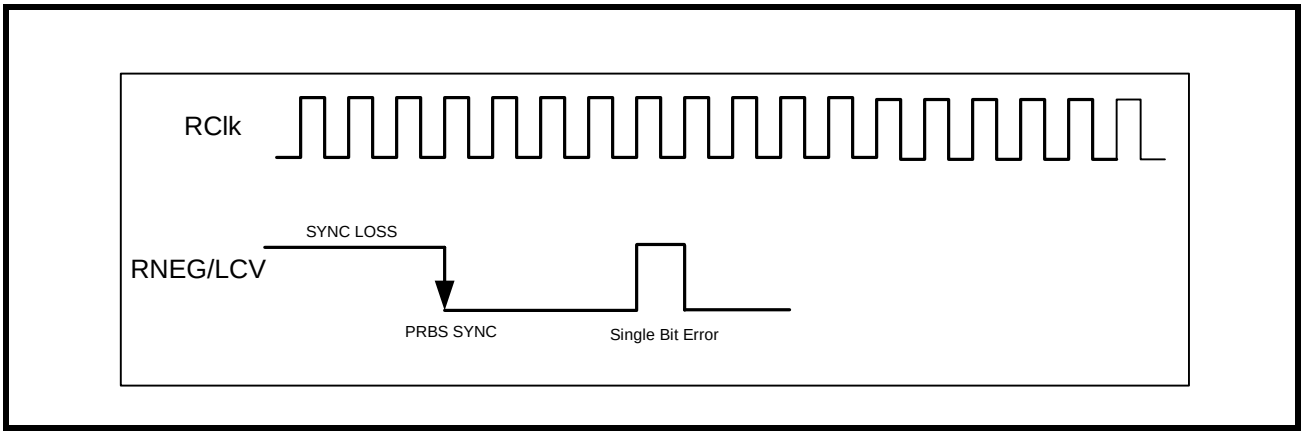
1) Either the Least Significant Byte (LSB, address 0x30) or the Most Significant Byte (MSB, address 0x31) can be read first. The value of the un-read register will be copied into the Holding register (address 0x38) and both the LSB and MSB registers will be reset to zero.

2) Read the Holding register and concatenate the result with the value from the first read operation to get the full 16 bit counter value.

When the PRBS mode is first enabled, errors will be counted while the receiver logic is synchronizing to the PRBS pattern. When RNEG/LCV goes "Low" indicating PRBS synchronization, reset the counter by reading either the LSB or the MSB register.

Figure 25 shows the status of RNEG/LCV pin when the XRT75VL00 is configured in PRBS mode.

FIGURE 25. PRBS MODE



8.2 LOOPBACKS:

The XRT75VL00 offers three loopback modes for diagnostic purposes. In Hardware mode, the loopback modes are selected via the RLB and LLB pins. In Host mode, the RLB and LLB bits in the control registers select the loopback modes.

8.2.1 ANALOG LOOPBACK:

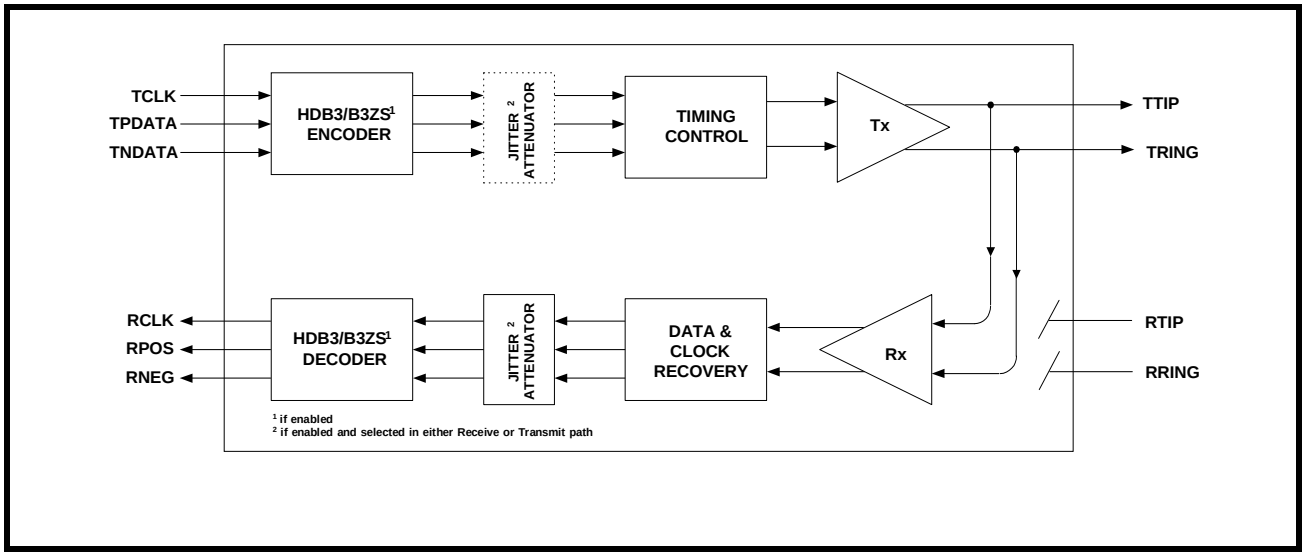
In this mode, the transmitter outputs (TTIP and TRING) are connected internally to the receiver inputs (RTIP and RRING) as shown in Figure 26. Data and clock are output at RCLK, RPOS and RNEG pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

XRT75VL00 can be configured in Analog Loopback either in Hardware mode via the LLB and RLB pins or in Host mode via LLB and RLB bits in the channel control registers.

NOTES:

1. *In the Analog loopback mode, data is also output via TTIP and TRING pins.*
2. *Signals on the RTIP and RRING pins are ignored during analog loopback.*

FIGURE 26. ANALOG LOOPBACK

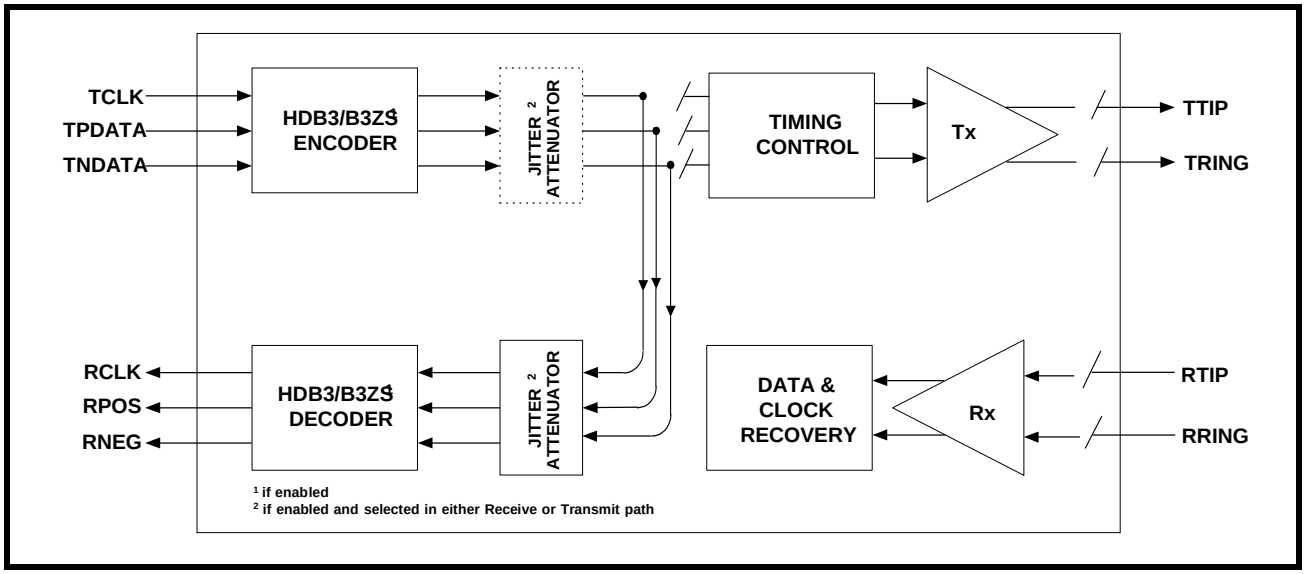


8.2.2 DIGITAL LOOPBACK:

The Digital Loopback function is available either in Hardware mode or Host mode. When the Digital Loopback is selected, the transmit clock (TxClk) and transmit data inputs (TPDATA & TNDATA) are looped back and output onto the RxClk, RPOS and RNEG pins as shown in Figure 27. The data presented on TxClk, TPDATA and TNDATA are not output on the TTIP and TRING pins.This provides the capability to configure the protection card (in redundancy applications) in Digital Loopback mode without affecting the traffic on the primary card.

NOTE: *Signals on the RTIP and RRING pins are ignored during digital loopback.*

FIGURE 27. DIGITAL LOOPBACK



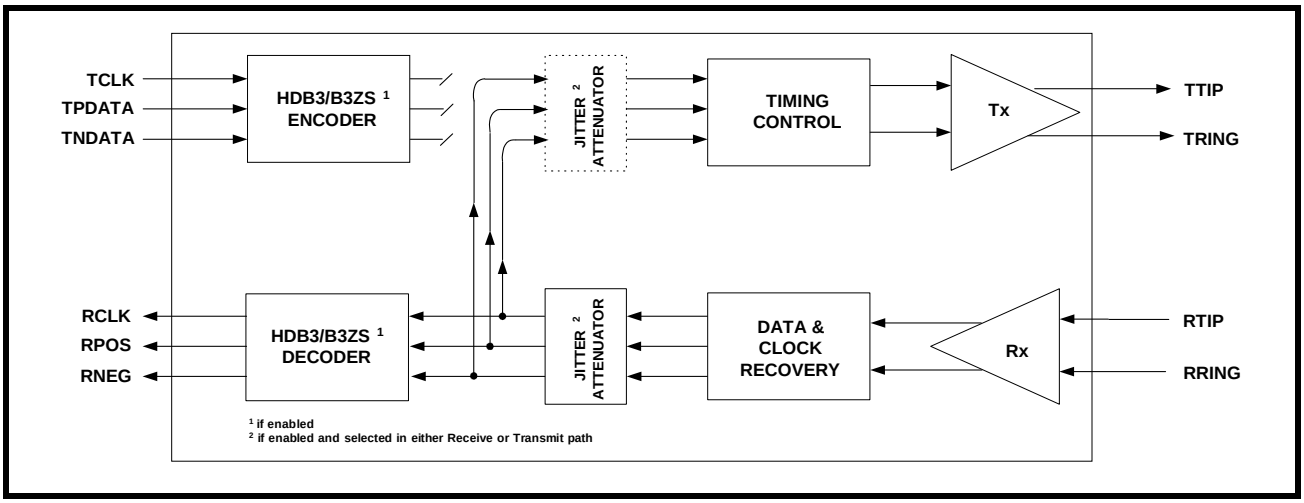
8.2.3 REMOTE LOOPBACK:

With Remote loopback activated as shown in Figure 28,the receive data on RTIP and RRING is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RPOS and RNEG pins.

During the remote loopback mode, if the jitter attenuator is selected in the transmit path, the receive data after the Clock and Data Recovery Block is looped back to the transmit path and pass through the jitter attenuator using RxClk as the transmit timing.

NOTE: *Input signals on TxClk, TPDATA and TNDATA are ignored during Remote loopback.*

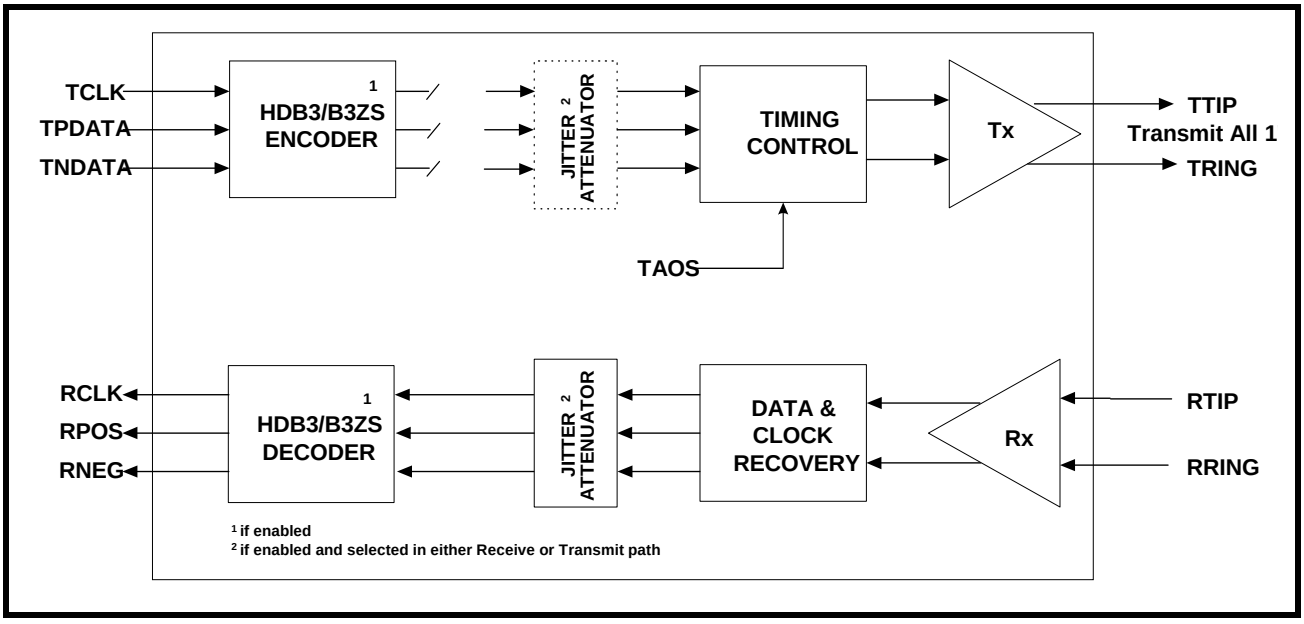
FIGURE 28. REMOTE LOOPBACK



8.3 TRANSMIT ALL ONES (TAOS):

Transmit All Ones (TAOS) can be set either in Hardware mode by pulling the TAOS pins “High” or in Host mode by setting the TAOS control bits to “1” in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all “1’s” pattern on TTIP and TRING pins. The frequency of this “1’s” pattern is determined by TClk.TAOS data path is shown in Figure 29.

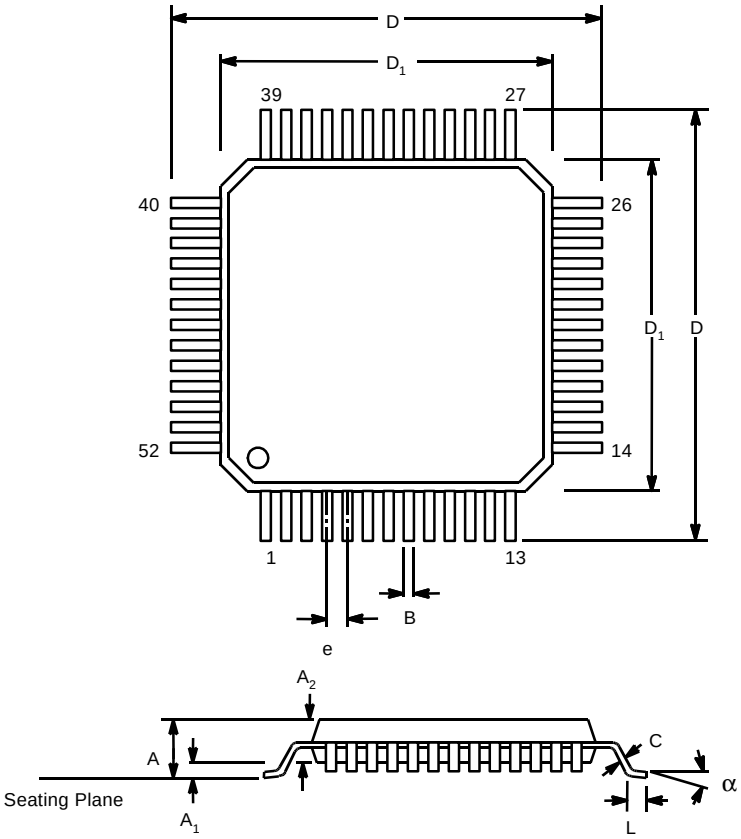
FIGURE 29. TRANSMIT ALL ONES (TAOS)



ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75VL00IV	52 Pin TQFP (10mm x 10mm)	-40℃ to +85℃

PACKAGE DIMENSIONS



Note: The control dimension is the millimeter column

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	7°typ		7°typ	
aaa	-	0.003	-	0.08

REVISION HISTORY

REVISION	DATE	CHANGES MADE
1.0.1	August 2003	Changed ICC and PDD in the electrical characteristics. Removed evaluation schematic. Changed the MTIP/MRING configuration in Figure 16 (Transmit Driver Monitor Setup)..
1.0.2	November 2003	Changed ICC and PDD in the electrical characteristics.
1.0.3	February 2004	Changed the Device ID to reflect the correct value.
1.0.4	January 2005	Corrected the Revision ID.
1.0.5	January 2005	Corrected the revision ID to 1xxxxxxx.
1.0.6	September 2008	Updated datasheet Headers. Corrected Figure 11 block diagram typo. Redefined t_{33} Serial Processor Interface timing.

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