600 V / 4.5 A, High and Low Side Automotive Gate Driver IC

Description

The FAN7191 / FAD7191 is a monolithic high– and low–side gate–driver IC, which can drive high speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse driving capability and minimum cross–conduction.

ON Semiconductor's high–voltage process and common–mode noise canceling technique provide stable operation of high–drivers under high dV/dt noise circumstances. An advanced level–shift circuit allows high–side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop features make this device suitable for controlling direct injection actuators and for use in many automotive DC–DC converter and motor control applications.

Features

- Floating Channel for Bootstrap Operation to +600 V
- 4.5 A Sourcing and 4.5 A Sinking Current Driving Capability
- Common–Mode dV/dt Noise Cancelling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3 V and 5 V Input Logic Compatible
- Output In-phase with Input
- Enable Pin (For 14–SOP Package Only)
- 14–SOP with Separate Signal and Power Ground for Enhanced Noise Immunity
- 14-SOP with Increased Clearance for High Voltage Applications
- Automotive Applications, AEC Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Electric and Hybrid Electric Vehicles
- 48 V Mild Hybrid Vehicles
- Automotive High Voltage DC-DC converters
- Motor Control (Fans, Pumps, Compressors)
- Advanced Fuel Injection Systems
- Starter/Alternator
- Electric Power Steering
- MOSFET and IGBT Driver Applications



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SOIC8 CASE 751EB



SOIC14 CASE 751EF

ORDERING INFORMATION

Part Number	Package	Shipping
FAN7191MX-F085	8-SOP (751EB)	2500 / Tape & Reel
FAD7191M1X	14-SOP (751EF)	2500 / Tape & Reel

Typical Application Circuit



Figure 1. Half–Bridge Application Circuit (8–SOP)



Figure 2. Half-Bridge Application Circuit (14-SOP)

INTERNAL BLOCK DIAGRAM



Figure 3. Functional Block Diagram (8–SOP)



Figure 4. Functional Block Diagram (14–SOP)

Pin Assignment



Figure 5. Pin Assignments (Top View)

Table 1. PIN DEFINITIONS

8–Pin	14–Pin	Name	Description	
1	1	HIN	Logic Input for High–Side Gate Driver Output	
2	2	LIN	Logic Input for Low–Side Gate Driver Output	
3	3	V _{SS}	Logic Ground, Power ground for 8–SOP	
	4	EN	Enable Input (Internal Pull Up)	
	5	СОМ	Power Ground for 14–SOP, Low–side Driver Return	
4	6	LO	Low-Side Driver Output	
5	7	V _{DD}	Low-Side and Logic Power Supply Voltage	
6	11	V _S	High-Side Floating Supply Return	
7	12	НО	High-Side Driver Output	
8	13	VB	High–Side Floating Supply	
	8, 9, 10, 14	NC	No Connect	

Table 2. ABSOLUTE MAXIMUM RATINGS

 $(T_A = -40^{\circ}C \text{ to } 125^{\circ}C, \text{ unless otherwise specified. } V_B, V_{DD} \text{ and } V_{IN} \text{ are referenced to } V_{SS})$

Symbol		Parameter		Min.	Max.	Unit
Vs	High-side offset voltage	High-side offset voltage VS		V _B – 25	V _B + 0.3	V
VB	High-side floating sup	pply voltage VB		-0.3	625	V
V _{HO}	High-side floating out	put voltage		V _S – 0.3	V _B + 0.3	V
V _{DD}	Low-side and logic-fi	xed supply voltage		-0.3	25	V
COM	Power Ground (14–S0	OP)		V _{DD} – 25	V _{DD} + 0.3	V
V _{IN}	Logic Input voltage (H	IN, LIN, EN)		-0.3	V _{DD} + 0.3	V
V _{LO}	Low-Side Output Volt	Low–Side Output Voltage LO (8–SOP)		V _{SS} – 0.3	V _{DD} + 0.3	V
	Low-Side Output Voltage LO (14-Se			COM – 0.3	V _{DD} + 0.3	V
T _{pulse} (Note 4)	Minimum Pulse Width	Minimum Pulse Width		80		ns
d _{VS/dt}	Allowable offset voltage	Allowable offset voltage slew rate			50	V/ns
PD	Power Dissipation, $T_A = 25^{\circ}C$		8-SOP		0.625	W
(Note 1, 2, 3)			14-SOP		0.80	W
θ _{JA}	Thermal Resistance, j	Thermal Resistance, junction-to-ambient			200	°C/W
(Note 1, 2)					156	°C/W
Τ _J	Junction temperature				+150	°C
Τ _S	Storage temperature	orage temperature		-55	+150	°C
ESD		Human Body Model,	8-SOP		3000	V
	Discharge Capability	JESD22–A114	14-SOP		2000	
		Charged Device Mode	l, JESD22–C101		2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on $76.2 \times 114.3 \times 1.6$ mm PCB (FR-4 glass epoxy material).

2. Refer to the following standards: JESD51-2: Integral circuits thermal test method environmental conditions - natural convection.

JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.

3. P_D is the power that raises T_J to 150° C for $T_A = 25^{\circ}$ C. P_D to be derated at higher ambient temperature. 4. Minimum input pulse width that guarantee to produce an output pulse. Valid for turn on and turn off pulse width.

Table 3. RECOMMENDED OPERATING CONDITIONS (V_S, V_{DD} and V_{IN} are referenced to V_{SS})

Symbol	Parameter	Min.	Max.	Unit
VB	High-side floating supply voltage	V _S + 10	V _S + 22	V
V _S	High-side Floating Supply Offset Voltage	6 – V _{BS}	600	V
V _{HO}	High-side Output Voltage	VS	V _B	V
V _{DD}	Low-side and Logic Supply voltage	10	22	V
	Low-side output voltage (8-SOP)	0	V _{DD}	V
V _{LO}	Low-side output voltage (14-SOP)	COM	V _{DD}	V
V _{IN}	Logic input voltage (HIN, LIN, EN)	0	V _{DD}	V
СОМ	Power Ground (14–SOP)	V _{DD} – 22	V _{DD}	V
T _A	Ambient Temperature	-40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

 $(V_{BIAS} (V_{DD}, V_{BS}) = 15.0 \text{ V}, V_S = V_{SS} = COM, T_A = -40^{\circ}\text{C}$ to 125°C, unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM (or V_{SS} in case of 8–SOP). V_S and COM (V_{SS} for 8–SOP) are applicable to the respective outputs HO and LO)

Symbol	Characteristic	Condition	Min.	Тур.	Max.	Unit
OWER SUPPLY	' SECTION (V _{DD} AND V _{BS})			•	•	
V _{DDUV+} V _{BSUV+}	V _{DD} and V _{BS} Supply Under–Voltage Positive–going Threshold		7.8	8.8	9.8	V
V _{DDUV-} V _{BSUV-}	V_{DD} and V_{BS} Supply Under–Voltage Negative Going Threshold		7.2	8.3	9.1	
V _{DDHYS}	V _{DD} supply under-voltage lockout hysteresis			0.5		
I _{LK}	Offset Supply Leakage Current	$V_{B} = V_{S} = 600 V$			50	μA
I _{QBS}	Quiescent V _{BS} Supply Current	$V_{IN} = 0 V \text{ or } 5 V$		45	110	
I _{QDD}	Quiescent V _{DD} Supply Current	$V_{IN} = 0 V \text{ or } 5 V$		75	150	
I _{PBS}	Operating V _{BS} Supply Current	f _{IN} = 20 kHz, RMS value (See Figure 26)		400	800	μA
I _{PDD}	Operating V _{DD} Supply Current	f _{IN} = 20 kHz, RMS value (See Figure 26)		400	800	
OGIC INPUT SE	ECTION (HIN, LIN, EN)		-			
V _{IH}	Logic "1" Input Voltage		2.5			V
VIL	Logic "0" Input Voltage				1.2	
I _{IN+}	Logic "1" Input Bias Current (HIN/LIN)	V _{IN} = 5 V		25	50	μA
I _{IN-}	Logic "0" Input Bias Current (HIN/LIN)	V _{IN} = 0 V		1.0	2.0	
I _{EN+}	Enable High Input Bias Current	EN = 5 V	-100	-50	-10	
I _{EN-}	Enable Low Input Bias Current	EN = 0 V	-140	-75	-20	
R _{IN}	Input Pull-down Resistance		100	200		kΩ
ATE DRIVER O	UTPUT SECTION (HO, LO)					
V _{OH}	High–level Output Voltage, V_{BIAS} – V_O	No Load			1.35	V

V _{OH}	High-level Output Voltage, V _{BIAS} -V _O	No Load			1.35	V
V _{OL}	Low-level Output Voltage, VO	No Load			35	mV
I _{O+} (Note 5)	Output HIGH, Short–circuit Pulsed Current	$V_O = 0 V$, $V_{IN} = 5 V$ with PW < 10 μ s	3.5	4.5		A
I _O _ (Note 5)	Output LOW Short-circuit Pulsed Current	V_{O} = 15 V, V_{IN} = 0 V with PW < 10 μs	3.5	4.5		
V _S	Allowable Negative V _S Pin Voltage for HIN Signal Propagation to HO	V _{BS} = 15V		-9.8	-9.0	V
COM-V _{SS} (Note 5)	Allowable COM–V _{SS} ground offset	14–SOP, V _{DD} = 15 V, V _{SS} = 0 V	-7.0			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Parameters guaranteed by design.

Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS

 $(V_{BIAS} (V_{DD}, V_{BS}) = 15.0 \text{ V}, \text{ V}_{S} = \text{V}_{SS} = \text{COM} = 0 \text{ V}, \text{ T}_{A} = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}, \text{ C}_{LOAD} = 1000 \text{ pF} \text{ unless otherwise specified})$

Symbol	Characteristic	Condition	Min.	Тур.	Max.	Unit
t _{on}	Turn-on Propagation Delay	V _S = 0 V		140	200	ns
t _{off}	Turn-off Propagation Delay	V _S = 0 V		140	200	ns
MT	Delay Matching				55	ns
t _r	Turn-on Rise Time			25	50	ns
t _f	Turn-off Fall Time			25	50	ns

Typical Characteristics









Figure 8. Turn-on Rise Time vs. Temperature

60

50

40

30

20

10

0

-50

-25

0

Delay Matching of turn on (ns)





Figure 9. Turn-off Fall Time vs. Temperature



Figure 10. Turn-on Delay Matching vs. Temperature

Temperature (°C)

50

75

25

Figure 11. Turn-off Delay Matching vs. Temperature

Тур

125

- Max

100

Typical Characteristics (continued)







Typical Characteristics (continued)





Current vs. Temperature

Switching Time Definitions







Figure 27. Input / Output Timing Diagram



Figure 28. Switching Time Waveform Definitions







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