



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

ATP101 — P-Channel Silicon MOSFET General-Purpose Switching Device Applications

Features

- Low ON-resistance
- Slim package
- Halogen free compliance
- Large current
- 4.5V drive
- Protection diode in

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V _{DSS}		-30	V
Gate-to-Source Voltage	V _{GSS}		±20	V
Drain Current (DC)	I _D		-25	A
Drain Current (PW≤10μs)	I _{DP}	PW≤10μs, duty cycle≤1%	-75	A
Allowable Power Dissipation	P _D	Tc=25°C	30	W
Channel Temperature	T _{ch}		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C
Avalanche Energy (Single Pulse) *1	E _{AS}		25	mJ
Avalanche Current *2	I _{AV}		-13	A

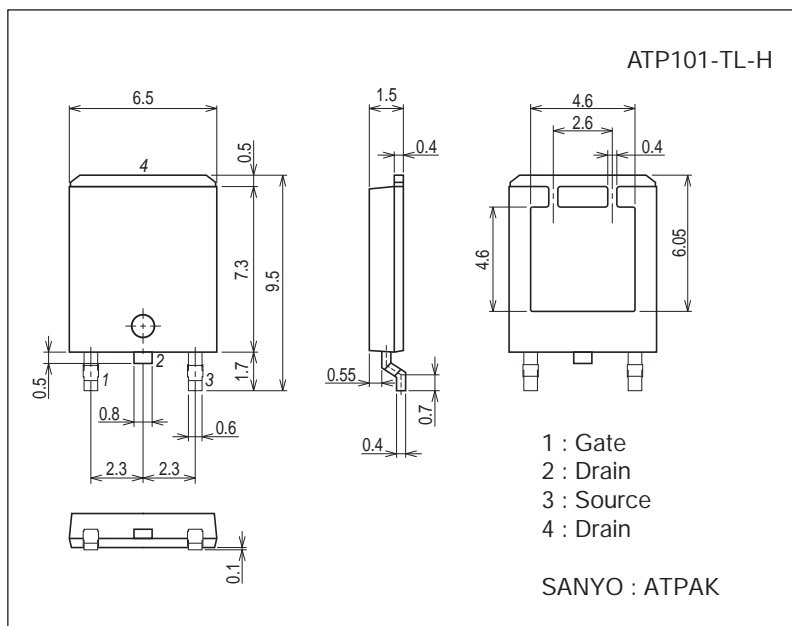
Note : *1 V_{DD}=-10V, L=200μH, I_{AV}=-13A

*2 L≤200μH, Single pulse

Package Dimensions

unit : mm (typ)

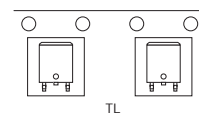
7057-001



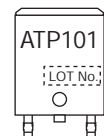
Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

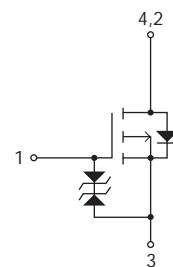
Packing Type: TL



Marking



Electrical Connection

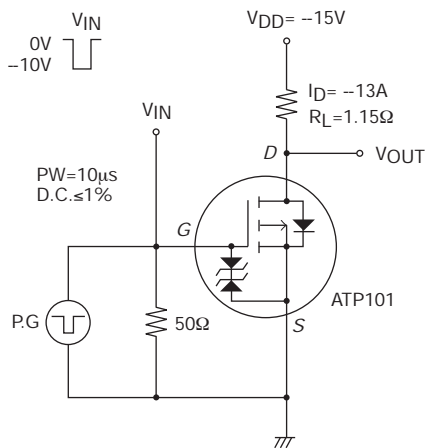


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Electrical Characteristics at Ta=25°C

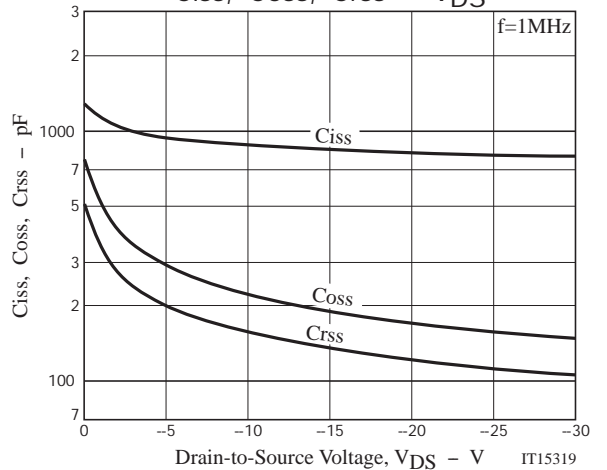
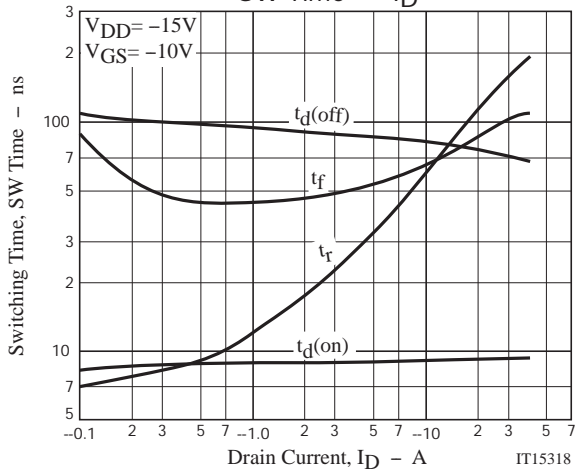
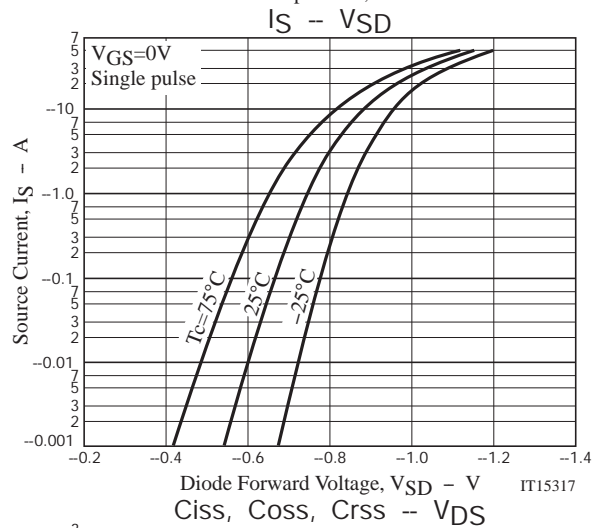
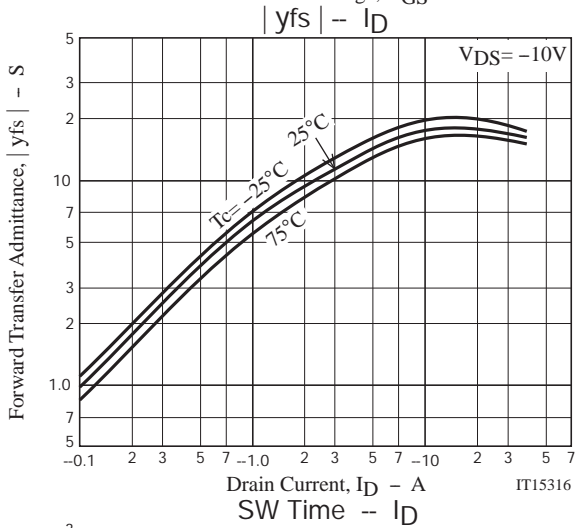
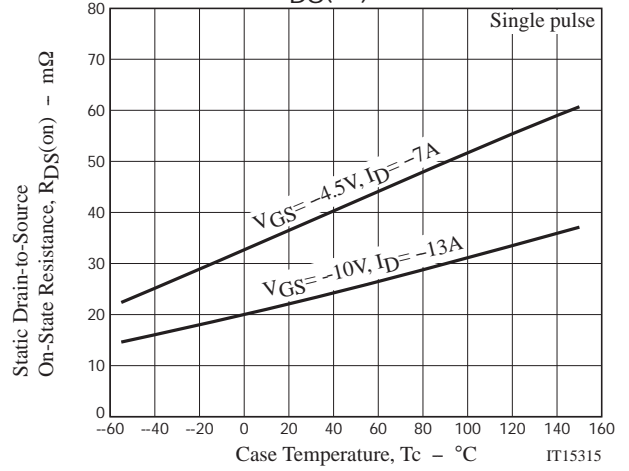
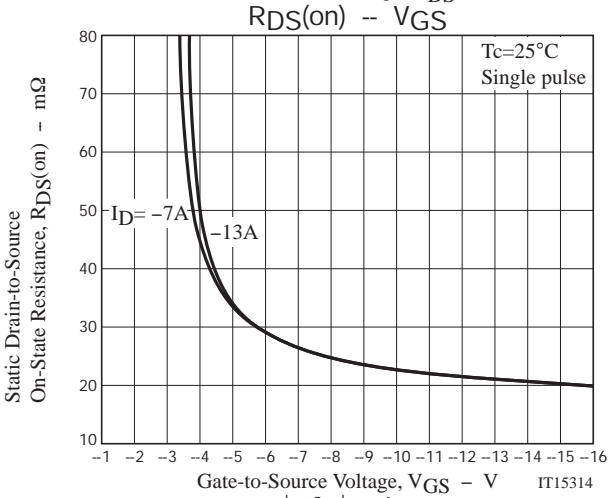
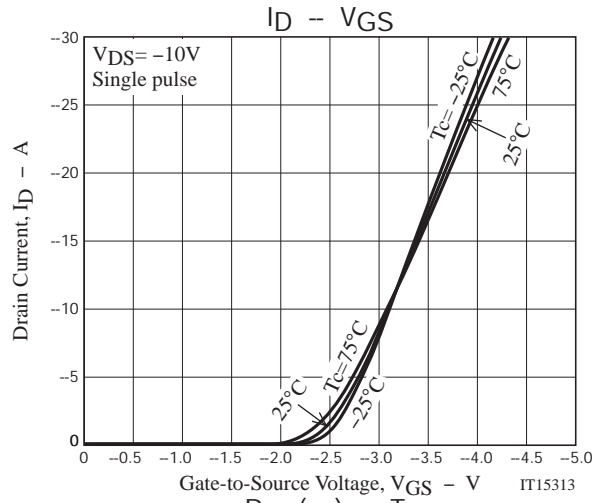
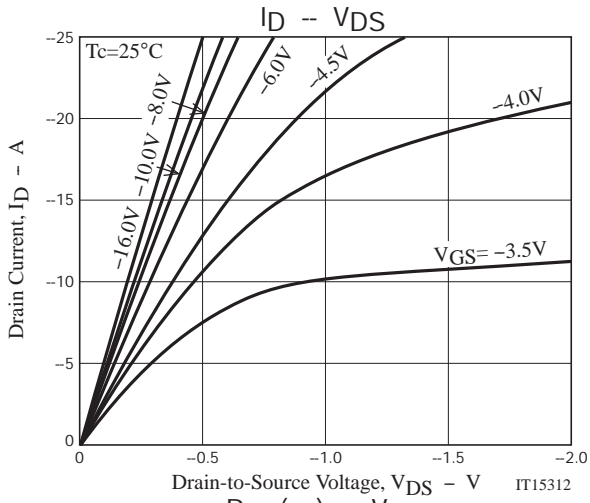
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	V(BR)DSS	I _D =-1mA, V _{GS} =0V	-30			V
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±16V, V _{DS} =0V			±10	μA
Cutoff Voltage	V _{GS(off)}	V _{DS} =-10V, I _D =-1mA	-1.2		-2.6	V
Forward Transfer Admittance	y _{fs}	V _{DS} =-10V, I _D =-13A		17		S
Static Drain-to-Source On-State Resistance	R _{DS(on)1}	I _D =-13A, V _{GS} =-10V		23	30	mΩ
	R _{DS(on)2}	I _D =-7A, V _{GS} =-4.5V		36	51	mΩ
Input Capacitance	C _{iss}	V _{DS} =-10V, f=1MHz		875		pF
Output Capacitance	C _{oss}			220		pF
Reverse Transfer Capacitance	C _{rss}			155		pF
Turn-ON Delay Time	t _{d(on)}	See specified Test Circuit.		9.2		ns
Rise Time	t _r			70		ns
Turn-OFF Delay Time	t _{d(off)}			80		ns
Fall Time	t _f			70		ns
Total Gate Charge	Q _g		V _{DS} =-15V, V _{GS} =-10V, I _D =-25A		18.5	
Gate-to-Source Charge	Q _{gs}			3.2		nC
Gate-to-Drain "Miller" Charge	Q _{gd}			4.0		nC
Diode Forward Voltage	V _{SD}	I _S =-25A, V _{GS} =0V		-0.99	-1.5	V

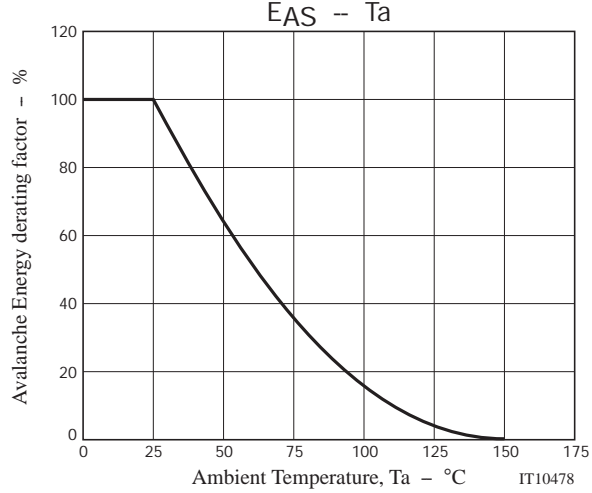
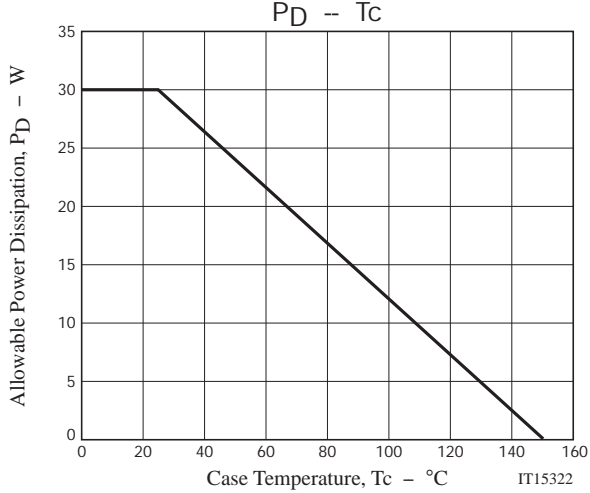
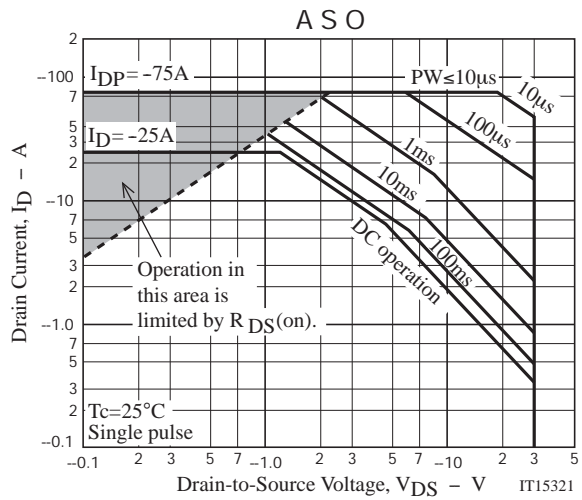
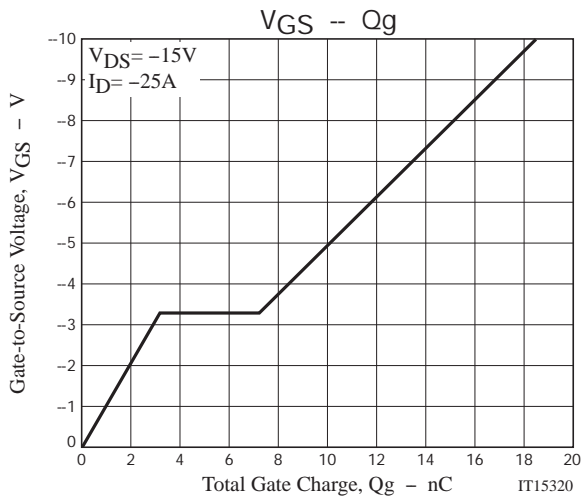
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
ATP101-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free





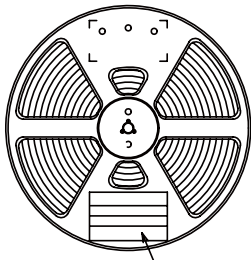
Taping Specification

ATP101-TL-H

1. Packing Format (TL)

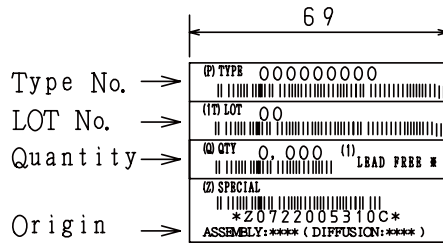
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

Packing method



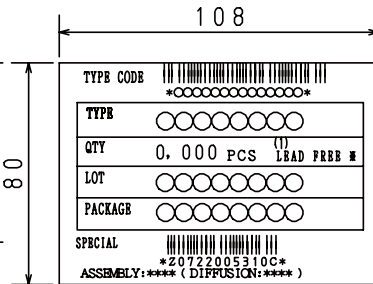
Reel label

Reel label, Inner box label
(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



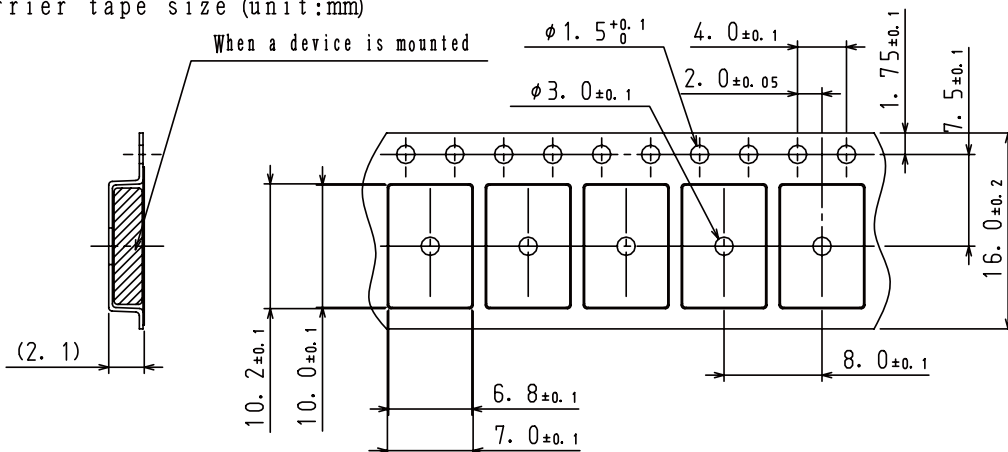
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

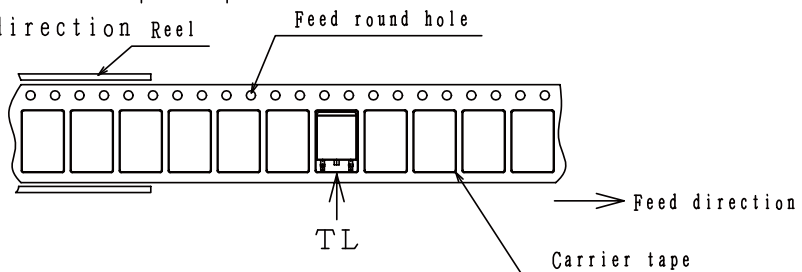
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel

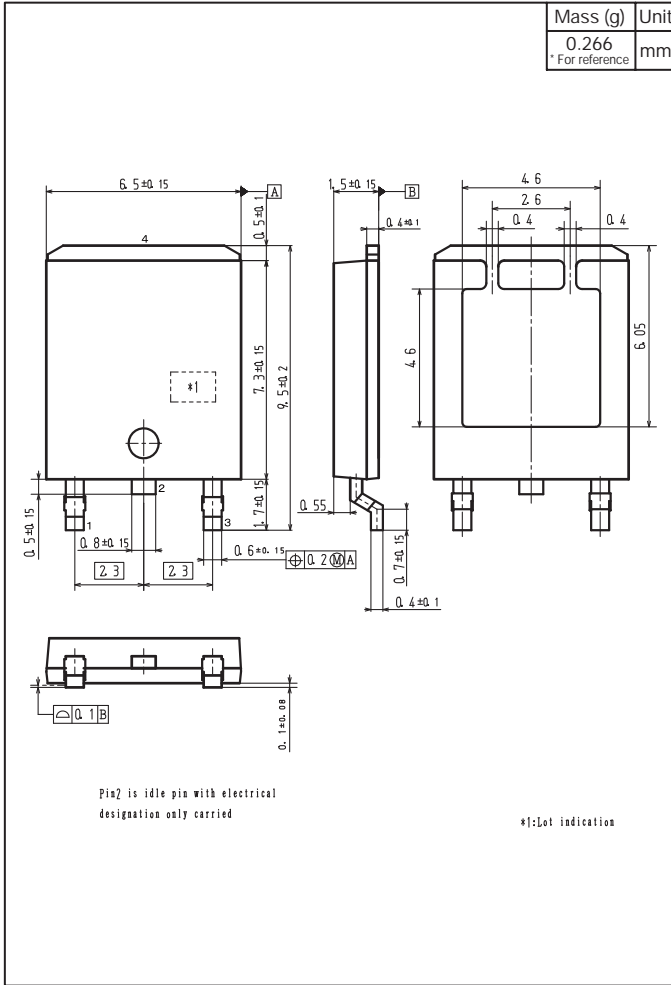


The one electrode terminals on feed hole side...TL

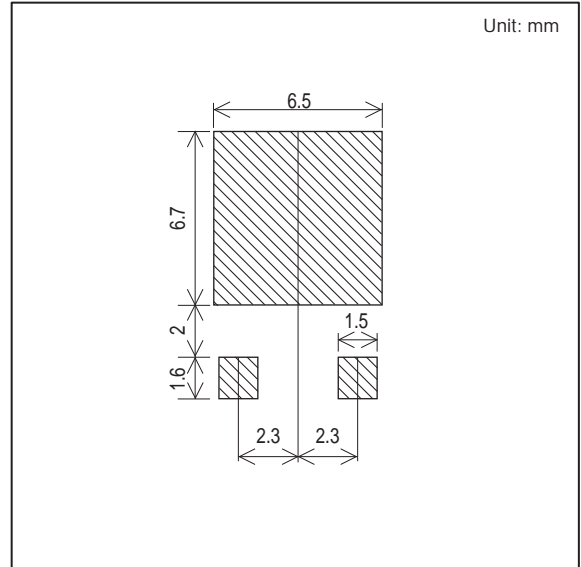
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Outline Drawing

ATP101-TL-H



Land Pattern Example



Note on usage : Since the ATP101 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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