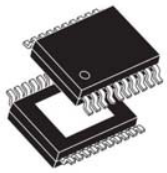
PM8803

High-efficiency, IEEE 802.3at compliant integrated PoE-PD interface and PWM controller

Datasheet - production data



HTSSOP20

Features

- IEEE 802.3at compliant PD interface
- Works with power supplied from Ethernet LAN cables or from local auxiliary sources
- Successful IEEE802.3at Layer1 classification indicator
- Integrated 100 V, 0.45 Ω, 1 A hot-swap MOSFET
- Accurate 140 mA typ. inrush current level
- Programmable classification current
- Programmable DC current limit up to 1 A
- Integrated high voltage start-up bias regulator
- Thermal shutdown protection
- Current mode pulse width modulator
- Programmable oscillator frequency
- 80% maximum duty cycle with internal slope compensation
- Support for flyback, forward, forward active clamp, flyback with synchronous rectification

Applications

- VoIP phones, WLAN AP
- WiMAX CPEs
- Security cameras
- PoE/PoE+ powered device appliances

Description

The PM8803 integrates a Power over Ethernet (PoE) interface and a current mode PWM controller to simplify the design of the power supply sections of all powered devices. The PoE/PoE+ interface includes all functions required by the IEEE 802.3at as well as detection, classification, undervoltage lockout (UVLO) and inrush current limitation.

The PM8803 specifically performs IEEE802.3at Layer 1 hardware classification, providing the system with an indication of Type 2 PSE successful detection.

The PM8803 has been designed to work with power either from the Ethernet cable or from an external power source such as a wall adapter, ensuring the priority of the auxiliary source over the PoE. The DC-DC section of the PM8803 features a programmable oscillator frequency, an adjustable slope compensation, dual complementary low-side drivers, programmable dead time and an internal temperature sensor.

The PM8803 targets high-efficiency conversion under all load conditions supporting flyback, forward, forward with active clamp converters and synchronous rectification.

Table 1: Device summary

Part number	Package	Packing
PM8803	HTSSOP20	Tube
PM8803TR	HTSSOP20	Tape and reel

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1 Typical application circuits and block diagrams

1.1 Application circuits

Figure 1: Simplified application schematic for powered devices using the PM8803 in forward active clamp configuration

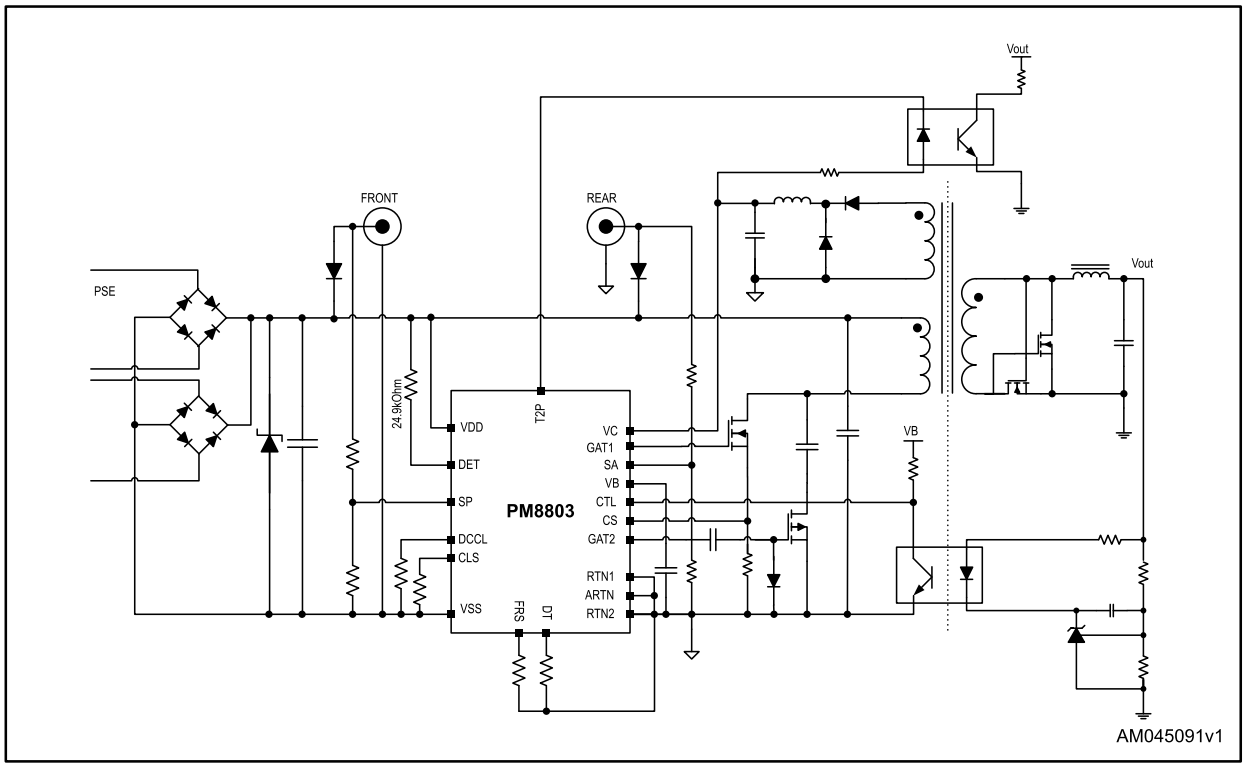
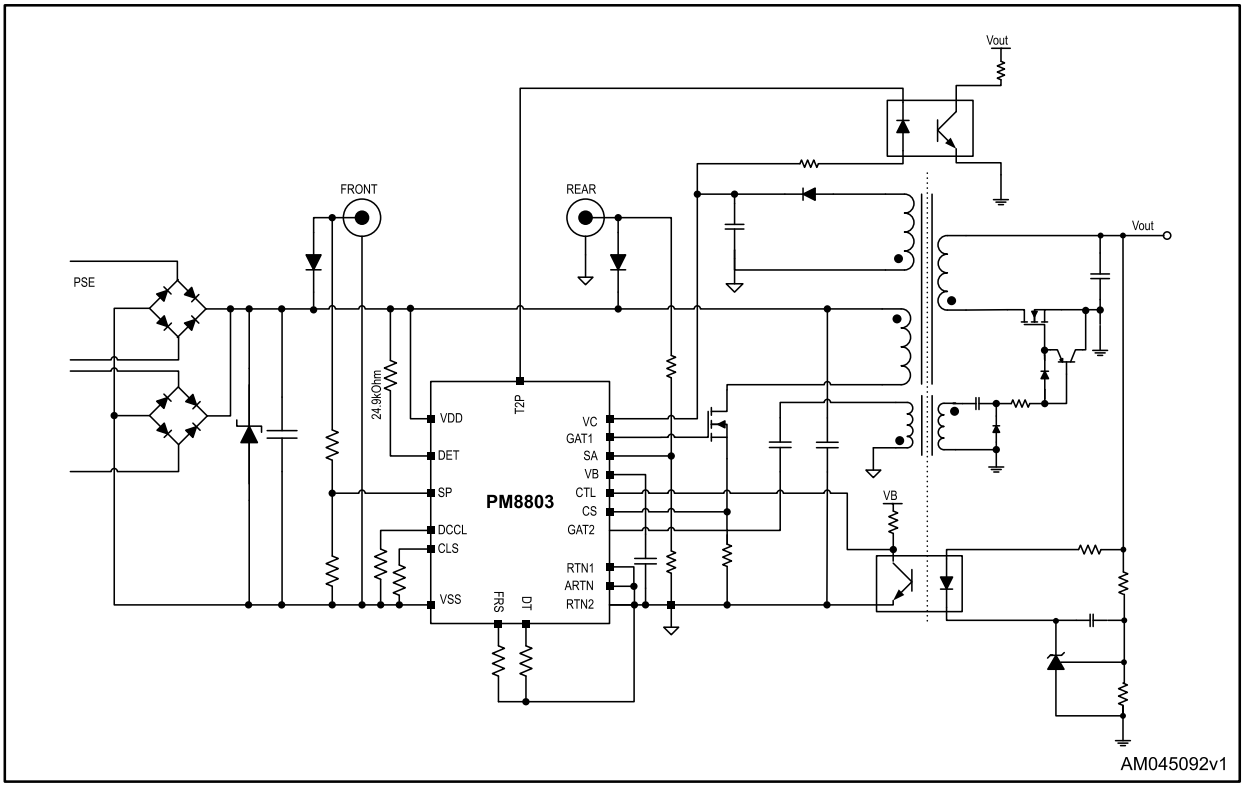


Figure 2: Simplified application schematic for powered devices using the PM8803 in synchronous flyback configuration



1.2 Block diagrams

Figure 3: PM8803 internal block diagram

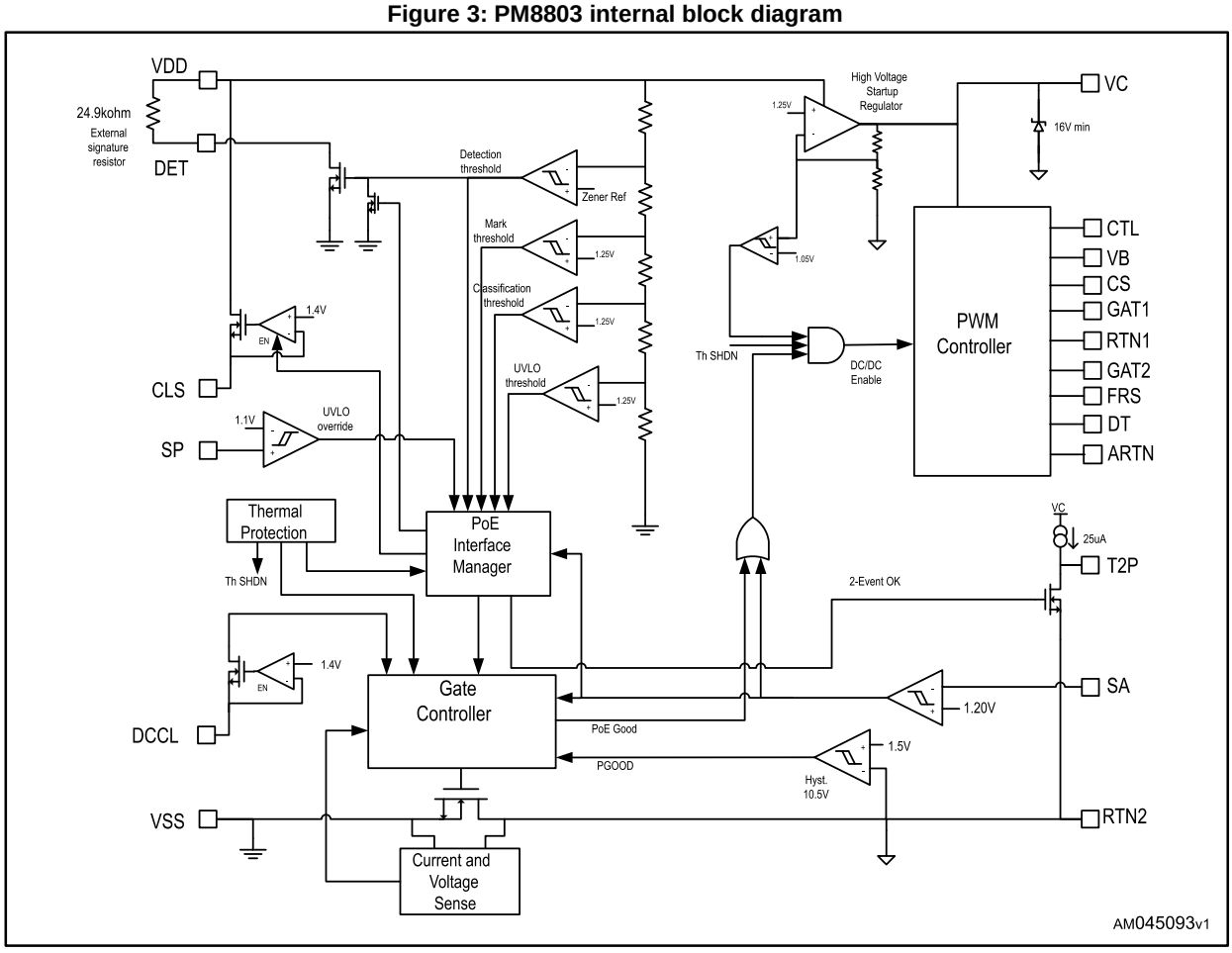
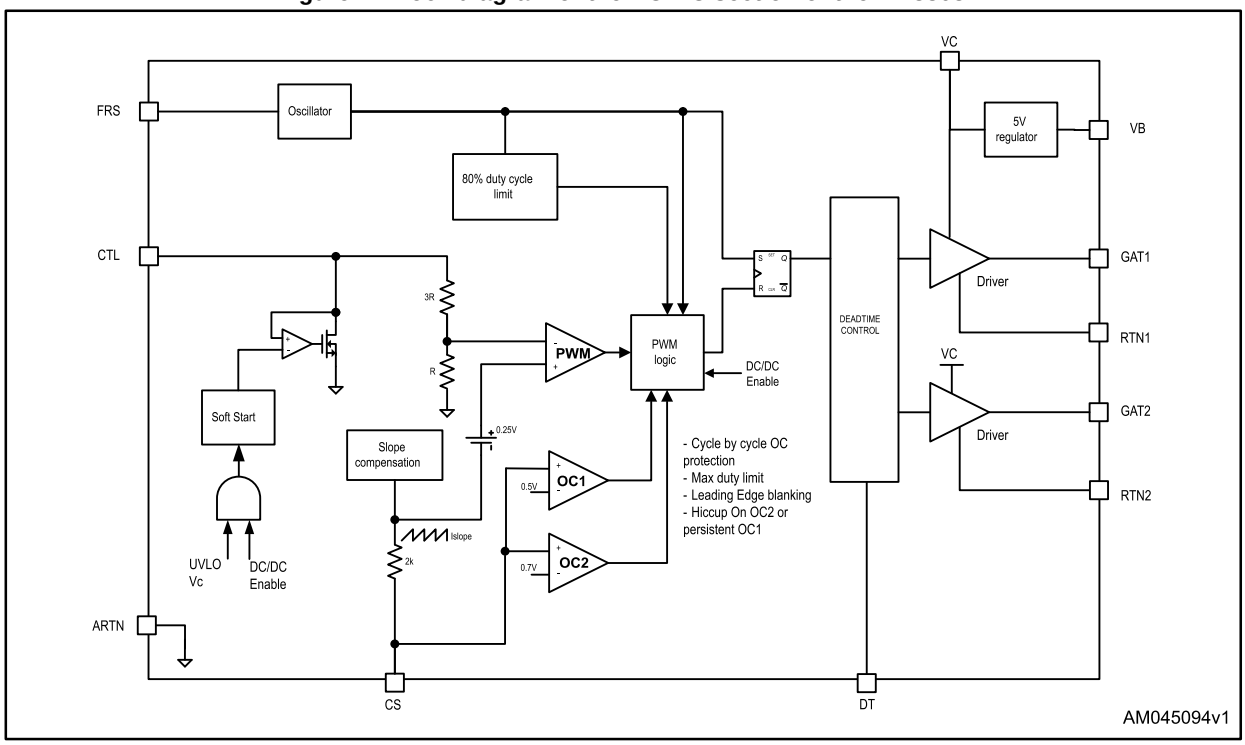


Figure 4: Block diagram of the DC-DC section of the PM8803



2 Pin descriptions and connection diagrams

Figure 5: Pin connections (top view)

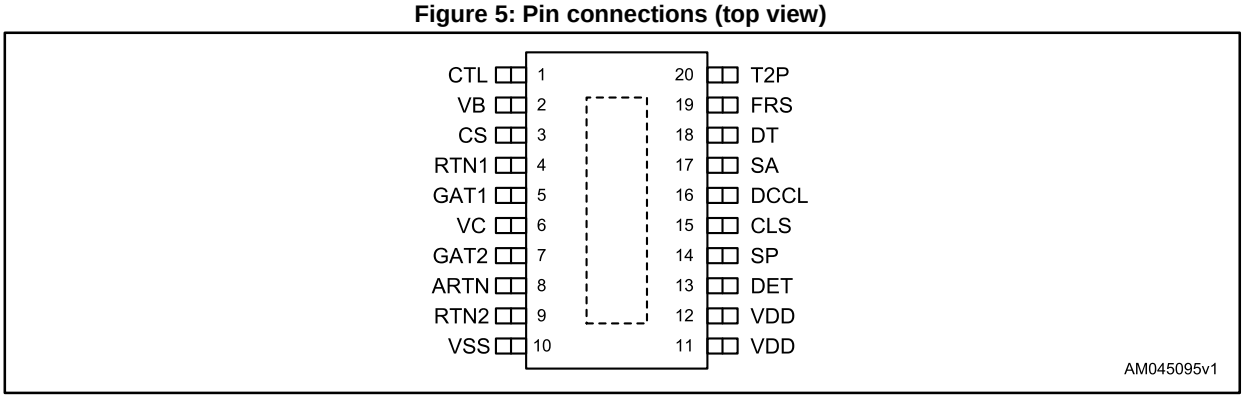


Table 2: Pin descriptions

Pin	Name	Function
1	CTL	Input of the pulse width modulator. CTL pull-up to VB is provided by an external resistor, which may be used to bias an optocoupler transistor.
2	VB	5 V, up to 10 mA bias rail. This reference voltage can be used to bias an optocoupler transistor.
3	CS	Current sense input for current mode control and overcurrent protection. Current sensing is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5 V, the GAT1 pin switches low for cycle-by-cycle current limiting. CS is internally held low for 60 ns after GAT1 switches high to blank leading edge current spikes.
4	RTN1	Power ground for the GAT1 driver. This pin must be connected to RTN2 and ARTN.
5	GAT1	Main gate driver output of the PWM controller. DC-DC converter gate driver output with 1 A peak sink-source current capability. (5 Ω typ. MOSFETs).
6	VC	Output of the internal high voltage regulator. When the auxiliary transformer winding (if used) raises the voltage on this pin above the 8 V typ. set point regulation, the internal regulator shuts down, reducing the internal power dissipation. Filter this pin with 1 µF typ. connected to ground.
7	GAT2	Secondary gate driver output. AUX gate driver output for active clamp or synchronous rectification designs. 1 A peak sink-source current capability (5 Ω typ. MOSFETs).
8	ARTN	Analog PWM supply ground. RTN for sensitive analog circuitry including the SMPS current limit amplifier.
9	RTN2	Power ground for the secondary gate driver. This pin is also connected to the drain of the internal current limiting power MOSFET which closes VSS to the return path of the DC-DC converter. This pin must be connected to RTN1 and ARTN
10	VSS	System low potential input. Diode "OR'd" to the RJ45 connector and PSE's -48 V supply, it is the most negative input potential.
11	VDD	System high potential input. The diode "OR" of several lines entering the PD; it is the most positive input potential.

Pin	Name	Function
12	VDD	System high potential input. The diode "OR" of several lines entering the PD; it is the most positive input potential.
13	DET	Detection resistor pin. Connect the signature resistance between the DET pin and VDD. Current flows through the resistor only during the detection phase. This pin is 100 V rated with negligible resistance with respect to the external 24.9 kΩ.
14	SP	Front auxiliary start-up pin. Pulling up this pin to the auxiliary source changes the internal UVLO settings and allows PD to be powered with voltage lower than nominal PoE voltages. Default inrush and DC current protection are active. Use a resistor voltage divider from the auxiliary voltage to VSS to connect this low voltage rating pin. Connect this pin to VSS if not used.
15	CLS	Classification resistor pin. Connect the classification programming resistor from this pin to VSS.
16	DCCL	DC current limit. A resistor between this pin and VSS sets the current limit for the interface section of the PM8803. It can be set to exceed the IEEE802.3at current limit. Leave the pin open for standard IEEE 802.3at applications.
17	SA	Rear auxiliary start-up pin. Pulling up this pin gives high priority to an auxiliary power source like an external wall adapter. Use a resistor voltage divider from the auxiliary voltage to ARTN to connect this low voltage rating pin. Connect this pin to ARTN if not used.
18	DT	Delay time set. A resistor connected from this pin to ARTN sets the delay time between GAT1 and GAT2. This pin cannot be left open.
19	FRS	Switching frequency set. An external resistor connected from FRS to ARTN sets the oscillator frequency.
20	T2P	Successful 2-event classification indicator. T2P open drain signal assertion happens when powered by a PSE performing a 2-event classification. T2P is an active-low signal.
	EP	Exposed Pad. Connect this to a PCB copper plane to improve heat dissipation; it must be electrically connected to VSS.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Parameter	Value	Unit
VDD, DET, ARTN to VSS	-0.3 to 100	V
CLS, SP, DCCL to VSS	-0.3 to 3.6	V
VC to ARTN	-0.3 to 16	V
GAT1, GAT2, T2P to ARTN	-0.3 to VC+0.3	V
CTL, VB, DT to ARTN	-0.3 to 5.5	V
FRS, SA, CS to ARTN	-0.3 to 3.6	V
RTN1, RTN2 to ARTN (1)	-0.3 to 0.3	V
ESD HBM	2	KV
ESD CDM	500	V
Operating junction temperature (2)	-40 to 150	°C
Storage temperature	-40 to 150	°C

Notes:

(1) See *Section 7: "Layout guidelines"* for more details.

(2)Internally limited to 160 °C typ. with internal overtemperature protection circuit.

Absolute maximum ratings are limits beyond which damage to the device may occur.

3.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Max. thermal resistance junction-to-ambient (1)	40	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Operative junction temperature range	-40 to 125	°C
T_A	Operative ambient temperature range	-40 to 85	°C

Notes:

(1)Package mounted on a 4-layer board (2 signals + 2 powers), CU thickness 35 micron, with 6-8 vias on the exposed pad copper area connected to an inner power plane.

3.3 Electrical characteristics

VDD = 48 V, VC = not loaded, C_{VC} = 1 µF, VB = not loaded, C_{VB} = 1 µF, GAT1 and GAT2 = not loaded, T_A = 25 °C unless otherwise specified.

Values in bold apply over the full operating ambient temperature range.

Table 5: Electrical characteristics - interface section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Detection and classification						
	Signature enable	VDD rising			**1.5**	V
	Signature pull-down resistance	Within signature range		150	**350**	W
	Signature disable	VDD rising	**10.3**	10.8	**11.3**	V
	Classification enable	VDD rising	**11.3**	12	12.7	V
	Classification turn-off	VDD rising	**21.5**	23.0	**24.5**	V
	Mark event threshold / Classification turn-off	VDD falling	**9**	10	**11**	V
	Classification reset threshold	VDD falling	**3**	4	**5**	V
	CLS voltage	Within classification range with 44 mA load	**1.3**	1.4	**1.5**	V
	CLS max. current capability	Within classification range with CLS pin grounded	**50**	65	**80**	mA
Bias current						
I_{DD}	VDD supply current during detection	VDD = 8 V			10	µA
	VDD supply current during classification			900	**1200**	µA
	VDD supply current during mark event		**500**	800	**1100**	µA
Undervoltage lockout						
V_{UVLO_R}	UVLO release	VIN rising	**34**	35	**36.5**	V
V_{UVLO_F}	UVLO lockout	VIN falling	**30**	31	**32.5**	V
	UVLO hysteresis		**3.5**	4	**4.5**	V
Hot-swap MOSFET						
$R_{DS(on)}$	MOSFET resistance			0.45	**1**	Ω
	Default inrush current limit		**125**	140	**155**	mA
	Default DC current limit		**590**	640	**690**	mA
DCCL adjust						
	DCCL voltage			1.4		V
	DC current limit selection range		140		1000	mA
	Adjustable DC current limit precision	R_{DCCL} = 30 to 150 kΩ	-15		+15	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Inrush to DC current switchover						
	V_{DS} required for inrush to DC switchover	V_{DS} falling - hot-swap MOSFET closing	**1.35**	1.50	**1.75**	V
	V_{GS} required for inrush to DC switchover	V_{DS} falling - hot-swap MOSFET closing. Guaranteed by design		2		V
	V_{DS} required for inrush to DC switchover	V_{DS} rising - hot-swap MOSFET opening	**11**	12	**13**	V
Front auxiliary source detection						
	SP threshold	Voltage rising	1.0	1.1	1.2	V
	SP hysteresis			200		mV
	Minimum VDD voltage for front auxiliary operations		13	15		V

Table 6: Electrical characteristics - SMPS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillator						
F_{OSC}	Frequency accuracy	In the range 100 to 500 kHz		+/-10		%
	Frequency programmability	R_{FRS} = 100 kΩ	**220**	245	**270**	kHz
		R_{FRS} = 47.5 kΩ	**445**	495	**545**	kHz
	Frequency range		100		1000	kHz
	FRS voltage		**1.20**	1.25	**1.30**	V
Delaytime						
	GAT1 to GAT2 delay time	RDT = 20 kΩ, GAT1 and GAT2 open		32		ns
		RDT = 200 kΩ, GAT1 and GAT2 open		320		ns
	DT voltage		**1.20**	1.25	**1.30**	V
Soft-start						
T_{SS}	Soft-start time	Over CTL full range (0 to 3 V), at F_{OSC} = 250 kHz		12.3		ms
Current limit						
	Delay-to-output	Guaranteed by design		20		ns
	Cycle-by-cycle current limit threshold voltage		**0.44**	0.50	**0.56**	V
	Leading edge blanking time		**45**	60	**75**	ns
	Slope compensation current	Sourced by CS pin		45		µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PWM comparator						
	Delay-to-output	Guaranteed by design		25		ns
	Minimum duty cycle	CTL = 0, CS = 0			0	%
	Maximum duty cycle	CTL = 2 V, CS = 0, F_{OSC} = 250 kHz	**75**	80	**85**	%
	CTL to PWM gain	Guaranteed by design		1 : 4		
	CTL operative range		1		3	V
Output driver GAT1						
	Output high	I_{GD} = 100 mA		VC-0.25	**VC-0.5**	V
	Output low	I_{GD} = -100 mA		0.25	**0.5**	V
	Fall time	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		40		ns
	Rise time	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		45		ns
	Peak source current	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		800		mA
	Peak sink current	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		1		A
Output driver GAT2						
	Output high	I_{GD} = 100 mA		VC-0.25	VC-0.5	V
	Output low	I_{GD} = -100 mA		0.25	0.5	V
	Fall time	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		40		ns
	Rise time	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		45		ns
	Peak source current	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		800		mA
	Peak sink current	C_{LOAD} = 3.3 nF, VC = 10 V guaranteed by design		1		A
Thermal shutdown						
	Shutdown temperature	Always active; guaranteed by design		160		°C
	Shutdown hysteresis			30		°C
VC regulation						
VC	Internal default		**7.7**	8.0	**8.3**	V
	VC current limit	IB = 0; GAT1, GAT2 = open	**14**	20		mA
VC_{UVLO}	Internal default UVLO, release	VC rising		VC-0.3		V
	Internal default UVLO, lockout	VC falling	5.7	6.0	**6.3**	V
	VC regulator dropout	IC = 10 mA; GAT1, GAT2 = open		2		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VB regulation						
VB	Internal default		**4.85**	5.0	**5.15**	V
	VB current limit	IC = 0; GAT1, GAT2 = open	5		10	mA
	VB sink current capability				**1**	mA
Rear auxiliary source detection						
	SA threshold		**1.1**	1.2	**1.3**	V
	SA hysteresis			180		mV
	Minimum VDD voltage for rear auxiliary operations		13	15		V
T2P flag						
	T2P pull-up current		**20**	25	**30**	µA
	T2P pull-down resistance			45	**75**	Ω
Device current consumption						
	VD quiescent current	VD > V_{UVLO_R},VC = 12 V, CTL = 0		1.25	**1.5**	mA
	VC quiescent current	VD > V_{UVLO_R},VC = 12 V, CTL = 0		2	**2.5**	mA

Minimum and maximum limits are guaranteed by test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25 °C, and are provided for reference only.

The device thermal limitations could limit useful operating range.

The VC regulator is intended for internal use only as the start-up supply of the PM8803; any additional external VC current, including the VB regulator current and external MOSFET driving current, has to be limited within the specified max. current limit.

4 PD interface

4.1 Detection

In Power over Ethernet systems, the power sourcing equipment (PSE) senses the Ethernet connection to detect if the powered device (PD) is plugged into the cable termination by applying a small voltage (2.7 V to 10 V) on the Ethernet cable and measures the equivalent resistance in at least two consecutive steps. During this phase, the PD must present a resistance between 23.75 kW and 26.25 kΩ.

The signature resistor must be connected between the DET and VDD pins. This series pass transistor (see *Figure 3: "PM8803 internal block diagram"*) is enabled only during the detection phase. No current flows through the signature resistor for the rest of the operative phases (classification and turn-on).

The typical voltage drop of the diode bridges has to be taken into account to select the value of the detection resistance. The typical used value in most cases is 24.9 kΩ.

During detection, most of circuits inside the PM8803 are disabled to minimize the offset current.

4.2 Classification

The classification phase in a PoE network is the feature that allows PSE to plan and allocate the available power to the appliances connected to various Ethernet ports.

The PM8803 complies with both IEEE802.3at 1-event and 2-event classification schemes. 1-event classification in IEEE802.3at is the same as specified in the IEEE 802.3af standard, which divides the power levels below 12.95 W into 5 classes (Class 0 to Class 4).

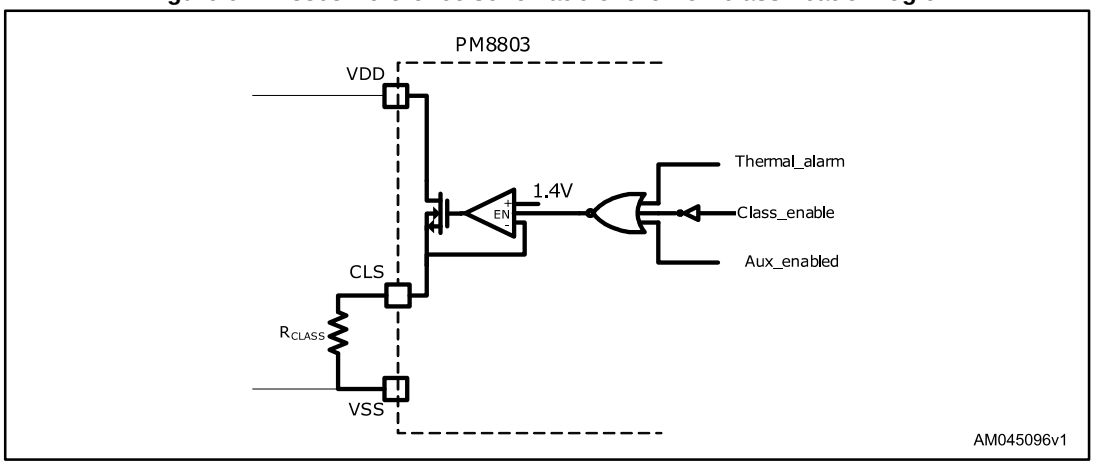
Class 4 is reserved in IEEE802.3af, while in IEEE802.3at Class 4 identifies Type 2 PDs requiring up to 25.5 W.

A Type 2 PD provides a Class 4 signature during physical layer classification, understands 2-event classification and data link layer classification.

Figure 8: "T2P signal when connected to PSE supporting 2-event classification" represent the voltage at the input of the PD when connected to a PSE performing 2-event classification. A Type 2 PD presents in both classification events a Class 4 current while during the so called “mark-event”, between the 2 classification fingers, the PD presents an invalid signature resistance.

To support the classification function, an equivalent programmable constant current generator has been implemented. *Figure 6: "PM8803: reference schematic of the PoE classification logic"* depicts a primary schematic of the classification circuit. Following the successful completion of the detection phase, the voltage of the CLS pin is set to the 1.4 V voltage reference and a pass transistor connects the VIN pin to the CLS pin.

Figure 6: PM8803: reference schematic of the PoE classification logic



The classification resistor can be disconnected for the following reasons:

- Classification has been successfully completed
- Auxiliary power source has been connected
- The device is in thermal protection

Designers can set the current by changing the value of the external resistor according to the following table:

Table 7: Value of the external classification resistor for the different PD classes of power

Class	PD max. average power (W)	R_{CLS} (Ω)
0	13	2k
1	3.84	150
2	6.49	80.6
3	13	51.1
4	25.5	35.6

4.3 Indication of successful 2-event classification

The PM8803 recognizes whether it is connected to a PSE performing 1-event or 2-event physical layer classification by asserting the T2P signal.

T2P is an open-drain, active-low signal which is asserted if a successful 2-event classification event is completed.

T2P is asserted as soon as the high voltage start-up regulator output is stable. (see *Figure 7: "T2P signal when connected to PSE supporting 1-event classification"* and *Figure 8: "T2P signal when connected to PSE supporting 2-event classification"* for timing sequences). If the PM8803 detects a 1-event classification or no classification, T2P is pulled up and the main circuit in the PD can establish an LLDP connection to negotiate the power. No LLDP response from the PSE means that the PD is connected to a Type 1 PSE, and only 13 W input power is available.

A low T2P signal after the turn-on phase of the POE means that the PD is connected to a Type 2, 2-event physical layer classification PSE which may allocate the power either through further LLDP negotiation or directly feed the PD with the required power.

In isolated applications, the main circuits and the PM8803 are at both sides of the galvanic isolation. The T2P signal is normally connected to an optocoupler to pass the Type 2, 2-event PSE detection information to the main circuit in the PD system.

Figure 7: T2P signal when connected to PSE supporting 1-event classification

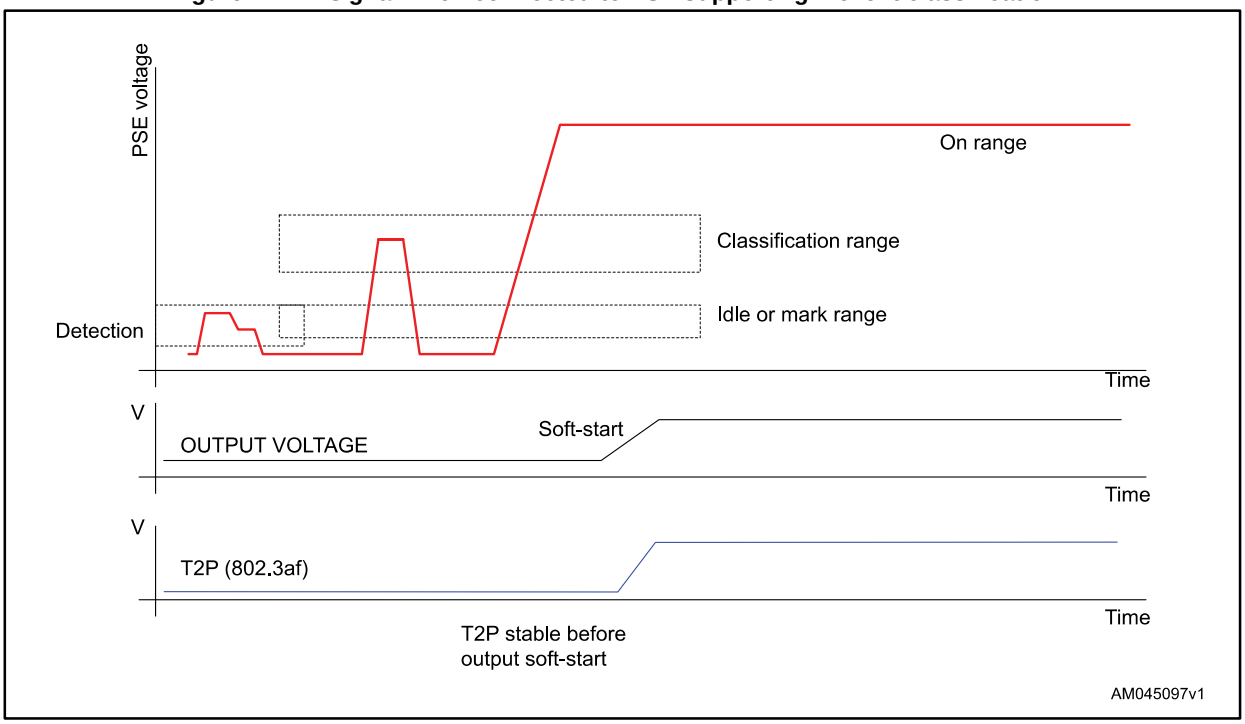
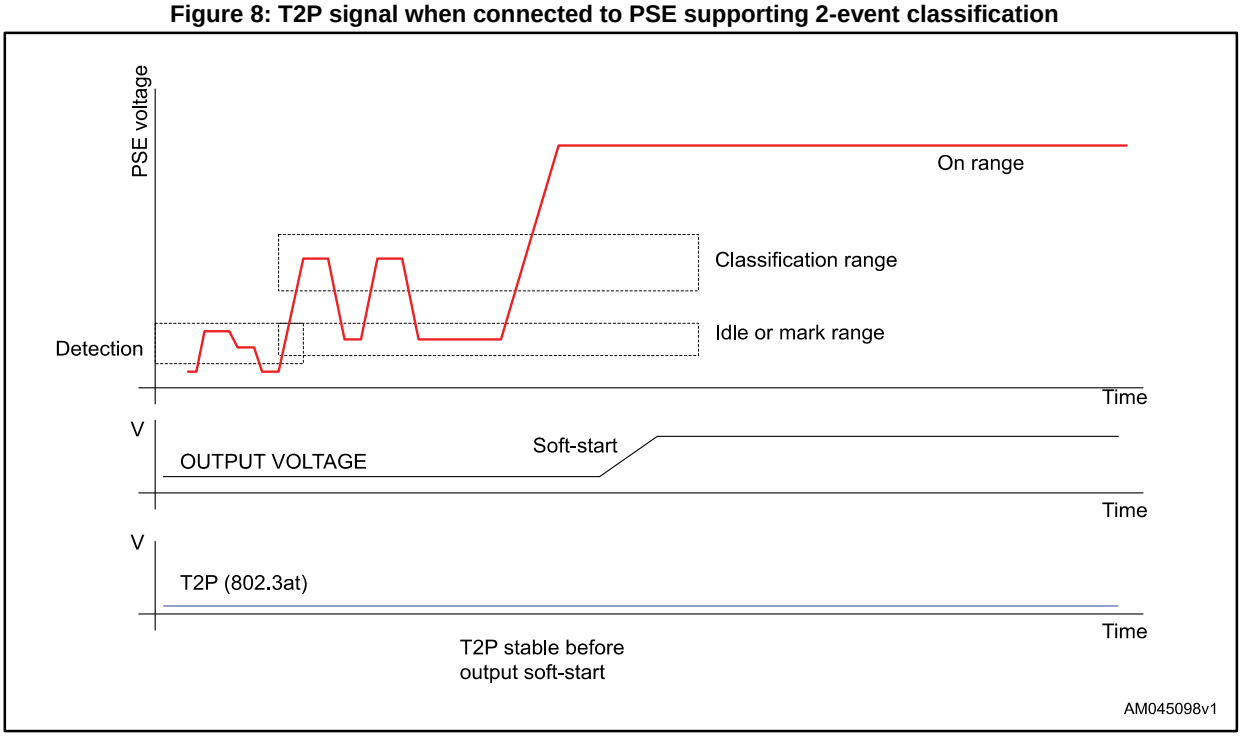


Figure 8: T2P signal when connected to PSE supporting 2-event classification



4.4 Undervoltage lockout

After the classification is completed, the PSE raises the voltage to provide the power devices with the negotiated power. During the transition from low to operating voltage, the internal UVLO is released and the hot-swap MOSFET is active, starting the inrush sequence.

The PM8803 implements the UVLO mechanism by setting 2 internal thresholds on the voltage across the VDD-VSS pins; one is to switch on the hot-swap (V_{UVLO_R}), while the other is to switch off the hot-swap MOSFET upon detection of a supply voltage drop (V_{UVLO_F}) from normal operating conditions.

No additional external component is required to comply with the IEEE requirements. The thermal protection alarm overrides the gate driving of the MOS, immediately switching off the MOS itself in case of the device overheating. The hot-swap is also bypassed in auxiliary source topology, supplying directly the PWM section of the PM8803 and bypassing the hot-swap MOSFET.

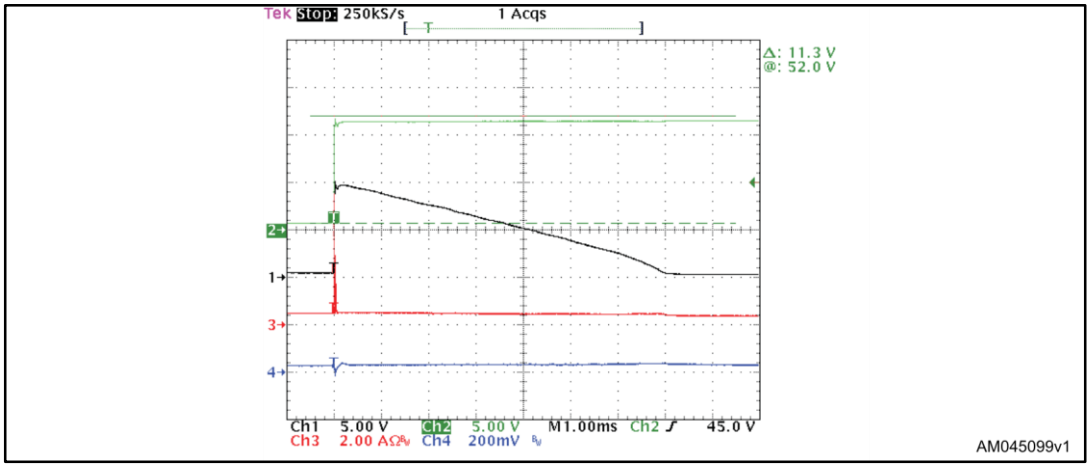
4.5 Inrush and DC current limiting

Once the detection and classification phases have been successfully completed, the PSE raises the voltage across the Ethernet cable. When the voltage difference between VIN and VSS is greater than the V_{UVLO_R} threshold, the internal hot-swap MOSFET is switched on and the DC-DC input capacitance is charged in a controlled manner.

During the inrush phase, the current is limited to 140 mA.

When the RTN voltage falls below 1.5 V, an internal signal (PGOOD in *Figure 3: "PM8803 internal block diagram"*) is asserted to activate the DC-DC section.

Figure 9: Line transient response



Ch1: RTN - VSS, Ch2: VDD - VSS, Ch3: I input, Ch4: 5 V_{OUT} (with offset)

This feature is active only when working from an input voltage with a "frontal" connection, the hot-swap MOSFET is used; this voltage could be from the PoE interface or from an external auxiliary adapter connected before the internal hot-swap MOSFET.

If the auxiliary source is connected after the hot-swap MOSFET, it is opened and this feature is disabled, allowing the converter to work with a low voltage auxiliary source. The PGOOD comparator includes hysteresis to allow the PM8803 to operate near the current limit point without inadvertently disabling it. The MOSFET voltage must increase to 12 V before PGOOD is deasserted.

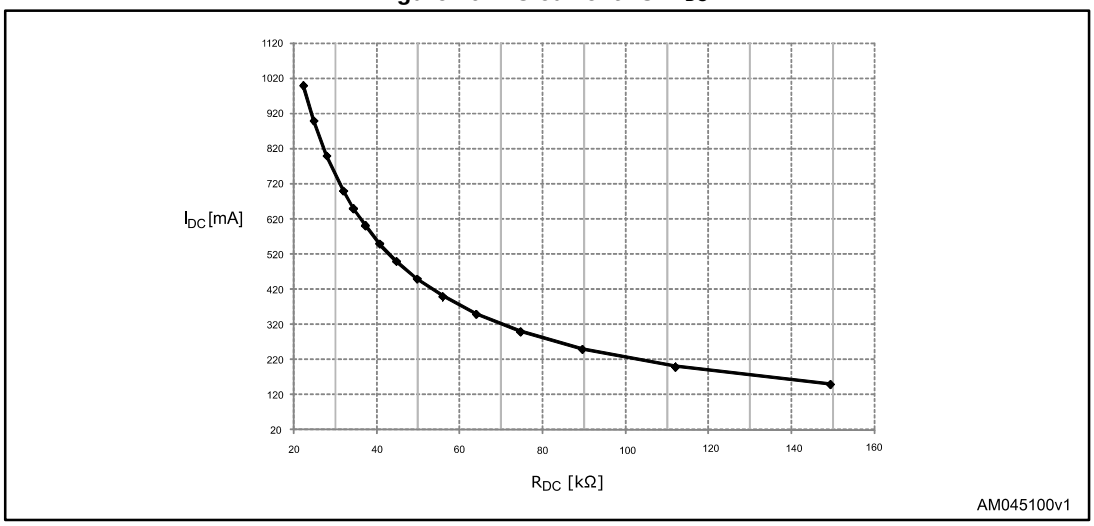
This feature also allows positive line transients up to 12 V to be withstood without stopping DC-DC normal operations as shown in *Figure 9: "Line transient response"*. The line transient is managed by the PWM section, fixing its operating parameters accordingly without shutting down the output voltage. The input current during the transient is controlled by the hot-swap MOSFET at the DC current limit.

After PGOOD assertion, a comparator on the gate of the hot-swap MOSFET controls the transition between the 140 mA to the programmed DC current limit, with a 2 V threshold. The comparator is needed to ensure that the charge of the DC-DC input capacitor is completed, avoiding current spikes on the last portion of the charge.

The PM8803 provides a default continuous current limitation of 640 mA. This is achieved by leaving the pin DCCL floating. A different DC current limit can be set by connecting a resistor R_{DC} between DCCL and VSS whose value can be obtained by the following equation:

$$R_{DC}[k] = \frac{22400}{I_{DC}[mA]}$$

Figure 10: DC current vs. R_{DC}



This limitation is active after the inrush phase is completed. The useful programming range for the current limitation is between 140 mA and 1 A. The practical resistor value range is between 22 kΩ and 150 kΩ.

4.6 High voltage start-up regulator

The PM8803 embeds a high voltage start-up regulator to provide a controlled reference voltage of 8.0 V to the internal current mode PWM controller during its start-up phase.

The regulator output is connected to the VC pin as well as to the DC-DC section

In normal isolated topology, the VC pin is diode-connected to the auxiliary winding of the transformer used for the flyback or forward configuration. When the voltage from the transformer exceeds the regulated voltage, the high voltage regulator is shut off, reducing the amount of power dissipated inside the PM8803.

In detail, when the voltage from the auxiliary winding exceeds 8.0 V, the regulator resets its intervention threshold to 7 V. In this manner, a loosely regulated voltage from the auxiliary winding is allowed without current-sharing with the internal regulator.

In the meantime, if the auxiliary voltage fails, the internal regulator takes over without losing DC-DC control.

The UVLO threshold on VC is 6.0 V typically: at this voltage the DC-DC controller operations are stopped and the outputs frozen in low-state.

While the external auxiliary voltage has to be chosen higher than 8.0 V to take advantage of the auxiliary winding, it must be also lower than 16 V for all operating conditions, to avoid the intervention of the internal protection clamp.

A capacitor in the range of 220 nF-10 uF must be connected to DC-DC ground for stability. For applications with high current drawn from VC, large capacitance should be used (e.g. 10 µF) in order to avoid converter switch-off during the start-up phase.

A VC UVLO mechanism monitors the level of voltage on the VC pin. When VC voltage exceeds the $VC_{UVLO\_R,}$ the PWM controller is enabled and it remains enabled until the VC voltage drops below its VC_{UVLO_F} value.

When an auxiliary winding is not used, the internal HV regulator UVLO threshold is set at 6.6 V and the current limit is set to typ. 20 mA. This value includes the current internally drawn to bias the DC-DC controller, the gate drivers, the VB bias regulator and the external components that may be connected to the VC and VB pins.

Notice that using the HV regulator without the auxiliary winding increases the internal power dissipation, and, at high ambient temperature, may lead the device to thermal shutdown.

4.7 5 V bias regulator

The PM8803 features an accurate 5 V output regulator, which can be used to bias the DC-DC feedback network and the optocoupler connected to the microcontroller.

A capacitor in the range of 100 nF - 2.2 µF must be connected to ARTN for stability.

The regulator current is supplied from the VC pin, to take advantage of the most efficient bias from the auxiliary winding. This means that the current drawn from the VB pin must be taken into account to evaluate the maximum current drawn from the VC pin

The current drawn from the VB pin must be limited to 10 mA maximum.

The VB regulator is also able to accept injected current up to 1 mA without losing voltage regulation.

5 PWM controller

5.1 Oscillator

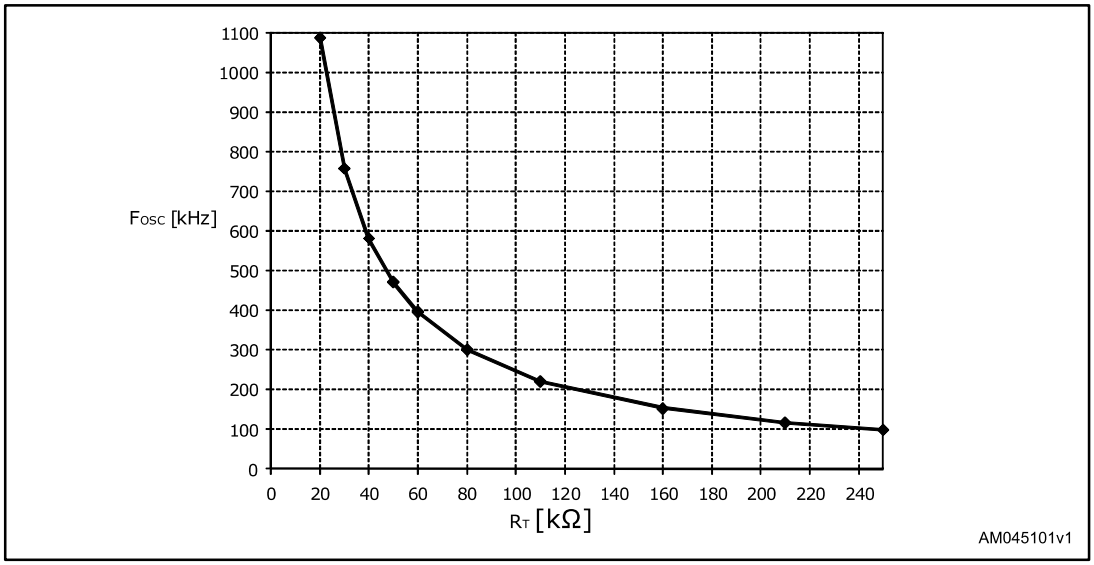
The internal oscillator frequency can be programmed by connecting an external resistor R_T between the FRS and ARTN pins. The relationship between the oscillator frequency F_{OSC} and the R_T resistor is:

$$F_{osc}(kHz) = \frac{25000}{3k\Omega + R_T(k\Omega)}$$

The PWM switching frequency is equal to the programmed oscillator frequency.

The useful range for R_T is between 20 k to 200 kΩ.

Figure 11: PWM frequency vs. R_T



5.2 Delay time control

The delay between the rising edge of GAT2 and GAT1 waveforms can be set by putting a programming resistor R_{DT} between DT and AGND or VB. The relationship between the delay time and the R_{DT} resistor is:

$$t_{del}(ns) = 1.6R_{DT}\ (k\Omega)$$

The same delay time is set between the GAT1 falling edge and the subsequent GAT2 falling edge.

The useful range for R_{DT} is between 5 k to 200 kΩ A resistor should be always connected to this pin.

Figure 12: Delay time vs. R_{DT}

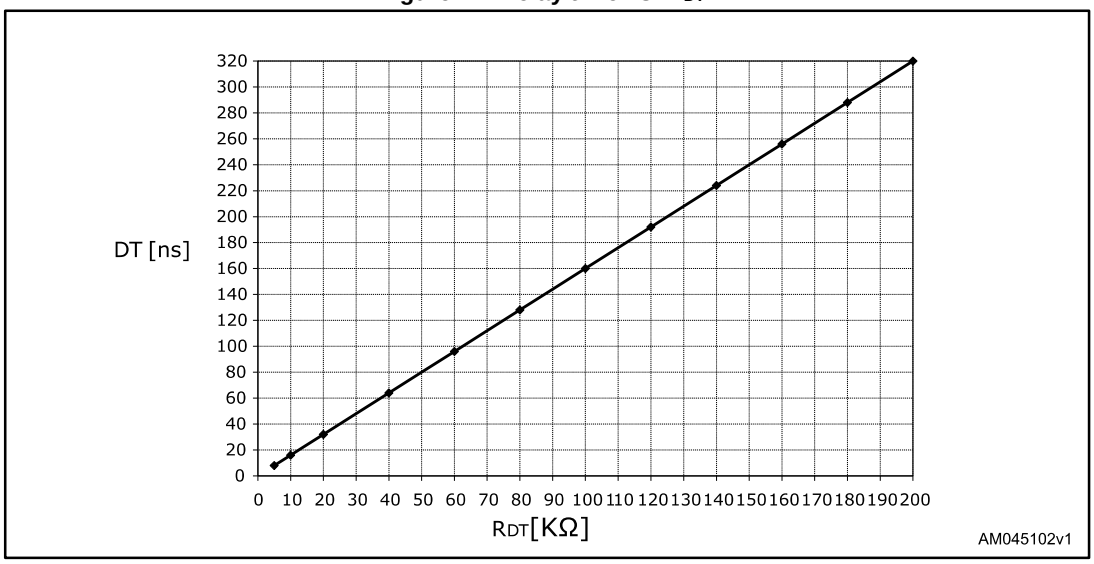
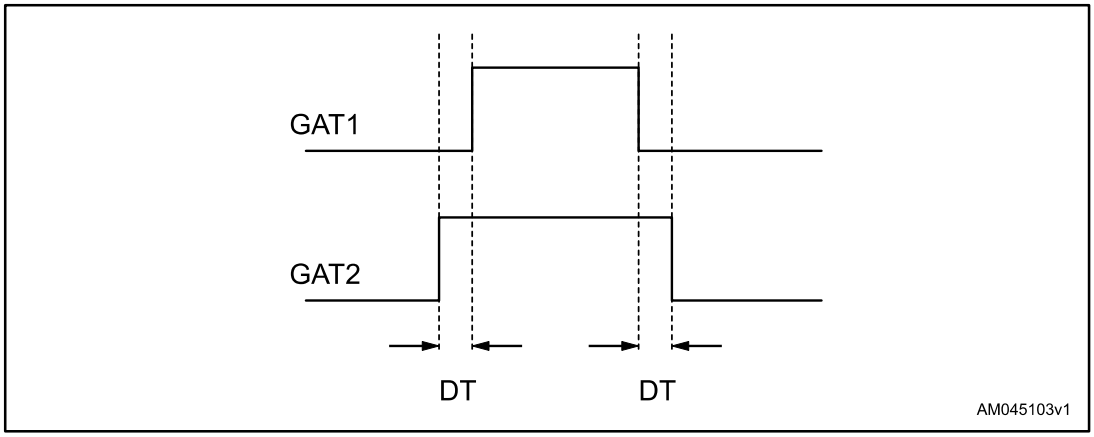


Figure 13: Timing relationship between output drivers as a function of DT



5.3 Soft-start

The DC-DC section of the PM8803 features an internal, digitally controlled, soft-start to make sure that output voltage ramps up in a safe and controlled manner.

At the startup of the converter, the input voltage of the PWM comparator (CTL pin) is clamped to a value which is increased cycle-by-cycle until it reaches the regulation voltage. This results in a converter duty cycle increasing from zero to the operative value in 4096 maximum switching periods.

Taking into account that the output voltage starts increasing only when the CTL pin is higher than 1 V, effective duration of the output voltage soft-start ramp can be estimated as per formula below:

$$T_{SS}[ms] = \frac{4096}{F_{OSC}[kHz]} \cdot \frac{CTL[V] - 1V}{4V}$$

5.4 PWM comparator / slope compensation

In typical isolated operations, current is sensed on a sense resistor R_S placed between the source of the primary side MOS and the RTN pin.

The PWM comparator produces the PWM duty cycle by comparing the R_S ramp signal on CS with an error voltage derived from the error amplifier output.

The error amplifier output voltage on the CTL pin is attenuated by a 4:1 resistor divider before it is presented to the PWM comparator input.

The PWM duty cycle increases according to the voltage at the CTL pin. The controller output duty cycle reduces to zero when the CTL pin voltage drops below approximately 1 V.

For duty cycles higher than 50%, current mode control loops are subjected to sub-harmonic oscillation. The PM8803 fixes the maximum duty cycle at 80% and implements a slope compensation technique consisting of adding a fixed slope voltage ramp to the signal on the CS pin. This is achieved by injecting a 45 µA sawtooth current into the current sense signal path on an integrated 2 kΩ resistor.

A further slope compensation may increase the source impedance of the current sense signal with an external resistor between the CS pin and the source of the current sense signal. The net effect in this case is to increase the slope of the voltage ramp on the PWM comparator terminals.

5.5 Current limit

The current sensed through the CS pin is compared to two fixed levels: 0.5 V and 0.7 V.

The lower level is used to perform a cycle-by-cycle current limit, terminating the PWM pulse. If the overload lasts longer than 4096 switching periods, the PWM is shut down for the same duration before beginning a new soft-start.

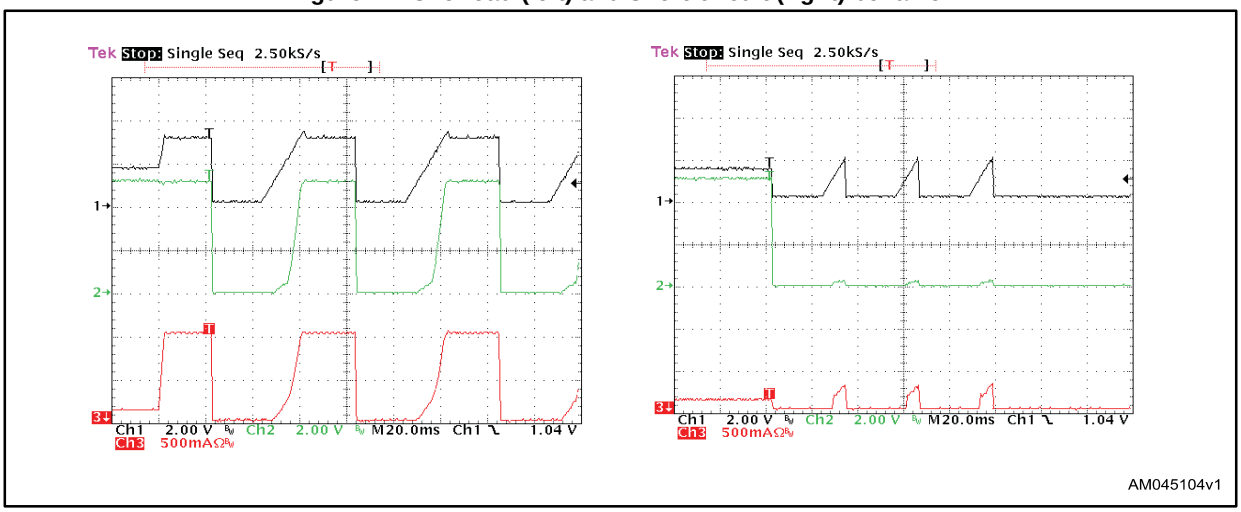
At 250 kHz the allowed overcurrent duration is about 16 ms.

When a severe overcurrent occurs, such as short-circuit of an internal power component, and 0.7 V level is reached on CS, the gate driver shuts down all at once and a new soft-start is performed after 4096 switching periods.

In case of persistent overcurrent, the control logic tries 4 cycles of fast hiccup before shutting down the PWM controller completely.

To restart the device, after removing the cause of the overcurrent, VDD must be reduced below the UVLO level.

Figure 14: Overload (left) and short-circuit (right) behavior



Ch1: CTL signal, Ch2: $5V_{OUT}$, Ch3: I input

5.6 Thermal protection

The PM8803 thermal protection limit is set to 160 °C on the junction temperature and is always active. When this threshold is exceeded, the hot-swap MOSFET is opened and the PWM controller is switched off.

When the junction temperature goes below about 130 °C, the converter starts automatically, without recycling the input voltage.

6 Auxiliary sources

The majority of powered devices is designed to work with power from either a PoE network or auxiliary sources. Even though both sources, simultaneously connected, are not the normal operating case, the presence of an auxiliary supply allows PDs to be used also when the PoE is not available or not sufficient.

Different alternatives are available to connect auxiliary sources to the PoE section of a PD device. Auxiliary sources can be connected before the hot-swap MOSFET, after the hot-swap MOSFET or even on the output of the DC-DC converter.

All the above-mentioned methods are available with the PM8803.

Both *Figure 1: "Simplified application schematic for powered devices using the PM8803 in forward active clamp configuration"* and *Figure 2: "Simplified application schematic for powered devices using the PM8803 in synchronous flyback configuration"* show simplified application schematics where auxiliary sources can be connected either before (front) or after (rear) the internal hot-swap MOSFET (VDD and RTN) using a resistor divider between the external source and respectively SP or SA pins.

The connection of the wall adapter before the internal hot-swap MOSFET has a limitation on the voltage of the adapter itself, since it is considered as an alternative of the PoE line and the embedded DC-DC section is active only when its value is above the UVLO_R threshold. If the voltage on the SP pin is above 1.1 V, the internal UVLO threshold is bypassed and the PM8803 operates with voltage as low as 15 V typical. The current flowing into the hot-swap MOSFET is limited by a dual threshold: typically140 mA during the inrush phase, and a user programmable value (DCCL pin) for the rest of the phases. Priority of one source over another cannot be guaranteed by design, since it depends on timings of insertion and the value of the PoE line with respect to the auxiliary. If, for example, the PoE connection has been already established, the auxiliary source cannot prevail unless its value is higher than that of the PoE after the diode bridge.

Please note that with a low-voltage adapter applied before the hot swap frontal connection, the max. power drawn could be evaluated as (Vin - Vd) x Imax.; in case of a 15 V adapter the input power is limited to about (15 - 0.5) x 1 A = 14.5 W, much lower than the available power from the PoE connection.

High-power systems must use high voltage power adapters, 48 V, and rear connections, to avoid the internal DC current limitation.

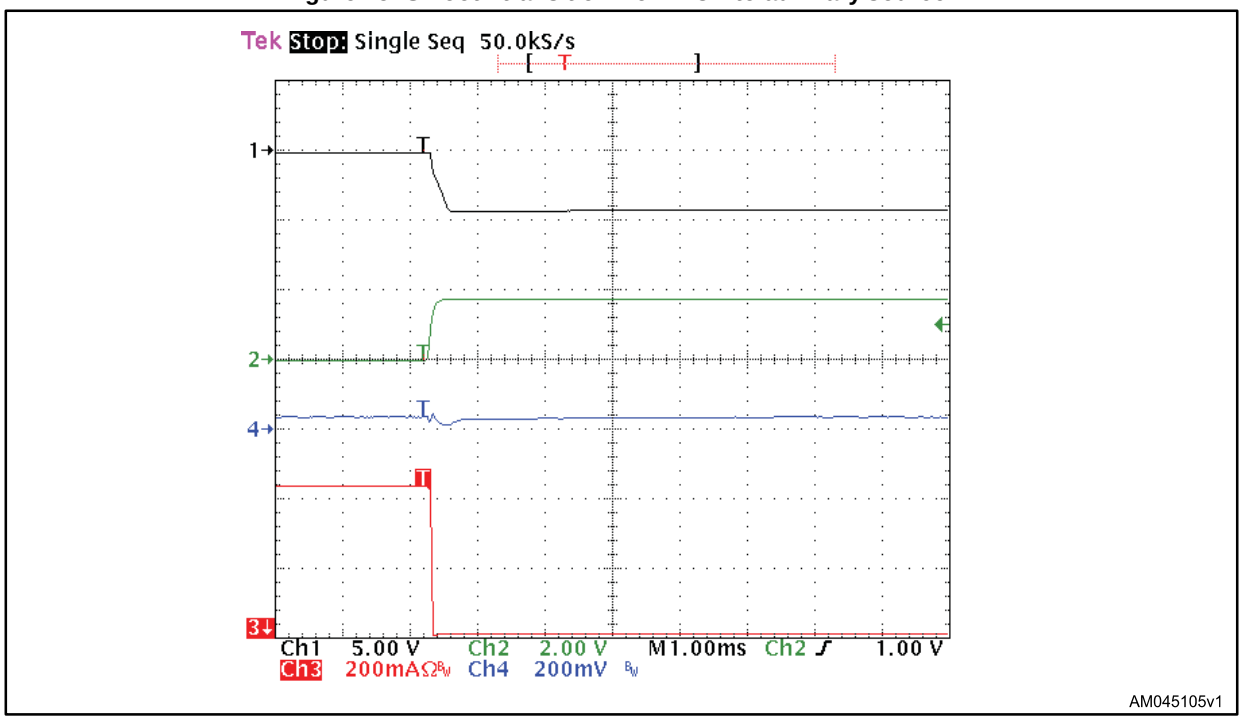
Both *Figure 1: "Simplified application schematic for powered devices using the PM8803 in forward active clamp configuration"* and *Figure 2: "Simplified application schematic for powered devices using the PM8803 in synchronous flyback configuration"* show simplified application schematics where auxiliary sources are also connected after the internal hot-swap MOSFET (VDD and RTN). This connection, together with the resistor divider on the SA pin, allows priority of the external source over the PoE. Indeed, if the voltage of this pin is above the value of 1.20 V, the PM8803 disables its PD interface section and enables the DC-DC section only. The internal hot-swap MOSFET is opened.

Depending on the value of the auxiliary source, the resistor divider must be dimensioned in order to have voltage on the SA and SP pins above their thresholds but still below their maximum operative value of 3.3 V specified in *Table 3: "Absolute maximum ratings"*.

Figure 15: "Smooth transition from POE to auxiliary source" depicts a smooth transition between a PoE and a wall adapter whose voltage is

5 V higher than the PoE voltage.

Figure 15: Smooth transition from POE to auxiliary source



Ch1: VSS-RTN, Ch2: SA, Ch3: I input, Ch4: $5V_{OUT}$

The minimum operative voltage for auxiliary sources is 13 V, thus allowing the use of a 15 V typ. +/-5% power adapter. The internal logic enables operations of the PWM controller only if the input voltage is over the signature threshold (10.8 V typ., 10.3 V -11.3 V range).

Note that inrush current in this case is not limited and an external solution must be found. The simplest solution is to put a low value resistor in series, but this lowers the efficiency of the converter. A more efficient solution is to use a MOSFET as the power switch limits the current during the charging phase, and to add only a few mΩ in series during normal operation.

No DC current limit is foreseen for the rear connection, since the current is not supposed to flow through the hot-swap MOSFET. Cycle-by-cycle, overcurrent protection and thermal protection are instead always active, as well as when the voltage on the SA pin is above 1.20 V.

The T2P signal remains high (deasserted) if a rear auxiliary source is connected.

If the T2P signal is asserted when the auxiliary source is connected, it turns off; its status is stored unless the input voltage drops. So if the PSE remains connected until the auxiliary source is removed, the T2P indication turns on again when the wall adapter is disconnected.

The removal of the external auxiliary source such as a wall adapter usually is followed by a system reboot because the PSE needs some time to re-detect the PD.

If a rear auxiliary connection (using the SA pin) is foreseen in the converter design, it is suggested that 0.1 µF capacitor required by the IEEE802.3at standard is moved from the input (VDD to VSS) to the internal hot-swap MOSFET (VSS to GND) . Alternatively, split the 0.1 µF into two capacitors of 47 nF each: one placed on the input terminal, the second across the hot-swap MOSFET.

7 Layout guidelines

7.1 General guidelines for a PoE converter

The following general guidelines are valid for all the typical converter topologies used for PoE / PoE + converters. Length of the interconnections between following groups of components belonging to the primary side of the converter must be kept as short as possible:

- Input ceramic capacitors
- Input side of the power transformer
- Power MOSFET and sense resistors
- Active clamp circuitry or snubber circuitry (if present)

Length of the interconnections between following groups of components belonging to the secondary side of the isolation must be kept as short as possible:

- Secondary rectifier diode(s), or synchronous rectifier MOSFET(s) and associated driving circuitry
- Output side of the power transformer
- Output ceramic capacitors

Isolation / spacing as required by applicable safety standards must be assured among all the rails / traces / planes at 48 V and between primary and secondary side of the converter.

7.2 How to layout the PM8803 different ground pins

There are 4 different pins of ground on the PM8803: VSS, RTN1, RTN2 and ARTN plus the exposed pad. The exposed pad of the PM8803 must be connected to VSS: design a fill area with at least 6 vias to VSS plane. Try, where possible, to increase the number of VSS power planes connected, at least below the PM8803 position, to improve the heat dissipation of the PM8803. VSS can be routed with a wide trace, but close to the PM8803 must become a copper plane, in order to dissipate the heat transferred through the exposed pad of the PM8803.

RTN1 and RTN2 are power ground pins for GAT1 and GAT2 drivers respectively. Those pins are not internally connected together and therefore must be externally connected with a wide, short connection on the same point of the board power ground, that is called GND. Use a wide power copper plane for such connections; use as fewer traces as possible.

Board GND must be divided into power GND (to connect input caps, R_{SENSE}, the PM8803 pin 4 and 9, SA auxiliary circuitry, isolation cap) and signal GND or ARTN (to connect the other components around the PM8803, the circuitry powered by VC voltage, and the IC pin 8). The signal GND must be connected to power GND to one point only, close to the PM8803 RTN pins 4 and 9.

Use large copper plane for the power GND, foresee a layer dedicated to it completely. ARTN can be a small copper plane or a wide trace connecting the several components referred to it.

To guarantee safe conditions and the correct operation even under extreme operating conditions like ESD surges, it is strongly suggested that 100 V 1 A Schottky diode is introduced with anode to VSS and cathode to RTN. On secondary side, keep the power path of the power secondary GND separated (output side of transformer, secondary rectifier, output capacitors) from feedback network GND, which is connected only to the output capacitor side.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 HTSSOP20 package information

Figure 16: HTSSOP20 package outline

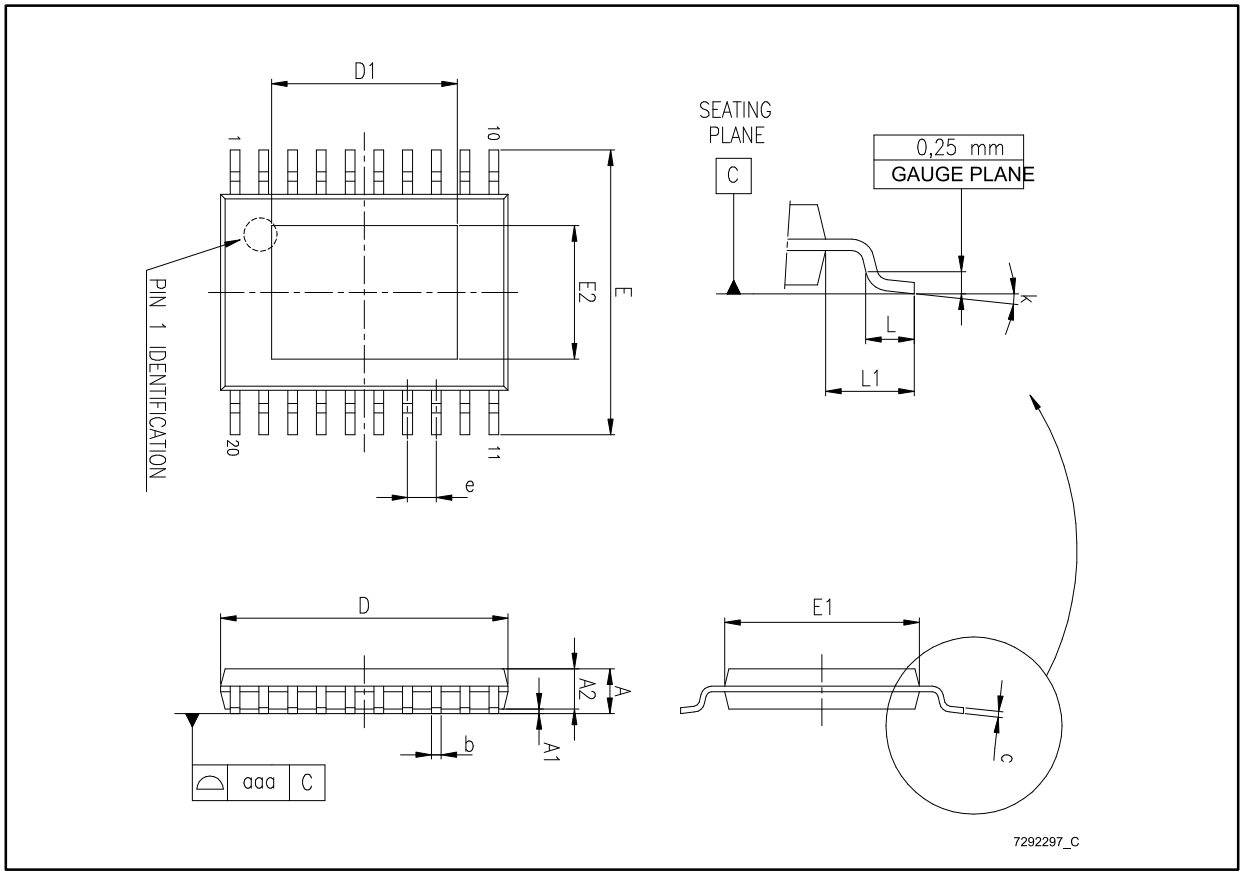


Table 8: HTSSOP20 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
D1	4.1	4.2	4.3	0.161	0.165	0.169
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.0	3.1	0.114	0.118	0.122
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

9 Revision history

Table 9: Document revision history

Date	Revision	Changes
10-Mar-2011	1	Initial release.
07-Nov-2012	2	Document status promoted from preliminary data to production data. Minor text changes.
04-May-2016	3	Added footnote in *Table 3: "Absolute maximum ratings"*. Added *Section 7: "Layout guidelines"*. Minor text changes.

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