

# BATTERY PROTECTION IC FOR 1-CELL PACK

## S-8211D Series

The S-8211D Series are protection ICs for single-cell lithium-ion / lithium-polymer rechargeable batteries and include high-accuracy voltage detectors and delay circuits.

These ICs are suitable for protecting single-cell rechargeable lithium-ion / lithium-polymer battery packs from overcharge, overdischarge, and overcurrent.

### ■ Features

- (1) High-accuracy voltage detection circuit
    - Overcharge detection voltage                      3.9 to 4.4 V (5 mV steps)                      Accuracy  $\pm 25$  mV (+25 °C)  
Accuracy  $\pm 30$  mV (-5 to +55 °C)
    - Overcharge release voltage                      3.8 to 4.4 V<sup>\*1</sup>                      Accuracy  $\pm 50$  mV
    - Overdischarge detection voltage                      2.0 to 3.0 V (10 mV steps)                      Accuracy  $\pm 50$  mV
    - Overdischarge release voltage                      2.0 to 3.4 V<sup>\*2</sup>                      Accuracy  $\pm 100$  mV
    - Discharge overcurrent detection voltage                      0.05 to 0.30 V (10 mV steps)                      Accuracy  $\pm 15$  mV
    - Load short-circuiting detection voltage                      0.5 V (fixed)                      Accuracy  $\pm 200$  mV
  - (2) Detection delay times are generated by an internal circuit (external capacitors are unnecessary).  
Accuracy  $\pm 20\%$
  - (3) High-withstanding-voltage device is used for charger connection pins (VM pin and CO pin : Absolute maximum rating = 28 V)
  - (4) 0 V battery charge function available / unavailable are selectable.
  - (5) Shutdown function yes / no are selectable.
  - (6) Wide operating temperature range                      -40 to +85 °C
  - (7) Low current consumption
    - Operation mode                      3.0  $\mu$ A typ., 5.5  $\mu$ A max. (+25 °C)
    - Power-down mode                      0.2  $\mu$ A max. (+25 °C)
  - (8) Small package:                      SOT-23-5, SNT-6A
  - (9) Lead-free product
- \*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 to 0.4 V in 50 mV steps.)
- \*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 to 0.7 V in 100 mV steps.)

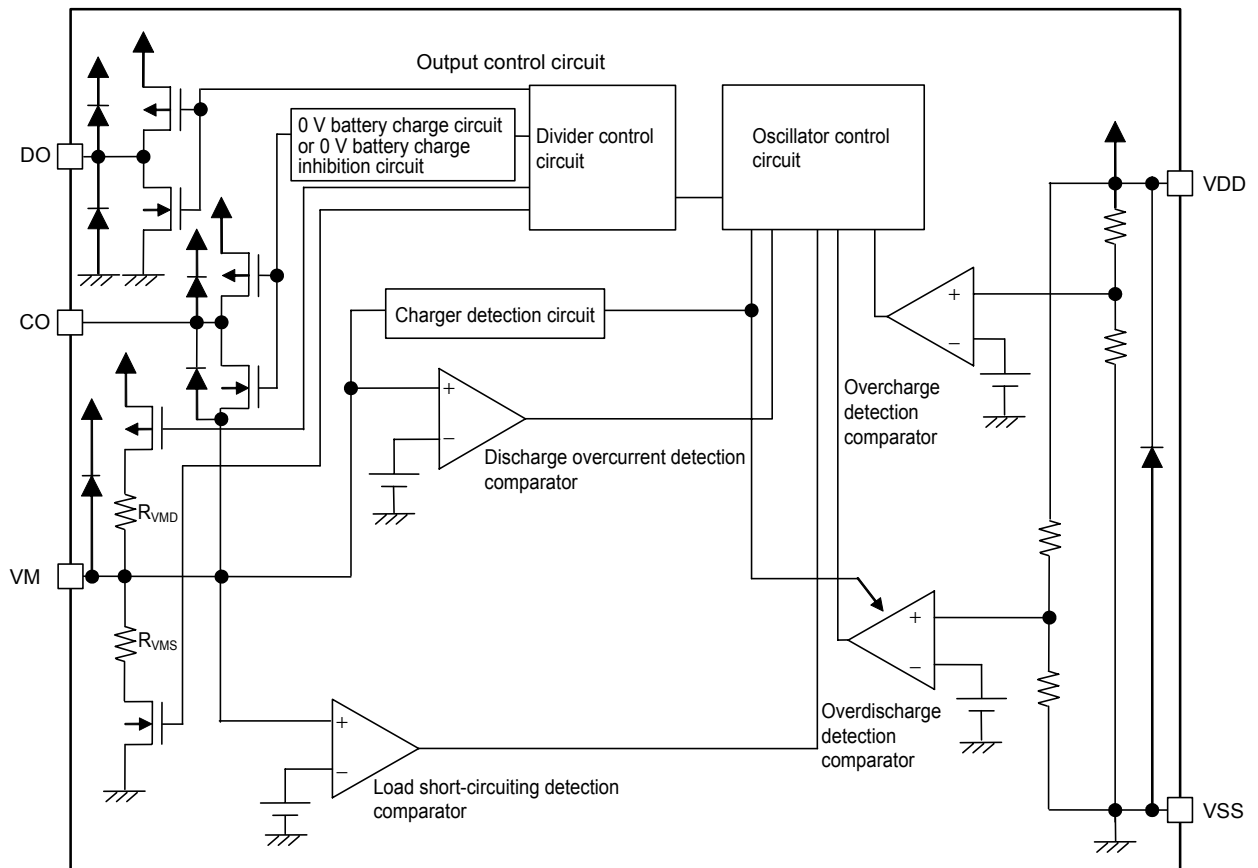
### ■ Applications

- Lithium-ion rechargeable battery packs
- Lithium-polymer rechargeable battery packs

### ■ Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SOT-23-5	MP005-A	MP005-A	MP005-A	-
SNT-6A	PG006-A	PG006-A	PG006-A	PG006-A

■ **Block Diagram**

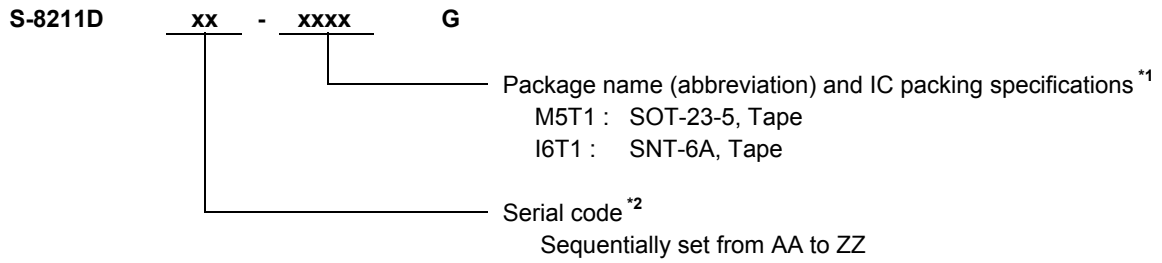


**Remark** All diodes shown in figure are parasitic diodes.

**Figure 1**

■ Product Name Structure

1. Product Name



\*1. Refer to the taping specifications.

\*2. Refer to the "2. Product Name List".

**2 Product Name List**

**(1) SOT-23-5**

**Table 1**

Product Name / Item	Overcharge Detection Voltage $V_{CU}$	Overcharge Release Voltage $V_{CL}$	Over-discharge Detection Voltage $V_{DL}$	Over-discharge Release Voltage $V_{DU}$	Discharge Overcurrent Detection Voltage $V_{DIOV}$	0 V Battery Charge Function	Delay Time Combination <sup>*1</sup>	Shutdown Function
S-8211DAB-M5T1G	4.250 V	4.050 V	2.60 V	2.90 V	0.12 V	Unavailable	(1)	No
S-8211DAE-M5T1G	4.280 V	4.180 V	2.50 V	2.70 V	0.19 V	Unavailable	(1)	Yes
S-8211DAH-M5T1G	4.275 V	4.175 V	2.30 V	2.40 V	0.10 V	Available	(1)	Yes
S-8211DAI-M5T1G	4.325 V	4.075 V	2.50 V	2.90 V	0.15 V	Unavailable	(1)	Yes
S-8211DAJ-M5T1G	4.280 V	4.080 V	3.00 V	3.00 V	0.08 V	Available	(1)	Yes
S-8211DAK-M5T1G	4.280 V	4.080 V	2.30 V	2.30 V	0.13 V	Unavailable	(1)	Yes
S-8211DAL-M5T1G	4.280 V	4.080 V	2.80 V	2.80 V	0.10 V	Available	(1)	Yes
S-8211DAM-M5T1G	4.275 V	4.075 V	2.50 V	2.90 V	0.15 V	Unavailable	(1)	Yes

\*1. Refer to the **Table 3** about the details of the delay time combinations (1).

**Remark** Please contact our sales office for the products with detection voltage value other than those specified above.

**(2) SNT-6A**

**Table 2**

Product Name / Item	Overcharge Detection Voltage $V_{CU}$	Overcharge Release Voltage $V_{CL}$	Over-discharge Detection Voltage $V_{DL}$	Over-discharge Release Voltage $V_{DU}$	Discharge Overcurrent Detection Voltage $V_{DIOV}$	0 V Battery Charge Function	Delay Time Combination <sup>*1</sup>	Shutdown Function
S-8211DAB-I6T1G	4.250 V	4.050 V	2.60 V	2.90 V	0.12 V	Unavailable	(1)	No
S-8211DAE-I6T1G	4.280 V	4.180 V	2.50 V	2.70 V	0.19 V	Unavailable	(1)	Yes
S-8211DAF-I6T1G	4.250 V	4.050 V	2.40 V	2.90 V	0.10 V	Available	(2)	No
S-8211DAG-I6T1G	4.280 V	4.080 V	2.30 V	2.30 V	0.08 V	Available	(1)	No

\*1. Refer to the **Table 3** about the details of the delay time combinations (1) and (2).

**Remark** Please contact our sales office for the products with detection voltage value other than those specified above.

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**Table 3**

Delay Time Combination	Overcharge Detection Delay Time $t_{CU}$	Overdischarge Detection Delay Time $t_{DL}$	Discharge Overcurrent Detection Delay Time $t_{DIOV}$	Load Short-circuiting Detection Delay Time $t_{SHORT}$
(1)	1.2 s	150 ms	9 ms	300 $\mu$ s
(2)	1.2 s	75 ms	9 ms	300 $\mu$ s

**Remark** The delay times can be changed within the range listed **Table 4**. For details, please contact our sales office.

**Table 4**

Delay Time	Symbol	Selection Range			Remark
Overcharge detection delay time	$t_{CU}$	143 ms	<b>573 ms</b>	1.2 s	Select a value from the left.
Overdischarge detection delay time	$t_{DL}$	38 ms	<b>150 ms</b>	300 ms	Select a value from the left.
Discharge overcurrent detection delay time	$t_{DIOV}$	4.5 ms	<b>9 ms</b>	18 ms	Select a value from the left.
Load short-circuiting detection delay time	$t_{SHORT}$	–	<b>300 <math>\mu</math>s</b>	560 $\mu$ s	Select a value from the left.

**Remark** The value surrounded by bold lines is the delay time of the standard products.

■ Pin Configurations

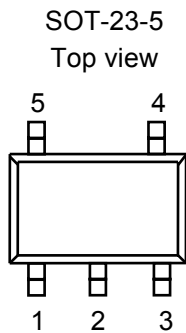


Figure 2

**Table 5**

Pin No.	Symbol	Description
1	VM	Voltage detection between VM pin and VSS pin (Overcurrent / charger detection pin)
2	VDD	Connection for positive power supply input
3	VSS	Connection for negative power supply input
4	DO	Connection of discharge control FET gate (CMOS output)
5	CO	Connection of charge control FET gate (CMOS output)

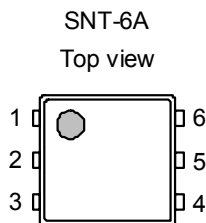


Figure 3

**Table 6**

Pin No.	Symbol	Description
1	NC*1	No connection
2	CO	Connection of charge control FET gate (CMOS output)
3	DO	Connection of discharge control FET gate (CMOS output)
4	VSS	Connection for negative power supply input
5	VDD	Connection for positive power supply input
6	VM	Voltage detection between VM pin and VSS pin (Overcurrent / charger detection pin)

\*1. The NC pin is electrically open.  
 The NC pin can be connected to VDD or VSS.

### ■ Absolute Maximum Ratings

Table 7

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Applied pin	Absolute Maximum Ratings	Unit
Input voltage between VDD pin and VSS pin	V <sub>DS</sub>	VDD	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 12	V
VM pin input voltage	V <sub>VM</sub>	VM	V <sub>DD</sub> - 28 to V <sub>DD</sub> + 0.3	V
DO pin output voltage	V <sub>DO</sub>	DO	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
CO pin output voltage	V <sub>CO</sub>	CO	V <sub>VM</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	–	250 (When not mounted on board)	mW
		SOT-23-5	600 <sup>*1</sup>	mW
		SNT-6A	400 <sup>*1</sup>	mW
Operating ambient temperature	T <sub>opr</sub>	–	- 40 to + 85	°C
Storage temperature	T <sub>stg</sub>	–	- 55 to + 125	°C

\*1. When mounted on board

[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × 1.6 mm
- (2) Board name: JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

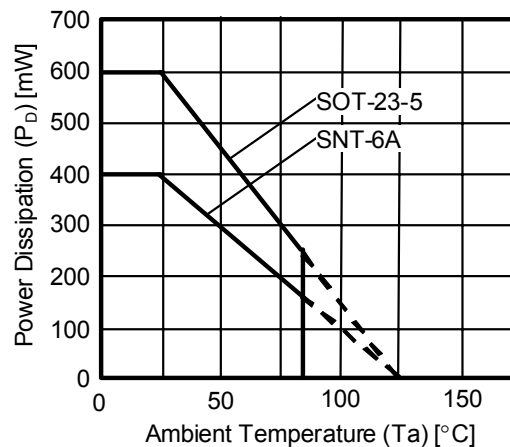


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ **Electrical Characteristics**

**1. Except Detection Delay Time (25 °C)**

**Table 8**

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit	
<b>DETECTION VOLTAGE</b>									
Overcharge detection voltage	V <sub>CU</sub>	3.90 to 4.40 V, Adjustable	V <sub>CU</sub> -0.025	V <sub>CU</sub>	V <sub>CU</sub> +0.025	V	1	1	
		3.90 to 4.40 V, Adjustable, Ta = -5 to +55 °C*1	V <sub>CU</sub> -0.03	V <sub>CU</sub>	V <sub>CU</sub> +0.03	V	1	1	
Overcharge release voltage	V <sub>CL</sub>	3.80 to 4.40 V, Adjustable	V <sub>CL</sub> ≠ V <sub>CU</sub>	V <sub>CL</sub> -0.05	V <sub>CL</sub>	V <sub>CL</sub> +0.05	V	1	1
			V <sub>CL</sub> = V <sub>CU</sub>	V <sub>CL</sub> -0.05	V <sub>CL</sub>	V <sub>CL</sub> +0.025	V	1	1
Overdischarge detection voltage	V <sub>DL</sub>	2.00 to 3.00 V, Adjustable	V <sub>DL</sub> -0.05	V <sub>DL</sub>	V <sub>DL</sub> +0.05	V	2	2	
Overdischarge release voltage	V <sub>DU</sub>	2.00 to 3.40 V, Adjustable	V <sub>DU</sub> ≠ V <sub>DL</sub>	V <sub>DU</sub> -0.10	V <sub>DU</sub>	V <sub>DU</sub> +0.10	V	2	2
			V <sub>DU</sub> = V <sub>DL</sub>	V <sub>DU</sub> -0.05	V <sub>DU</sub>	V <sub>DU</sub> +0.05	V	2	2
Discharge overcurrent detection voltage	V <sub>DIOV</sub>	0.05 to 0.30 V, Adjustable	V <sub>DIOV</sub> -0.015	V <sub>DIOV</sub>	V <sub>DIOV</sub> +0.015	V	3	2	
Load short-circuiting detection voltage*2	V <sub>SHORT</sub>	–	0.30	0.50	0.70	V	3	2	
Charger detection voltage	V <sub>CHA</sub>	–	-1.0	-0.7	-0.4	V	4	2	
<b>0 V BATTERY CHARGE FUNCTION</b>									
0 V battery charge starting charger voltage	V <sub>OCHA</sub>	0 V battery charging function "available"	1.2	–	–	V	10	2	
0 V battery charge inhibition battery voltage	V <sub>OINH</sub>	0 V battery charging function "unavailable"	–	–	0.5	V	11	2	
<b>INTERNAL RESISTANCE</b>									
Resistance between VM pin and VDD pin	R <sub>VMD</sub>	V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V	100	300	900	kΩ	5	3	
Resistance between VM pin and VSS pin	R <sub>VMS</sub>	V <sub>DD</sub> = 3.5 V, V <sub>VM</sub> = 1.0 V	10	20	40	kΩ	5	3	
<b>[INPUT VOLTAGE]</b>									
Operating voltage between VDD pin and VSS pin	V <sub>DSOP1</sub>	–	1.5	–	8	V	–	–	
Operating voltage between VDD pin and VM pin	V <sub>DSOP2</sub>	–	1.5	–	28	V	–	–	
<b>INPUT CURRENT (Shutdown Function Yes)</b>									
Current consumption during operation	I <sub>OPE</sub>	V <sub>DD</sub> = 3.5 V, V <sub>VM</sub> = 0 V	1.0	3.0	5.5	μA	4	2	
Current consumption at power-down	I <sub>PDN</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	–	–	0.2	μA	4	2	
<b>INPUT CURRENT (Shutdown Function No)</b>									
Current consumption during operation	I <sub>OPE</sub>	V <sub>DD</sub> = 3.5 V, V <sub>VM</sub> = 0 V	1.0	3.0	5.5	μA	4	2	
Current consumption during overdischarge	I <sub>OPED</sub>	V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V	0.3	2.0	3.5	μA	4	2	
<b>OUTPUT RESISTANCE</b>									
CO pin resistance "H"	R <sub>COH</sub>	V <sub>CO</sub> = 3.0 V, V <sub>DD</sub> = 3.5 V, V <sub>VM</sub> = 0 V	2.5	5	10	kΩ	6	4	
CO pin resistance "L"	R <sub>COL</sub>	V <sub>CO</sub> = 0.5 V, V <sub>DD</sub> = 4.5 V, V <sub>VM</sub> = 0 V	2.5	5	10	kΩ	6	4	
DO pin resistance "H"	R <sub>DOH</sub>	V <sub>DO</sub> = 3.0 V, V <sub>DD</sub> = 3.5 V, V <sub>VM</sub> = 0 V	2.5	5	10	kΩ	7	4	
DO pin resistance "L"	R <sub>DOL</sub>	V <sub>DO</sub> = 0.5 V, V <sub>DD</sub> = V <sub>VM</sub> = 1.8 V	2.5	5	10	kΩ	7	4	

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

\*2. In any conditions, Load short-circuiting detection voltage (V<sub>SHORT</sub>) is higher Discharge overcurrent detection voltage (V<sub>DIOV</sub>).



# BATTERY PROTECTION IC FOR 1-CELL PACK S-8211D Series

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## 2. Except Detection Delay Time (−40 to +85°C \*1)

Table 9

(−40 to +85°C \*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>DETECTION VOLTAGE</b>								
Overcharge detection voltage	$V_{CU}$	3.90 to 4.40 V, Adjustable	$V_{CU}$ − 0.060	$V_{CU}$	$V_{CU}$ + 0.040	V	1	1
Overcharge release voltage	$V_{CL}$	3.80 to 4.40 V, Adjustable	$V_{CL} \neq V_{CU}$	$V_{CL}$ − 0.08	$V_{CL}$ + 0.065	V	1	1
			$V_{CL} = V_{CU}$	$V_{CL}$ − 0.08	$V_{CL}$ + 0.04	V	1	1
Overdischarge detection voltage	$V_{DL}$	2.00 to 3.00 V, Adjustable	$V_{DL}$ − 0.11	$V_{DL}$	$V_{DL}$ + 0.13	V	2	2
Overdischarge release voltage	$V_{DU}$	2.00 to 3.40 V, Adjustable	$V_{DU} \neq V_{DL}$	$V_{DU}$ − 0.15	$V_{DU}$ + 0.19	V	2	2
			$V_{DU} = V_{DL}$	$V_{DU}$ − 0.11	$V_{DU}$ + 0.13	V	2	2
Discharge overcurrent detection voltage	$V_{DIOV}$	0.05 to 0.30 V, Adjustable	$V_{DIOV}$ − 0.021	$V_{DIOV}$	$V_{DIOV}$ + 0.024	V	3	2
Load short-circuiting detection voltage*2	$V_{SHORT}$	−	0.16	0.50	0.84	V	3	2
Charger detection voltage	$V_{CHA}$	−	−1.2	−0.7	−0.2	V	4	2
<b>0 V BATTERY CHARGE FUNCTION</b>								
0 V battery charge starting charger voltage	$V_{OCHA}$	0 V battery charging function "available"	1.7	−	−	V	10	2
0 V battery charge inhibition battery voltage	$V_{OINH}$	0 V battery charging function "unavailable"	−	−	0.3	V	11	2
<b>INTERNAL RESISTANCE</b>								
Resistance between VM pin and VDD pin	$R_{VMD}$	$V_{DD} = 1.8 \text{ V}, V_{VM} = 0 \text{ V}$	78	300	1310	k $\Omega$	5	3
Resistance between VM pin and VSS pin	$R_{VMS}$	$V_{DD} = 3.5 \text{ V}, V_{VM} = 1.0 \text{ V}$	7.2	20	44	k $\Omega$	5	3
<b>INPUT VOLTAGE</b>								
Operating voltage between VDD pin and VSS pin	$V_{DSOP1}$	−	1.5	−	8	V	−	−
Operating voltage between VDD pin and VM pin	$V_{DSOP2}$	−	1.5	−	28	V	−	−
<b>INPUT CURRENT (Shutdown Function Yes)</b>								
Current consumption during operation	$I_{OPE}$	$V_{DD} = 3.5 \text{ V}, V_{VM} = 0 \text{ V}$	0.7	3.0	6.0	$\mu\text{A}$	4	2
Current consumption at power-down	$I_{PDN}$	$V_{DD} = V_{VM} = 1.5 \text{ V}$	−	−	0.3	$\mu\text{A}$	4	2
<b>INPUT CURRENT (Shutdown Function No)</b>								
Current consumption during operation	$I_{OPE}$	$V_{DD} = 3.5 \text{ V}, V_{VM} = 0 \text{ V}$	0.7	3.0	6.0	$\mu\text{A}$	4	2
Current consumption during overdischarge	$I_{OPED}$	$V_{DD} = V_{VM} = 1.5 \text{ V}$	0.2	2.0	3.8	$\mu\text{A}$	4	2
<b>OUTPUT RESISTANCE</b>								
CO pin resistance "H"	$R_{COH}$	$V_{CO} = 3.0 \text{ V}, V_{DD} = 3.5 \text{ V}, V_{VM} = 0 \text{ V}$	1.2	5	15	k $\Omega$	6	4
CO pin resistance "L"	$R_{COL}$	$V_{CO} = 0.5 \text{ V}, V_{DD} = 4.5 \text{ V}, V_{VM} = 0 \text{ V}$	1.2	5	15	k $\Omega$	6	4
DO pin resistance "H"	$R_{DOH}$	$V_{DO} = 3.0 \text{ V}, V_{DD} = 3.5 \text{ V}, V_{VM} = 0 \text{ V}$	1.2	5	15	k $\Omega$	7	4
DO pin resistance "L"	$R_{DOL}$	$V_{DO} = 0.5 \text{ V}, V_{DD} = V_{VM} = 1.8 \text{ V}$	1.2	5	15	k $\Omega$	7	4

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

\*2. In any conditions, Load short-circuiting detection voltage ( $V_{SHORT}$ ) is higher Discharge overcurrent detection voltage ( $V_{DIOV}$ ).

**3. Detection Delay Time**

(1) S-8211DAB, S-8211DAE, S-8211DAG, S-8211DAH, S-8211DAI, S-8211DAJ, S-8211DAK, S-8211DAL, S-8211DAM

**Table 10**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>DELAY TIME (Ta = 25°C)</b>								
Overcharge detection delay time	t <sub>CU</sub>	–	0.96	1.2	1.4	s	8	5
Overdischarge detection delay time	t <sub>DL</sub>	–	120	150	180	ms	8	5
Discharge overcurrent detection delay time	t <sub>DIOV</sub>	–	7.2	9	11	ms	9	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	–	240	300	360	μs	9	5
<b>DELAY TIME (Ta = -40 to +85°C) *1</b>								
Overcharge detection delay time	t <sub>CU</sub>	–	0.7	1.2	2.0	s	8	5
Overdischarge detection delay time	t <sub>DL</sub>	–	83	150	255	ms	8	5
Discharge overcurrent detection delay time	t <sub>DIOV</sub>	–	5	9	15	ms	9	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	–	150	300	540	μs	9	5

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

(2) S-8211DAF

**Table 11**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>DELAY TIME (Ta = 25°C)</b>								
Overcharge detection delay time	t <sub>CU</sub>	–	0.96	1.2	1.4	s	8	5
Overdischarge detection delay time	t <sub>DL</sub>	–	61	75	90	ms	8	5
Discharge overcurrent detection delay time	t <sub>DIOV</sub>	–	7.2	9	11	ms	9	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	–	240	300	360	μs	9	5
<b>DELAY TIME (Ta = -40 to +85°C) *1</b>								
Overcharge detection delay time	t <sub>CU</sub>	–	0.7	1.2	2.0	s	8	5
Overdischarge detection delay time	t <sub>DL</sub>	–	41	75	128	ms	8	5
Discharge overcurrent detection delay time	t <sub>DIOV</sub>	–	5	9	15	ms	9	5
Load short-circuiting detection delay time	t <sub>SHORT</sub>	–	150	300	540	μs	9	5

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

## ■ Test Circuits

**Caution** Unless otherwise specified, the output voltage levels “H” and “L” at CO pin ( $V_{CO}$ ) and DO pin ( $V_{DO}$ ) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to  $V_{VM}$  and the DO pin level with respect to  $V_{SS}$ .

### (1) Overcharge Detection Voltage, Overcharge Release Voltage (Test Condition 1, Test Circuit 1)

Overcharge detection voltage ( $V_{CU}$ ) is defined as the voltage between the VDD pin and VSS pin at which  $V_{CO}$  goes from “H” to “L” when the voltage  $V_1$  is gradually increased from the starting condition of  $V_1 = 3.5$  V. Overcharge release voltage ( $V_{CL}$ ) is defined as the voltage between the VDD pin and VSS pin at which  $V_{CO}$  goes from “L” to “H” when the voltage  $V_1$  is then gradually decreased. Overcharge hysteresis voltage ( $V_{HC}$ ) is defined as the difference between overcharge detection voltage ( $V_{CU}$ ) and overcharge release voltage ( $V_{CL}$ ).

### (2) Overdischarge Detection Voltage, Overdischarge Release Voltage (Test Condition 2, Test Circuit 2)

Overdischarge detection voltage ( $V_{DL}$ ) is defined as the voltage between the VDD pin and VSS pin at which  $V_{DO}$  goes from “H” to “L” when the voltage  $V_1$  is gradually decreased from the starting condition of  $V_1 = 3.5$  V,  $V_2 = 0$  V. Overdischarge release voltage ( $V_{DU}$ ) is defined as the voltage between the VDD pin and VSS pin at which  $V_{DO}$  goes from “L” to “H” when the voltage  $V_1$  is then gradually increased. Overdischarge hysteresis voltage ( $V_{HD}$ ) is defined as the difference between overdischarge release voltage ( $V_{DU}$ ) and overdischarge detection voltage ( $V_{DL}$ ).

### (3) Discharge Overcurrent Detection Voltage (Test Condition 3, Test Circuit 2)

Discharge overcurrent detection voltage ( $V_{DIOV}$ ) is defined as the voltage between the VM pin and VSS pin whose delay time for changing  $V_{DO}$  from “H” to “L” lies between the minimum and the maximum value of discharge overcurrent delay time when the voltage  $V_2$  is increased rapidly (within 10  $\mu$ s) from the starting condition of  $V_1 = 3.5$  V,  $V_2 = 0$  V.

### (4) Load Short-circuiting Detection Voltage (Test Condition 3, Test Circuit 2)

Load short-circuiting detection voltage ( $V_{SHORT}$ ) is defined as the voltage between the VM pin and VSS pin whose delay time for changing  $V_{DO}$  from “H” to “L” lies between the minimum and the maximum value of load short-circuiting delay time when the voltage  $V_2$  is increased rapidly (within 10  $\mu$ s) from the starting condition of  $V_1 = 3.5$  V,  $V_2 = 0$  V.

### (5) Operating Current Consumption (Test Condition 4, Test Circuit 2)

The operating current consumption ( $I_{OPE}$ ) is the current that flows through the VDD pin ( $I_{DD}$ ) under the set conditions of  $V_1 = 3.5$  V and  $V_2 = 0$  V (normal status).

### (6) Charger detection voltage (= the detection voltage for irregular charging current) (Test Condition 4, Test Circuit 2)

The charger detection voltage ( $V_{CHA}$ ) is the voltage between the VM and VSS pin; when gradually increasing  $V_1$  at  $V_1 = 1.8$  V,  $V_2 = 0$  V to set  $V_1 = V_{DL} + (V_{HD}/2)$ , after that, decreasing  $V_2$  gradually from 0 V so that  $V_{DO}$  goes “L” to “H”. Measurement of the charger detection voltage is available for the product with overdischarge hysteresis  $V_{HD} \neq 0$  only. The detection voltage for irregular charging current is the voltage between the VM and VSS pin; when gradually decreasing  $V_2$  at  $V_1 = 3.5$  V,  $V_2 = 0$  V and  $V_{CO}$  goes “H” to “L”.

The value of the detection voltage for irregular charging current is equal to the charger detection voltage ( $V_{CHA}$ ).

**(7) Power-down Current Consumption, Overdischarge Current Consumption**  
**(Test Condition 4, Test Circuit 2)**

**Shutdown function yes product**

The power-down current consumption ( $I_{PDN}$ ) is the current that flows through the VDD pin ( $I_{DD}$ ) under the set conditions of  $V1 = V2 = 1.5$  V (overdischarge status).

**Shutdown function no product**

The overdischarge current consumption ( $I_{OPED}$ ) is the current that flows through the VDD pin ( $I_{DD}$ ) under the set conditions of  $V1 = V2 = 1.5$  V (overdischarge status).

**(8) Resistance between VM Pin and VDD Pin**  
**(Test Condition 5, Test Circuit 3)**

The resistance between VM pin and VDD pin ( $R_{VMD}$ ) is the resistance between VM pin and VDD pin under the set conditions of  $V1 = 1.8$  V,  $V2 = 0$  V.

**(9) Resistance between VM Pin and VSS Pin**  
**(Test Condition 5, Test Circuit 3)**

The resistance between VM pin and VSS pin ( $R_{VMS}$ ) is the resistance between VM pin and VSS pin under the set conditions of  $V1 = 3.5$  V,  $V2 = 1.0$  V.

**(10) CO Pin Resistance "H"**  
**(Test Condition 6, Test Circuit 4)**

The CO pin resistance "H" ( $R_{COH}$ ) is the resistance at the CO pin under the set conditions of  $V1 = 3.5$  V,  $V2 = 0$  V,  $V3 = 3.0$  V.

**(11) CO Pin Resistance "L"**  
**(Test Condition 6, Test Circuit 4)**

The CO pin resistance "L" ( $R_{COL}$ ) is the resistance at the CO pin under the set conditions of  $V1 = 4.5$  V,  $V2 = 0$  V,  $V3 = 0.5$  V.

**(12) DO Pin Resistance "H"**  
**(Test Condition 7, Test Circuit 4)**

The DO pin H resistance ( $R_{DOH}$ ) is the resistance at the DO pin under the set conditions of  $V1 = 3.5$  V,  $V2 = 0$  V,  $V4 = 3.0$  V.

**(13) DO Pin Resistance "L"**  
**(Test Condition 7, Test Circuit 4)**

The DO pin L resistance ( $R_{DOL}$ ) is the resistance at the DO pin under the set conditions of  $V1 = 1.8$  V,  $V2 = 0$  V,  $V4 = 0.5$  V.

**(14) Overcharge Detection Delay Time**  
**(Test Condition 8, Test Circuit 5)**

The overcharge detection delay time ( $t_{CU}$ ) is the time needed for  $V_{CO}$  to change from "H" to "L" just after the voltage  $V1$  momentarily increases (within 10  $\mu$ s) from overcharge detection voltage ( $V_{CU}$ )  $-0.2$  V to overcharge detection voltage ( $V_{CU}$ )  $+0.2$  V under the set conditions of  $V2 = 0$  V.

**(15) Overdischarge Detection Delay Time**  
**(Test Condition 8, Test Circuit 5)**

The overdischarge detection delay time ( $t_{DL}$ ) is the time needed for  $V_{DO}$  to change from "H" to "L" just after the voltage  $V1$  momentarily decreases (within 10  $\mu$ s) from overcharge detection voltage ( $V_{DL}$ )  $+0.2$  V to overcharge detection voltage ( $V_{DL}$ )  $-0.2$  V under the set condition of  $V2 = 0$  V.

**(16) Discharge Overcurrent Detection Delay Time**  
**(Test Condition 9, Test Circuit 5)**

Discharge overcurrent detection delay time ( $t_{DIOV}$ ) is the time needed for  $V_{DO}$  to go to “L” after the voltage  $V_2$  momentarily increases (within 10  $\mu$ s) from 0 V to 0.35 V under the set conditions of  $V_1 = 3.5$  V,  $V_2 = 0$  V.

**(17) Load Short-circuiting Detection Delay Time**  
**(Test Condition 9, Test Circuit 5)**

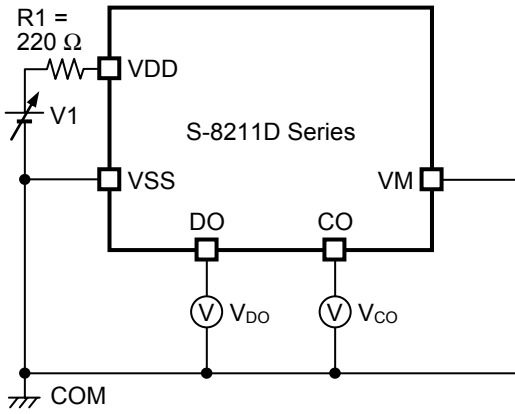
Load short-circuiting detection delay time ( $t_{SHORT}$ ) is the time needed for  $V_{DO}$  to go to “L” after the voltage  $V_2$  momentarily increases (within 10  $\mu$ s) from 0 V to 1.6 V under the set conditions of  $V_1 = 3.5$  V,  $V_2 = 0$  V.

**(18) 0 V Battery Charge Starting Charger Voltage (Products with 0 V Battery Charging Function Is “Available”)**  
**(Test Condition 10, Test Circuit 2)**

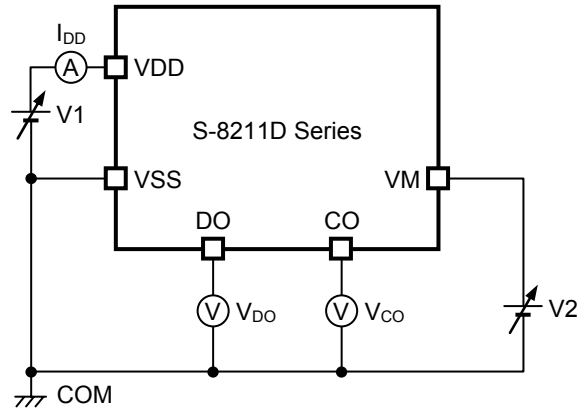
The 0 V charge starting charger voltage ( $V_{0CHA}$ ) is defined as the voltage between the VDD pin and VM pin at which  $V_{CO}$  goes to “H” ( $V_{VM} + 0.1$  V or higher) when the voltage  $V_2$  is gradually decreased from the starting condition of  $V_1 = V_2 = 0$  V.

**(19) 0 V Battery Charge Inhibition Battery Voltage (Products with 0 V Battery Charging Function Is “Unavailable”)**  
**(Test Condition 11, Test Circuit 2)**

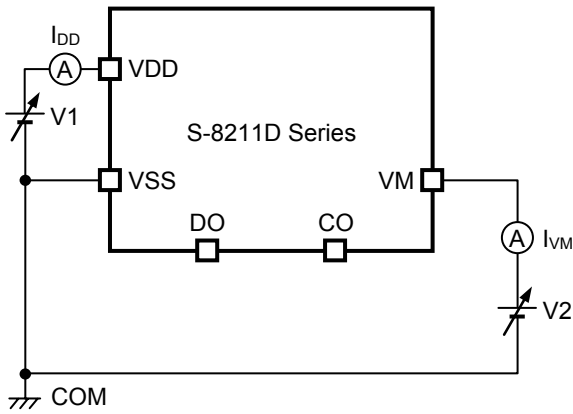
The 0 V charge inhibition charger voltage ( $V_{0INH}$ ) is defined as the voltage between the VDD pin and VSS pin at which  $V_{CO}$  goes to “H” ( $V_{VM} + 0.1$  V or higher) when the voltage  $V_1$  is gradually increased from the starting condition of  $V_1 = 0$  V,  $V_2 = -4$  V.



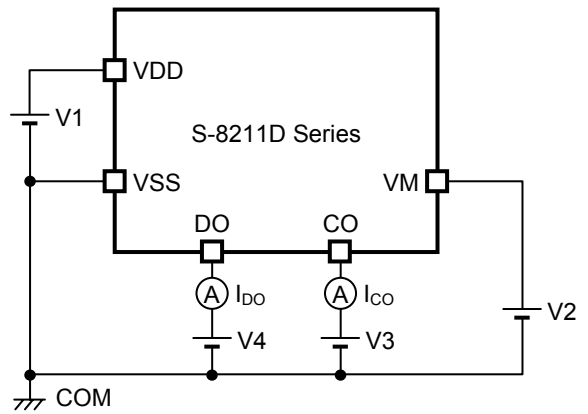
**Figure 5 Test Circuit 1**



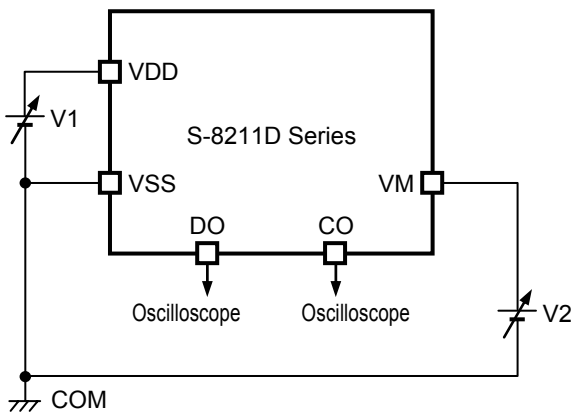
**Figure 6 Test Circuit 2**



**Figure 7 Test Circuit 3**



**Figure 8 Test Circuit 4**



**Figure 9 Test Circuit 5**

## ■ Operation

**Remark** Refer to the “**Battery Protection IC Connection Example**”.

### 1. Normal Status

This IC monitors the voltage of the battery connected between the VDD pin and VSS pin and the voltage difference between the VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage ( $V_{DL}$ ) to overcharge detection voltage ( $V_{CU}$ ), and the VM pin voltage is not more than the discharge overcurrent detection voltage ( $V_{DIOV}$ ), the IC turns both the charging and discharging control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.

The resistance ( $R_{VMD}$ ) between the VM pin and VDD pin, and the resistance ( $R_{VMS}$ ) between the VM pin and VSS pin are not connected in the normal status.

**Caution** When the battery is connected for the first time, discharging may not be enabled. In this case, short the VM pin and VSS pin or connect the charger to restore the normal status.

### 2. Overcharge Status

When the battery voltage becomes higher than overcharge detection voltage ( $V_{CU}$ ) during charging in the normal status and detection continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the S-8211D Series turns the charging control FET off to stop charging. This condition is called the overcharge status.

The resistance ( $R_{VMD}$ ) between the VM pin and VDD pin, and the resistance ( $R_{VMS}$ ) between the VM pin and VSS pin are not connected in the overcharge status.

The overcharge status is released in the following two cases ( (1) and (2) ).

- (1) In the case that the VM pin voltage is higher than or equal to charger detection voltage ( $V_{CHA}$ ), and is lower than the discharge overcurrent detection voltage ( $V_{DIOV}$ ), S-8211D Series releases the overcharge status when the battery voltage falls below the overcharge release voltage ( $V_{CL}$ ).
- (2) In the case that the VM pin voltage is higher than or equal to the discharge overcurrent detection voltage ( $V_{DIOV}$ ), S-8211D Series releases the overcharge status when the battery voltage falls below the overcharge detection voltage ( $V_{CU}$ ).

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises more than the voltage at VSS pin due to the  $V_f$  voltage of the parasitic diode. This is because the discharge current flows through the parasitic diode in the charging control FET. If this VM pin voltage is higher than or equal to the discharge overcurrent detection voltage ( $V_{DIOV}$ ), S-8211D Series releases the overcharge status when the battery voltage is lower than or equal to the overcharge detection voltage ( $V_{CU}$ ).

**Cautions** 1. If the battery is charged to a voltage higher than overcharge detection voltage ( $V_{CU}$ ) and the battery voltage does not fall below overcharge detection voltage ( $V_{CU}$ ) even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below overcharge detection voltage ( $V_{CU}$ ). Since an actual battery has an internal impedance of tens of  $m\Omega$ , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below overcharge release voltage ( $V_{CL}$ ). The overcharge status is released when the VM pin voltage goes over charger detection voltage ( $V_{CHA}$ ) by removing the charger.

### 3. Overdischarge Status

#### With shutdown function

When the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ) during discharging in the normal status and the detection continues for the overdischarge detection delay time ( $t_{DL}$ ) or longer, the S-8211D Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status. Under the overdischarge status, the VM pin voltage is pulled up by the resistor between the VM pin and VDD pin in the IC ( $R_{VMD}$ ). When voltage difference between the VM pin and VDD pin then is 1.3 V (Typ.) or lower, the current consumption is reduced to the power-down current consumption ( $I_{PDN}$ ). This condition is called the power-down status.

The resistance ( $R_{VMS}$ ) between the VM pin and VSS pin is not connected in the power-down status and the overdischarge status.

The power-down status is released when a charger is connected and the voltage difference between the VM pin and VDD pin becomes 1.3 V (typ.) or higher.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than charger detection voltage ( $V_{CHA}$ ), the S-8211D Series releases the overdischarge status and turns the discharging FET on when the battery voltage reaches overdischarge detection voltage ( $V_{DL}$ ) or higher.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than charger detection voltage ( $V_{CHA}$ ), the S-8211D Series releases the overdischarge status when the battery voltage reaches overdischarge release voltage ( $V_{DU}$ ) or higher.

#### Without shutdown function

When the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ) during discharging in the normal status and the detection continues for the overdischarge detection delay time ( $t_{DL}$ ) or longer, the S-8211D Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status. Under the overdischarge status, the VM pin voltage is pulled up by the resistor between the VM pin and VDD pin in the IC ( $R_{VMD}$ ).

The resistance ( $R_{VMS}$ ) between the VM pin and VSS pin is not connected in the overdischarge status.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than charger detection voltage ( $V_{CHA}$ ), the S-8211D Series releases the overdischarge status and turns the discharging FET on when the battery voltage reaches overdischarge detection voltage ( $V_{DL}$ ) or higher.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than charger detection voltage ( $V_{CHA}$ ), the S-8211D Series releases the overdischarge status when the battery voltage reaches overdischarge release voltage ( $V_{DU}$ ) or higher.

### 4. Discharge Overcurrent Status (Discharge Overcurrent, Load Short-circuiting)

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the discharge overcurrent detection voltage because the discharge current is higher than the specified value and the status lasts for the discharge overcurrent detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

In the discharge overcurrent status, the VM pin and VSS pin are shorted by the resistor between VM pin and VSS pin ( $R_{VMS}$ ) in the IC. However, the voltage of the VM pin is at the  $V_{DD}$  potential due to the load as long as the load is connected. When the load is disconnected, the VM pin returns to the  $V_{SS}$  potential.

This IC detects the status when the impedance between the EB+ pin and EB- pin (Refer to the **Figure 13**) increases and is equal to the impedance that enables automatic restoration and the voltage at the VM pin returns to discharge overcurrent detection voltage ( $V_{DIOV}$ ) or lower, the discharge overcurrent status is restored to the normal status.

Even if the connected impedance is smaller than automatic restoration level, the S-8211D Series will be restored to the normal status from discharge overcurrent detection status when the voltage at the VM pin becomes the discharge overcurrent detection voltage ( $V_{DIOV}$ ) or lower by connecting the charger.

The resistance ( $R_{VMD}$ ) between the VM pin and VDD pin is not connected in the discharge overcurrent detection status.



## 5. Detection for irregular charging current

During charging a battery which is in the normal status, if the VM pin voltage becomes lower than the charger detection voltage ( $V_{CHA}$ ) and this status is held longer than the overcharge detection delay time ( $t_{CU}$ ), S-8211D turns off the charge-control FET to stop charging. This is detection for irregular charging current.

This function works in the case that the DO pin voltage is in "H", and the VM pin voltage becomes lower than the charger detection voltage ( $V_{CHA}$ ). Thus if the irregular charger current flows in the battery in the overdischarge status, S-8211D turns off the charge-control FET to stop charging; the DO pin voltage goes in "H" so that the battery voltage becomes higher than the overdischarge detection voltage, and after the overcharge detection delay time ( $t_{CU}$ ).

The status irregular charging current detection is released by the lower potential difference between the VM and VSS pin than the charger detection voltage ( $V_{CHA}$ ).

## 6. 0 V Battery Charging Function "Available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage ( $V_{0CHA}$ ) or a higher voltage is applied between the EB+ and EB- pins by connecting a charger, the charging control FET gate is fixed to the VDD pin voltage.

When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than overdischarge release voltage ( $V_{DU}$ ), the S-8211D Series enters the normal status.

**Caution** Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charging function.

## 7. 0 V Battery Charging Function "Unavailable"

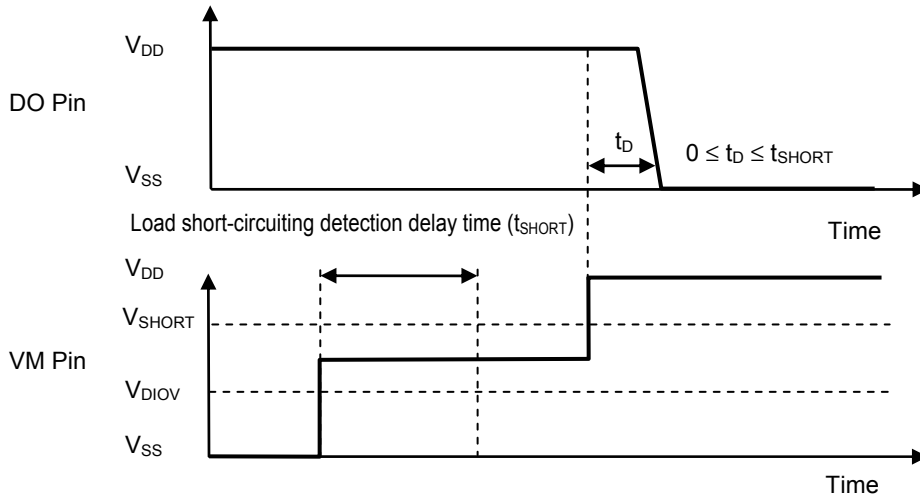
This function inhibits recharging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) or lower, the charging control FET gate is fixed to the EB- pin voltage to inhibit charging. When the battery voltage is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) or higher, charging can be performed.

**Caution** Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charging function.

**9. Delay Circuit**

The detection delay times are determined by dividing a clock of approximately 3.5 kHz by the counter.

**Remark1.** The discharge overcurrent detection delay time ( $t_{DIOV}$ ) and the load short-circuiting detection delay time ( $t_{SHORT}$ ) start when the discharge overcurrent detection voltage ( $V_{DIOV}$ ) is detected. When the load short-circuiting detection voltage ( $V_{SHORT}$ ) is detected over the load short-circuiting detection delay time ( $t_{SHORT}$ ) after the detection of discharge overcurrent detection voltage ( $V_{DIOV}$ ), the S-8211D turns the discharging control FET off within  $t_{SHORT}$  from the time of detecting  $V_{SHORT}$ .



**Figure 10**

**2. With shutdown function**

When any overcurrent is detected and the overcurrent continues for longer than the overdischarge detection delay time ( $t_{DL}$ ) without the load being released, the status changes to the power-down status at the point where the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ).

When the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ) due to overcurrent, the S-8211D Series turns the discharging control FET off via overcurrent detection. In this case, if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time is still lower than the overdischarge detection voltage, S-8211D Series shifts to the power-down status.

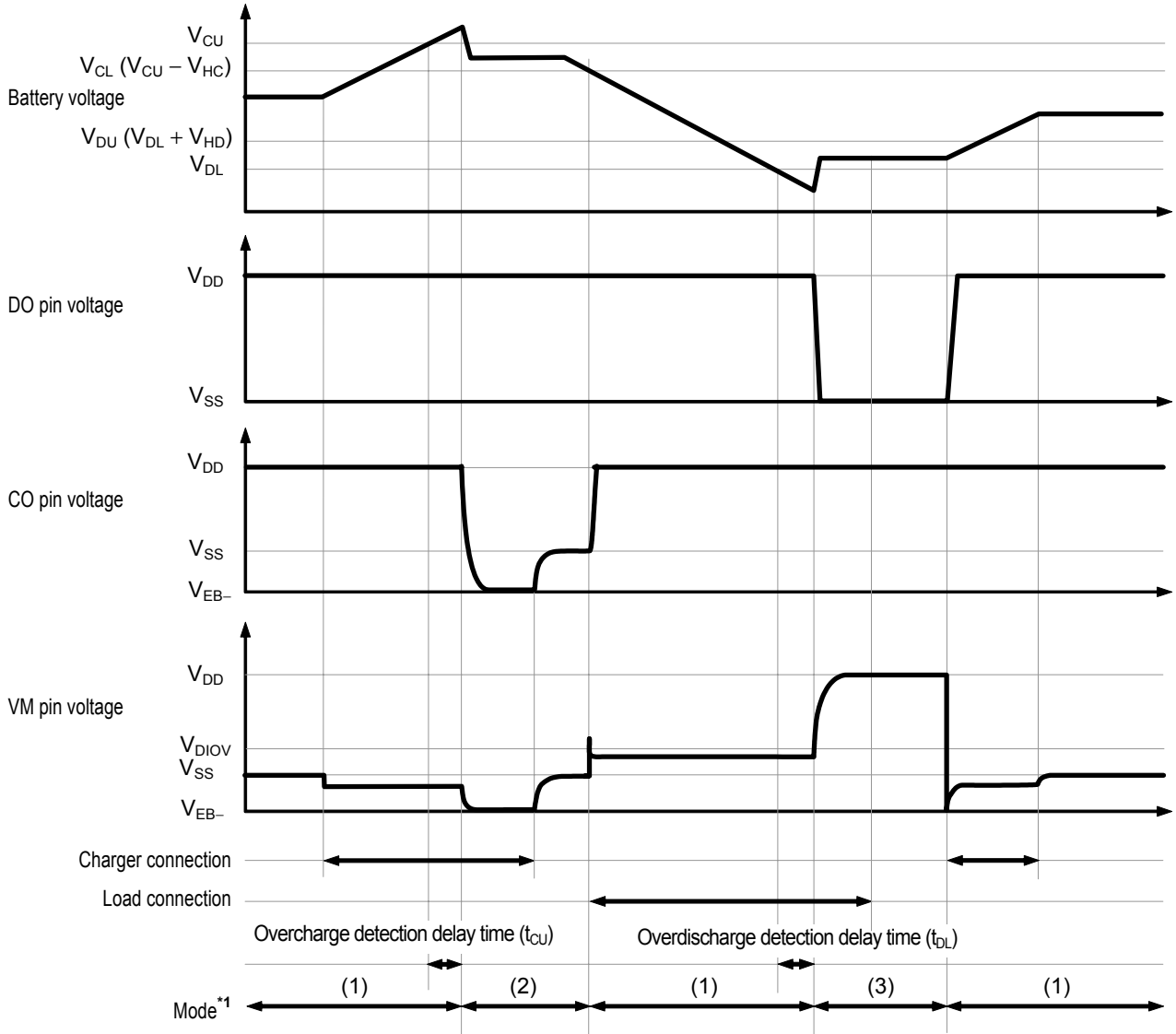
**Without shutdown function**

When any overcurrent is detected and the overcurrent continues for longer than the overdischarge detection delay time ( $t_{DL}$ ) without the load being released, the status changes to the overdischarge status at the point where the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ).

When the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ) due to overcurrent, the S-8211D Series turns the discharging control FET off via overcurrent detection. In this case, if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time is still lower than the overdischarge detection voltage, S-8211D Series shifts to the overdischarge status.

■ Timing Chart

(1) Overcharge Detection, Overdischarge Detection

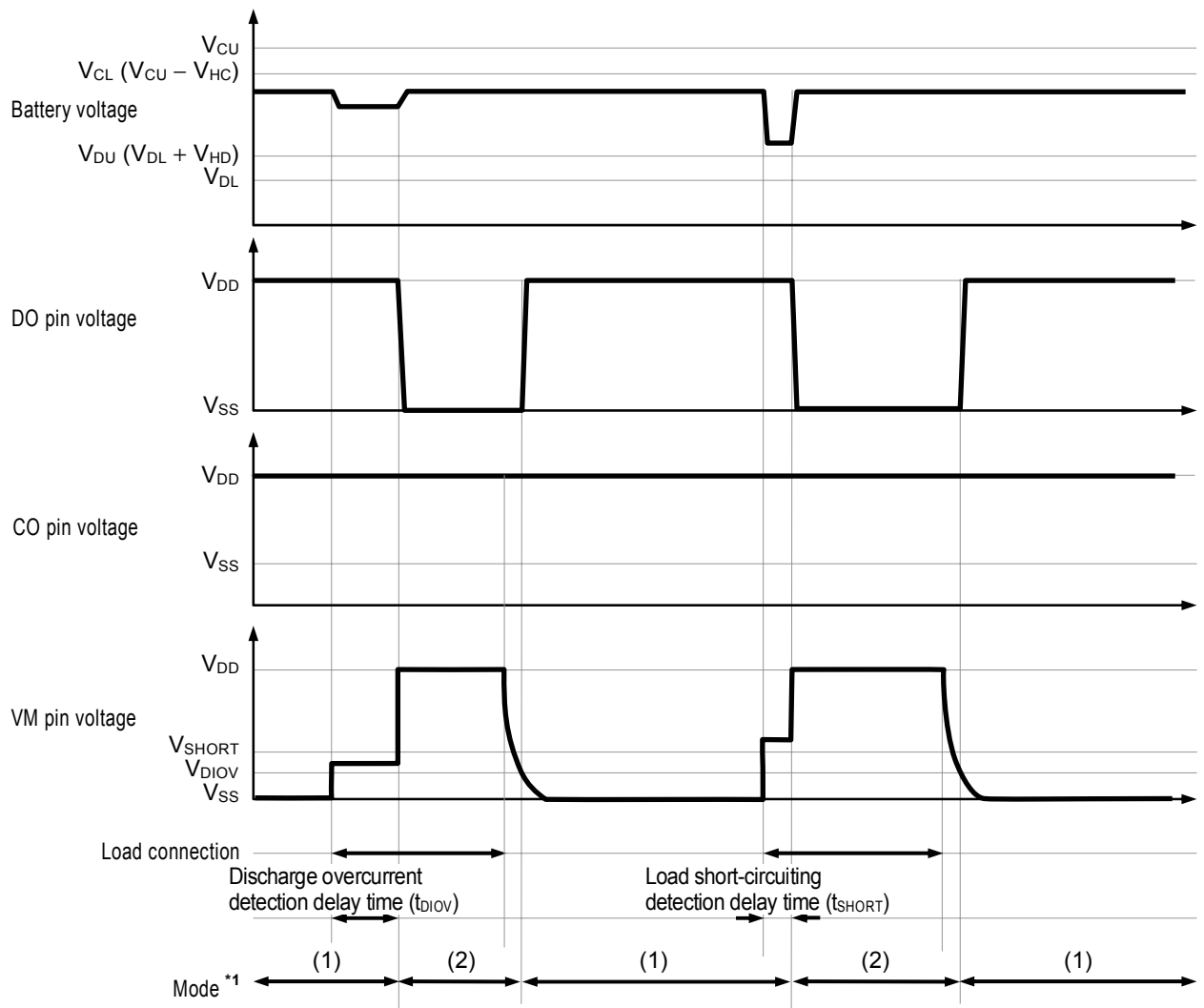


- \*1. (1) : Normal mode
- (2) : Overcharge mode
- (3) : Overdischarge mode

**Remark** The charger is assumed to charge with a constant current.

Figure 11

**(2) Discharge Overcurrent Detection**

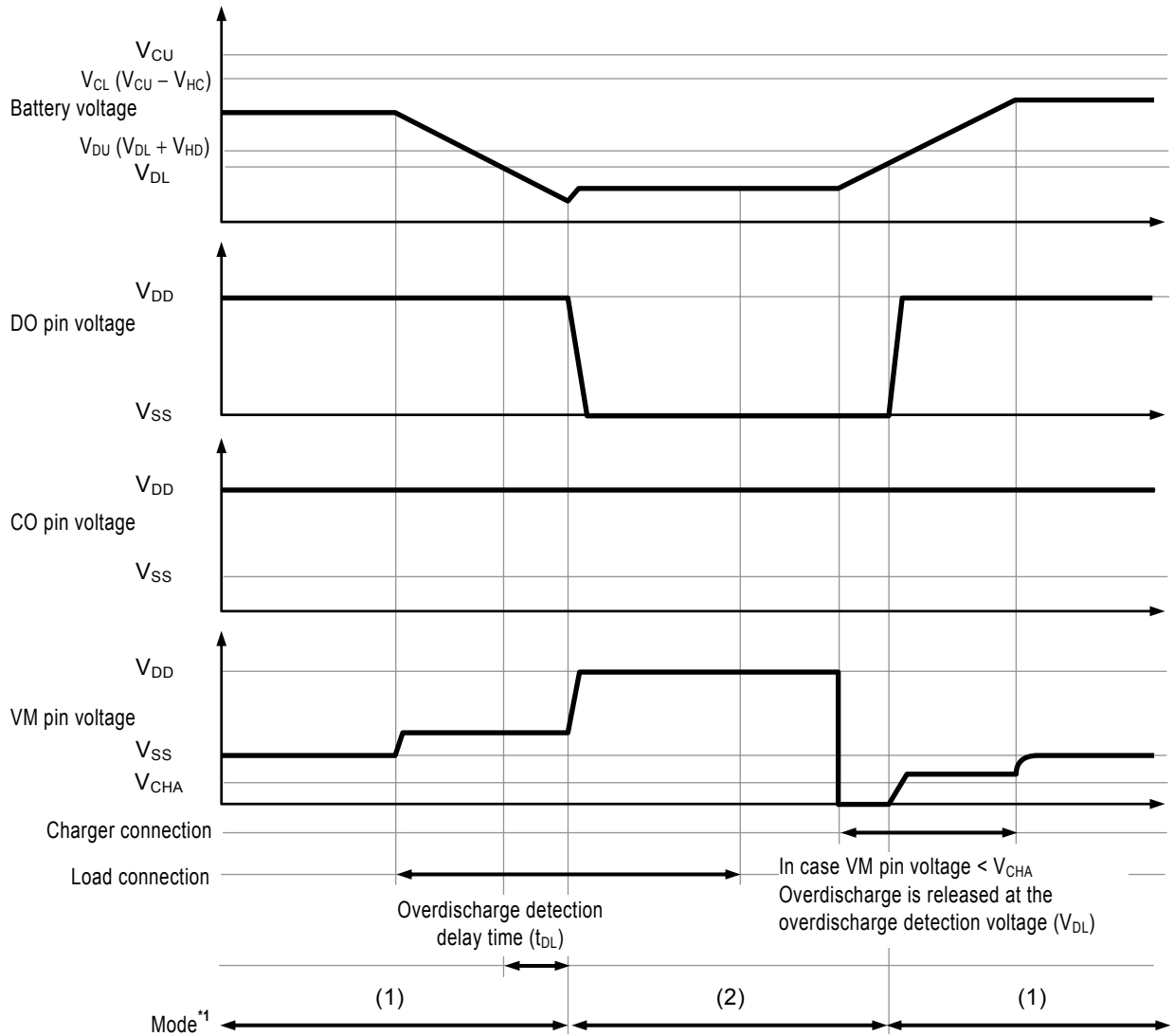


\*1. (1) : Normal mode  
 (2) : Discharge overcurrent mode

**Remark** The charger is assumed to charge with a constant current.

**Figure 12**

(3) Charger Detection

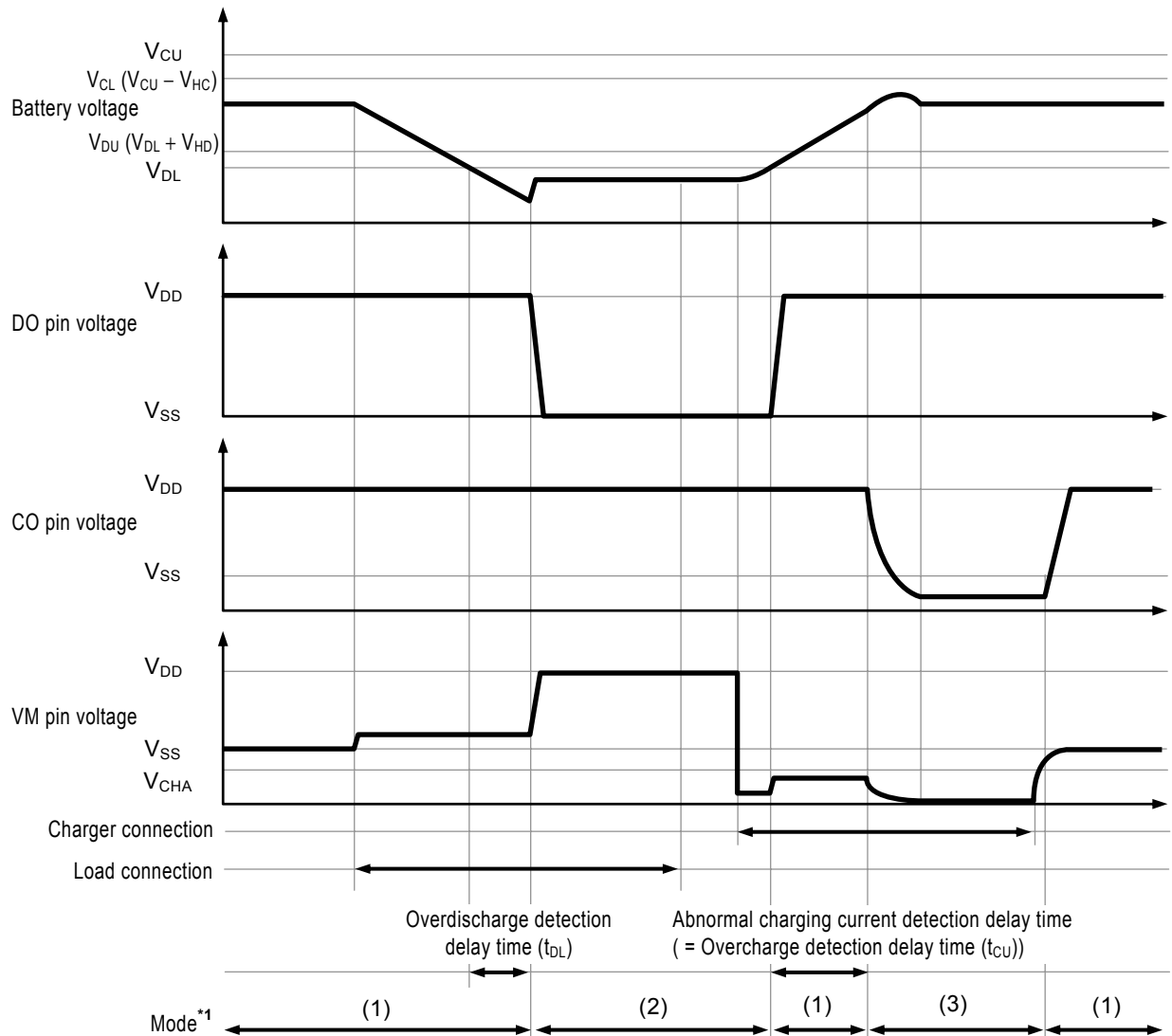


\*1. (1) : Normal mode  
(2) : Overdischarge mode

**Remark** The charger is assumed to charge with a constant current.

Figure 13

**(4) Detection for irregular charging current**



- \*1. (1) : Normal mode
- (2) : Overdischarge mode
- (3) : Overcharge mode

**Remark** The charger is assumed to charge with a constant current.

**Figure 14**

■ **Battery Protection IC Connection Example**

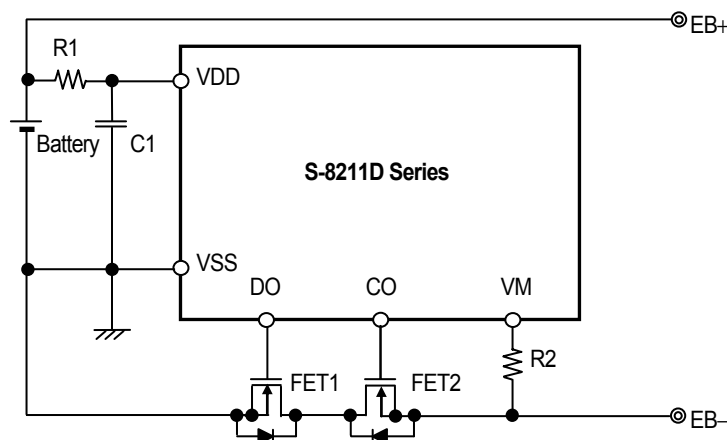


Figure 15

**Table 12 Constants for External Components**

Symbol	Part	Purpose	Typ.	Min.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	—	—	—	Threshold voltage $\leq$ Overdischarge detection voltage <sup>*1</sup> Gate to source withstanding voltage $\geq$ Charger voltage <sup>*2</sup>
FET2	N-channel MOS FET	Charge control	—	—	—	Threshold voltage $\leq$ Overdischarge detection voltage <sup>*1</sup> Gate to source withstanding voltage $\geq$ Charger voltage <sup>*2</sup>
R1	Resistor	ESD protection, For power fluctuation	220 $\Omega$	100 $\Omega$	330 $\Omega$	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption. <sup>*3</sup>
C1	Capacitor	For power fluctuation	0.1 $\mu$ F	0.022 $\mu$ F	1.0 $\mu$ F	Connect a capacitor of 0.022 $\mu$ F or higher between VDD pin and VSS pin. <sup>*4</sup>
R2	Resistor	Protection for reverse connection of a charger	2 k $\Omega$	300 $\Omega$	4 k $\Omega$	Select as large a resistance as possible to prevent current when a charger is connected in reverse. <sup>*5</sup>

\*1. If the threshold voltage of an FET is low, the FET may not cut the charging current. If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

\*2. If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

\*3. If R1 has a high resistance, the voltage between VDD pin and VSS pin may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC. Insert a resistor of 100  $\Omega$  or higher as R1 for ESD protection.

\*4. If a capacitor of less than 0.022  $\mu$ F is connected to C1, DO pin may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.022  $\mu$ F or higher to C1.

\*5. If R2 has a resistance higher than 4 k $\Omega$ , the charging current may not be cut when a high-voltage charger is connected.

**Caution** 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

■ **Precautions**

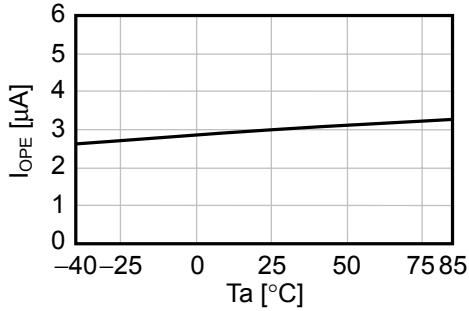
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.



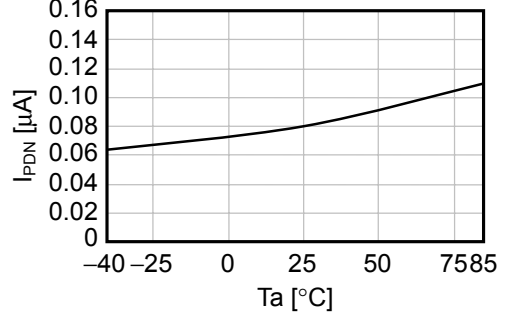
■ Characteristics (Typical Data)

1. Current Consumption

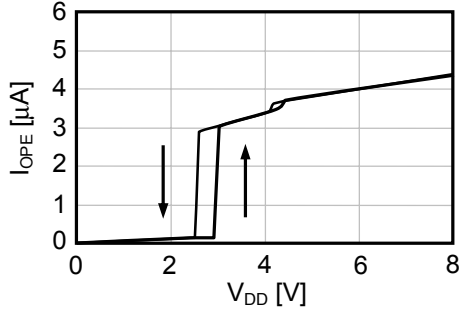
(1)  $I_{OPE}$  vs.  $T_a$



(2)  $I_{PDN}$  vs.  $T_a$

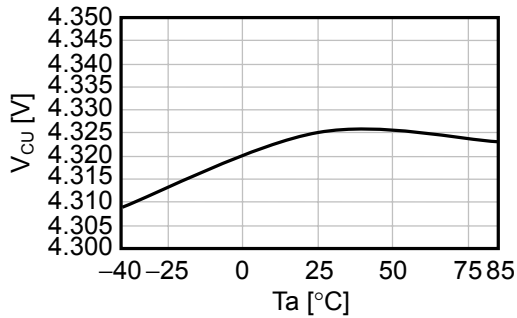


(3)  $I_{OPE}$  vs.  $V_{DD}$

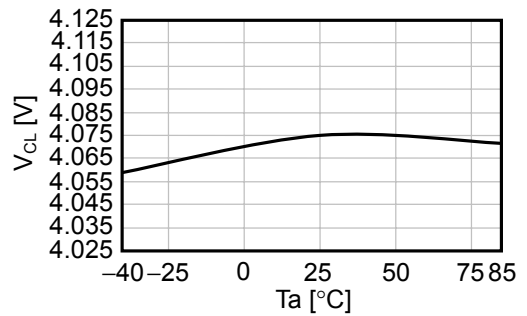


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Time

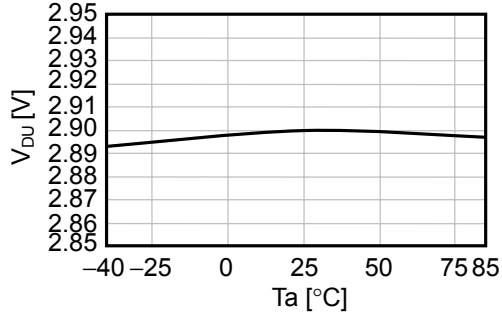
(1)  $V_{CU}$  vs.  $T_a$



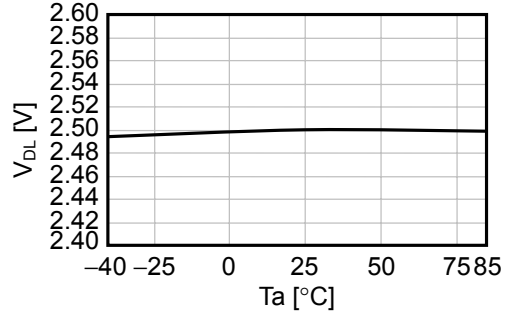
(2)  $V_{CL}$  vs.  $T_a$



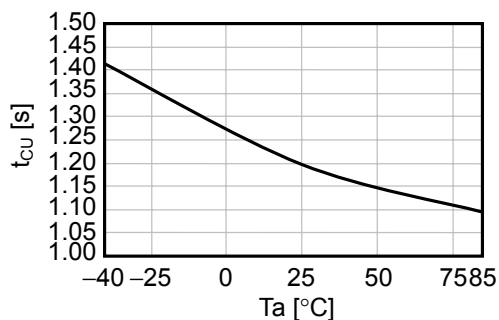
(3)  $V_{DU}$  vs.  $T_a$



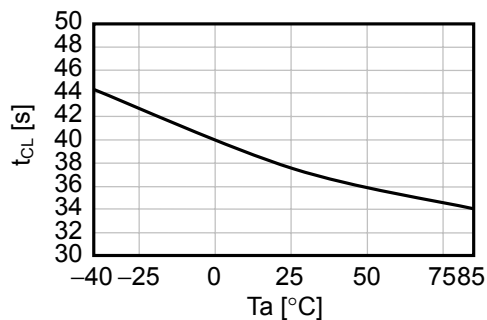
(4)  $V_{DL}$  vs.  $T_a$



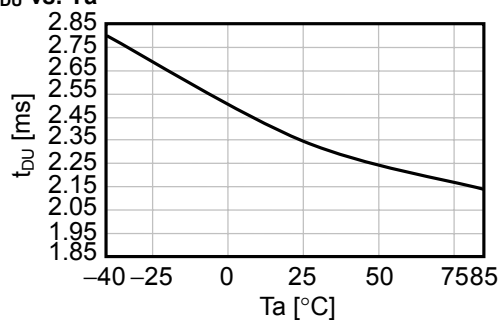
(5)  $t_{CU}$  vs.  $T_a$



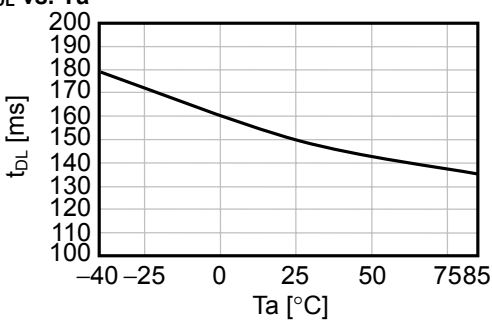
(6)  $t_{CL}$  vs.  $T_a$



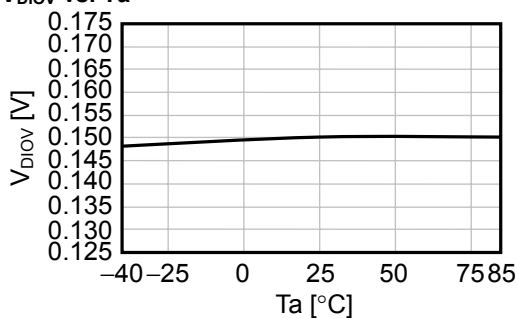
(7)  $t_{DU}$  vs.  $T_a$



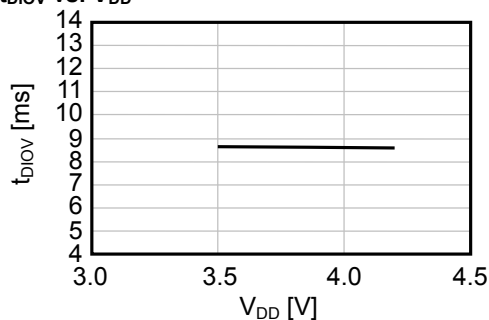
(8)  $t_{DL}$  vs.  $T_a$



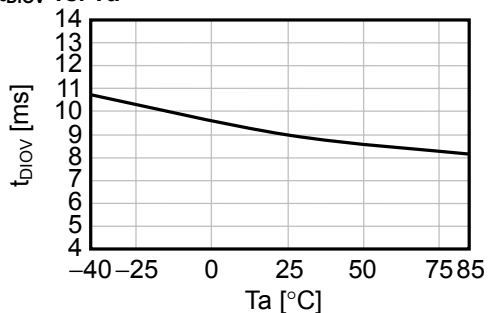
(9)  $V_{DIOV}$  vs.  $T_a$



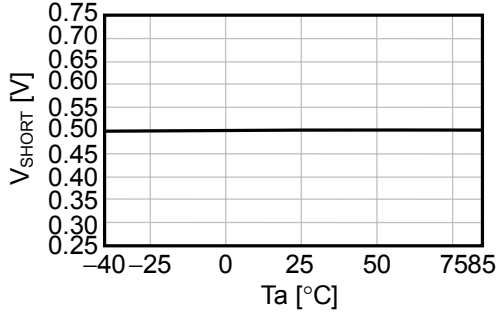
(10)  $t_{DIOV}$  vs.  $V_{DD}$



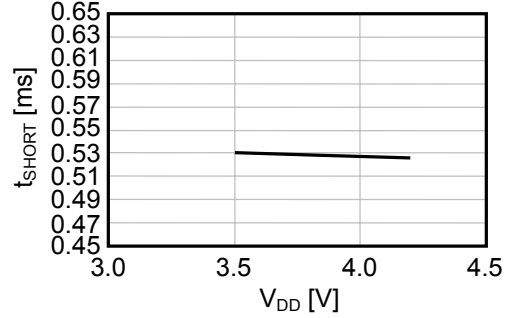
(11)  $t_{DIOV}$  vs.  $T_a$



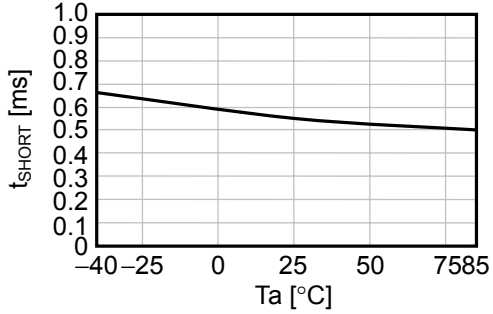
(12)  $V_{SHORT}$  vs.  $T_a$



(13)  $t_{SHORT}$  vs.  $V_{DD}$

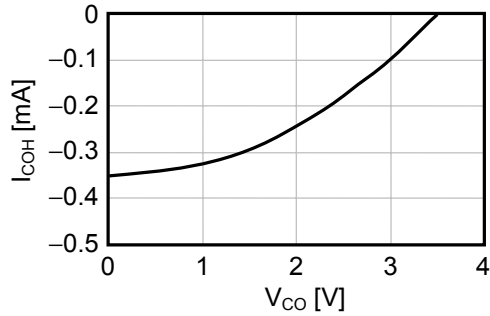


(14)  $t_{SHORT}$  vs.  $T_a$

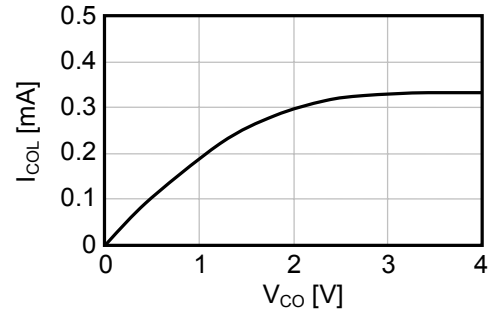


### 3. CO pin / DO pin

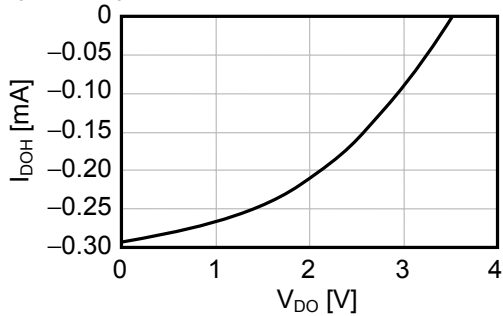
(1)  $I_{COH}$  vs.  $V_{CO}$



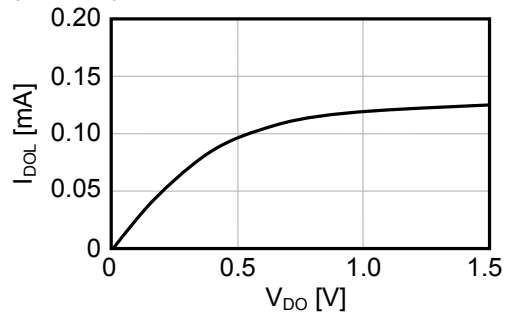
(2)  $I_{COL}$  vs.  $V_{CO}$



(3)  $I_{DOH}$  vs.  $V_{DO}$

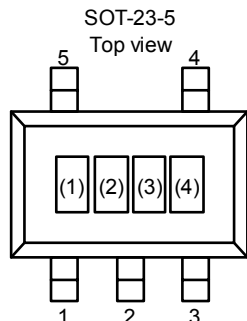


(4)  $I_{DOL}$  vs.  $V_{DO}$



■ **Marking Specifications**

**(1) SOT-23-5**



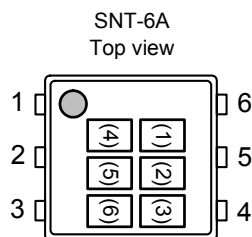
(1) to (3): Product Code (refer to **Product Name vs. Product Code**)  
 (4) : Lot number

**Product Name vs. Product Code**

Product Name	Product Code		
	(1)	(2)	(3)
S-8211DAB-M5T1G	R	2	B
S-8211DAE-M5T1G	R	2	E
S-8211DAH-M5T1G	R	2	H
S-8211DAI-M5T1G	R	2	I
S-8211DAJ-M5T1G	R	2	J
S-8211DAK-M5T1G	R	2	K
S-8211DAL-M5T1G	R	2	L
S-8211DAM-M5T1G	R	2	M

**Remark** Please contact our sales office for the products other than those specified above.

**(2) SNT-6A**

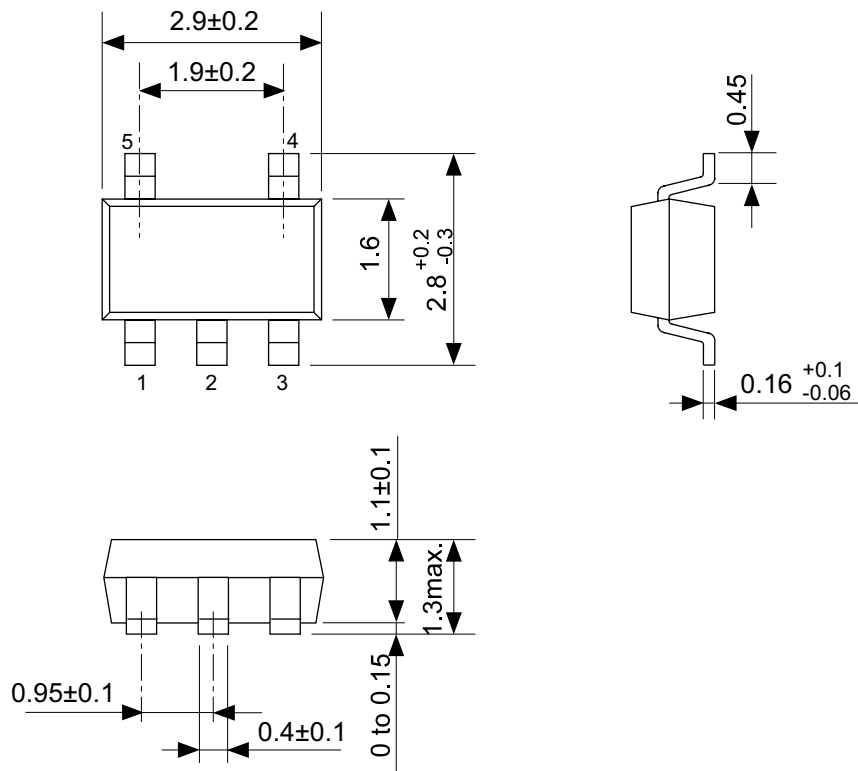


(1) to (3): Product Code (refer to **Product Name vs. Product Code**)  
 (4) to (6): Lot number

**Product Name vs. Product Code**

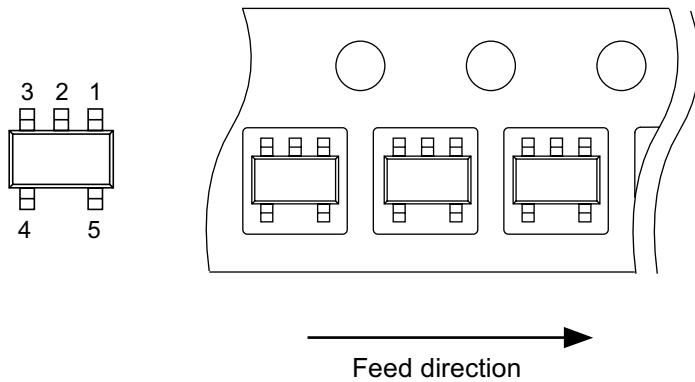
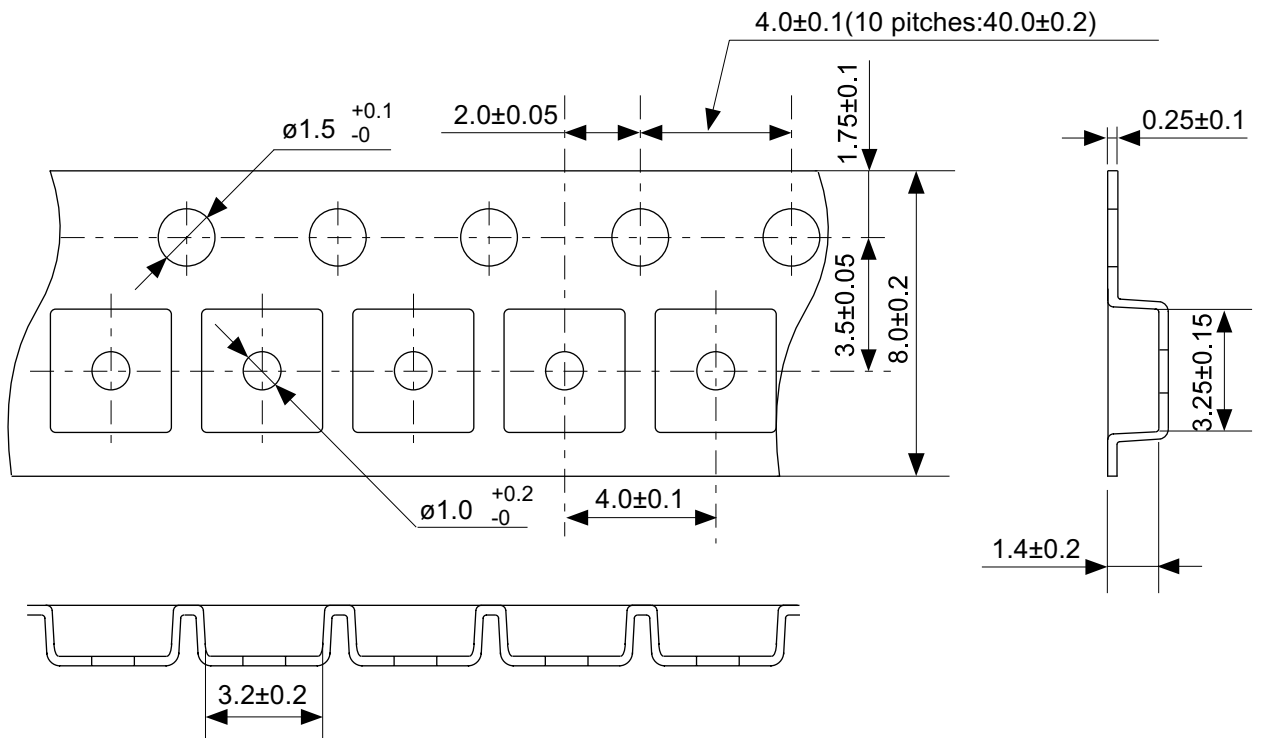
Product Name	Product Code		
	(1)	(2)	(3)
S-8211DAB-I6T1G	R	2	B
S-8211DAE-I6T1G	R	2	E
S-8211DAF-I6T1G	R	2	F
S-8211DAG-I6T1G	R	2	G

**Remark** Please contact our sales office for the products other than those specified above.



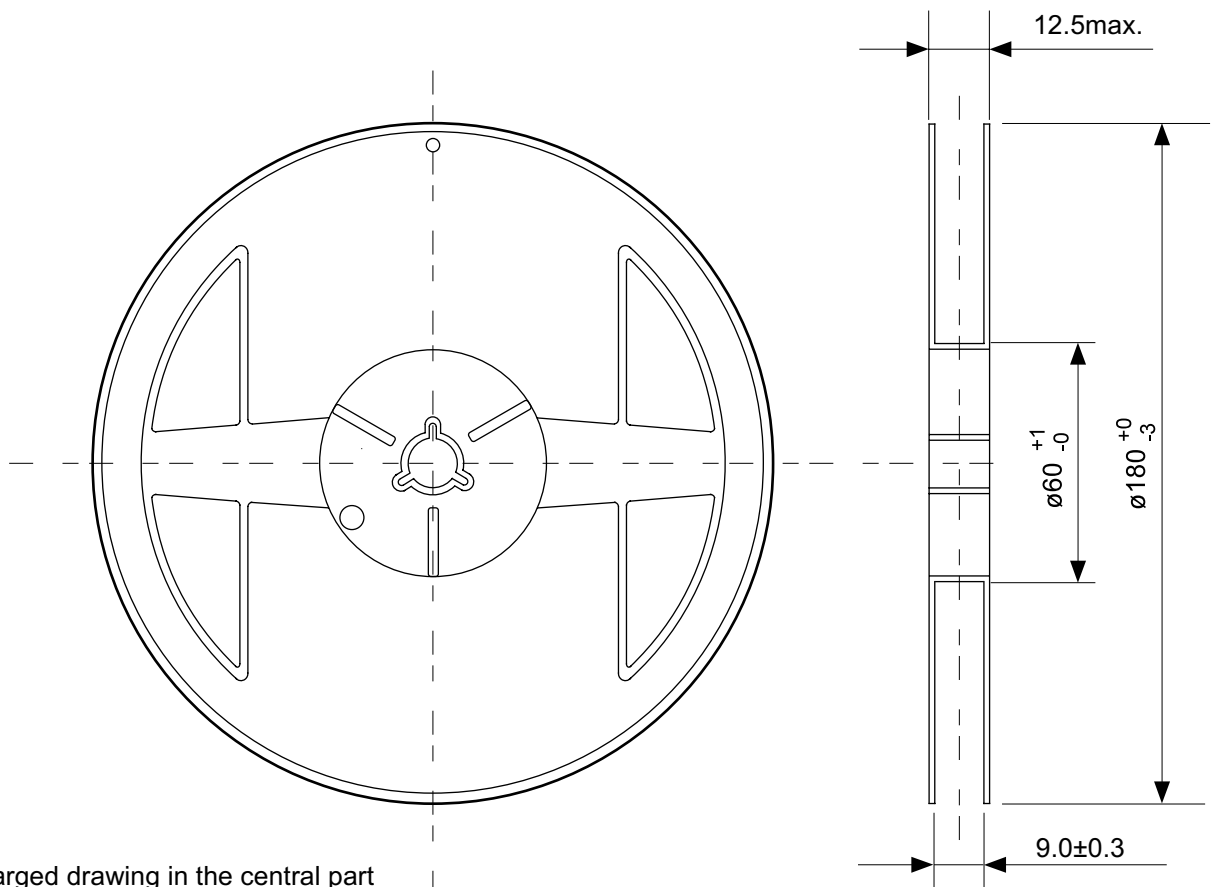
No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm
Seiko Instruments Inc.	

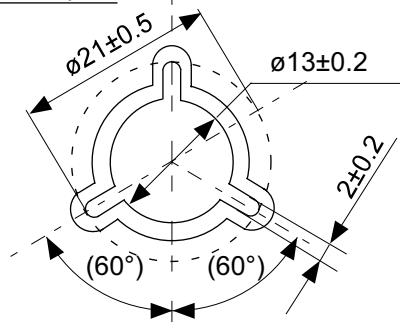


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

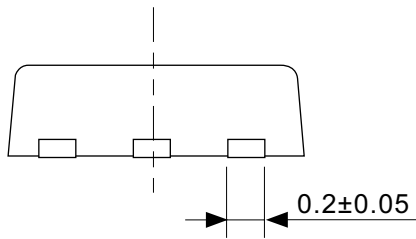
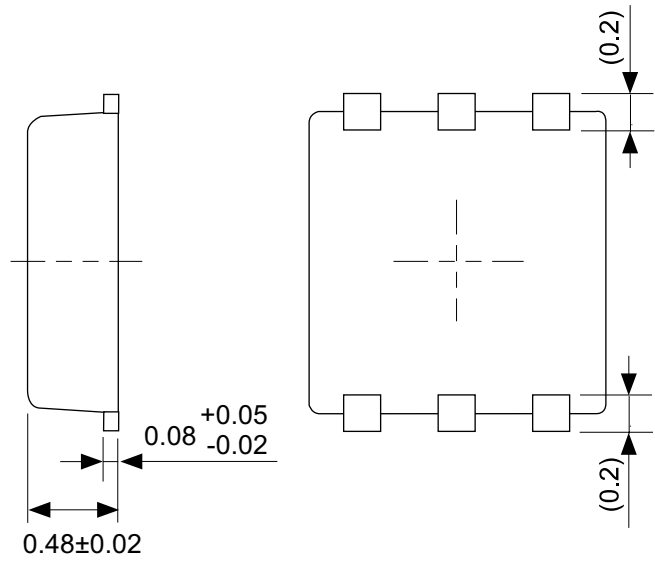
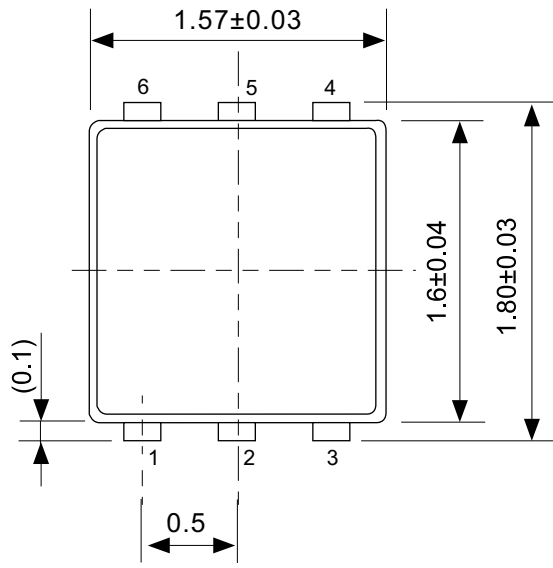


Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

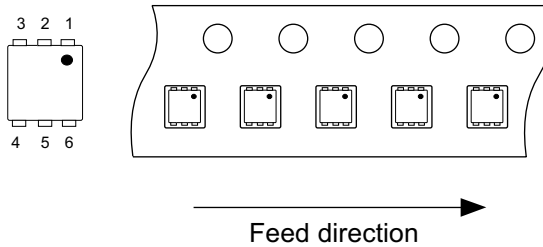
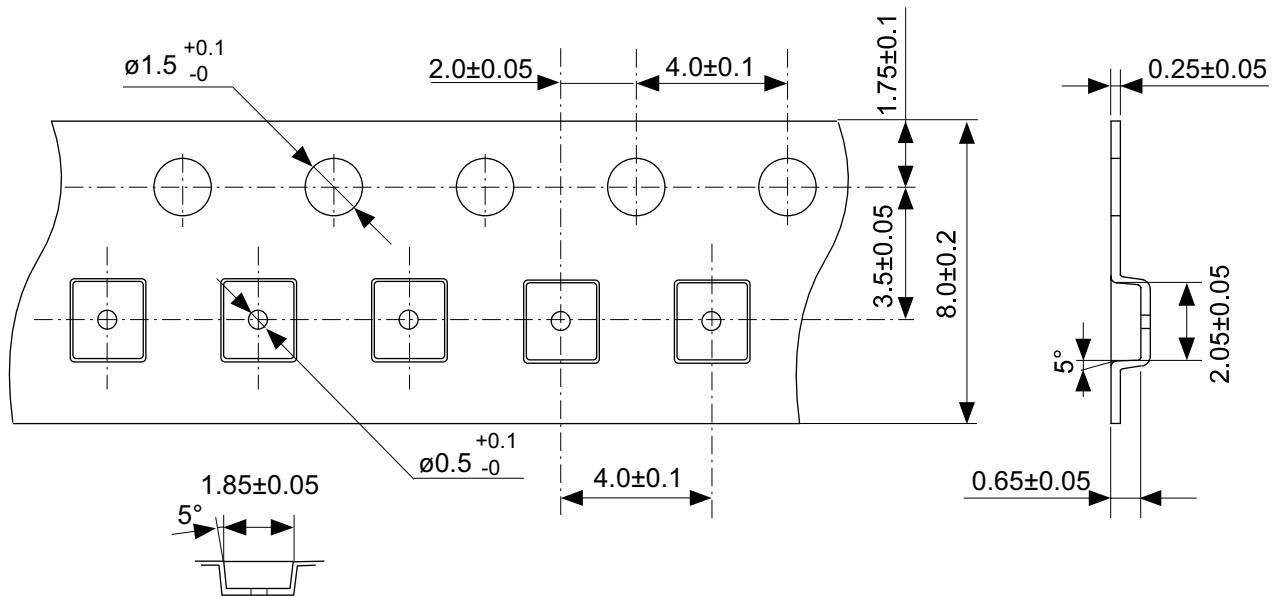
TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			



No. PG006-A-P-SD-2.0

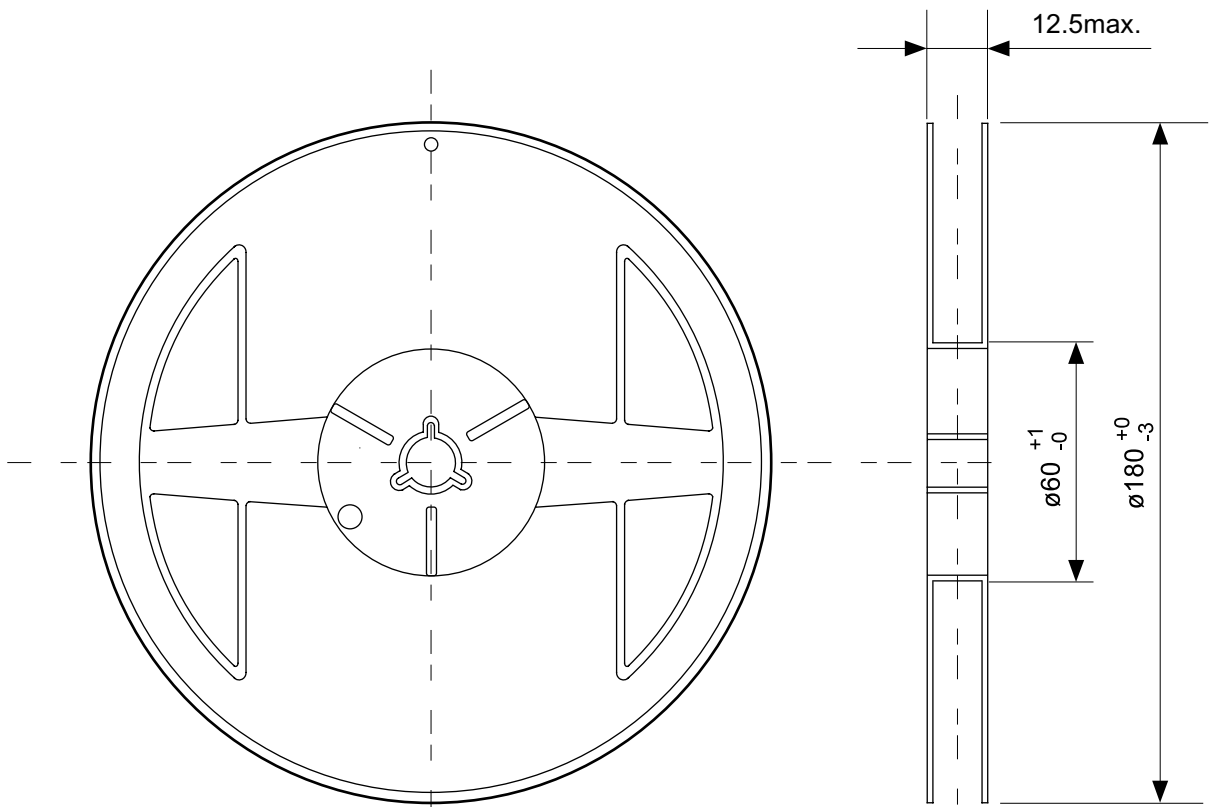
TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



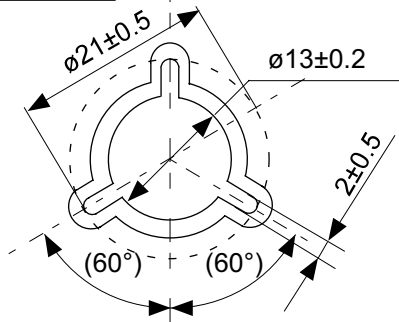


No. PG006-A-C-SD-1.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

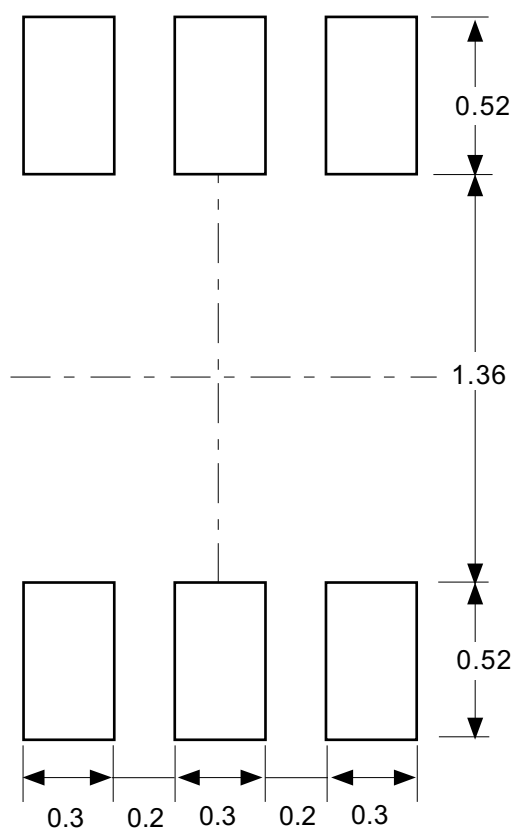


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			



Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がる場合がありますのでご配慮ください。

No. PG006-A-L-SD-3.0

TITLE	SNT-6A-A-Land Recommendation
No.	PG006-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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