HCPL-5300, HCPL-5301, HCPL-530K, 5962-96852 [1]

Intelligent Power Module and Gate Drive Interface Hermetically Sealed Optocouplers

Data Sheet

Description

The HCPL-530x devices consist of a GaAsP LED optically coupled to an integrated high gain photo detector in a hermetically sealed package. The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial product or with full MIL-PRF-38534 Class Level H or K testing or from the DLA Standard Microcircuit Drawing (SMD) 5962-96852. All devices are manufactured and tested on a MIL-PRF-38534 certified line, and Class H and K devices are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits. Minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. An on-chip 20-kΩ output pull-up resistor can be enabled by shorting output pins 6 and 7, thus eliminating the need for an external pull-up resistor in common IPM applications. Specifications and performance plots are given for typical IPM applications.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Features

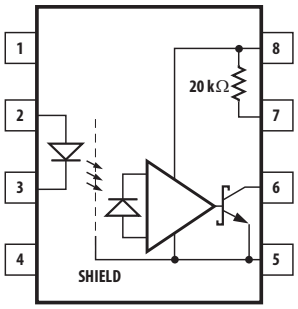
- Performance specified over full military temperature Range: –55°C to +125°C
- Fast maximum propagation delays
  - t_{PHL} = 450 ns
  - t_{PLH} = 650 ns
- Minimized pulse width distortion (PWD = 450 ns)
- High common mode rejection (CMR): 10 kV/µs at V_{CM} = 1000V
- CTR > 30% at I_F = 10 mA
- 1500 Vdc withstand test voltage
- Manufactured and tested on a MIL-PRF-38534 certified line
- Hermetically sealed packages
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- QML-38534, Class H and K
- HCPL-4506 function compatibility

Applications

- Military and space
- High reliability systems
- Harsh industrial environments
- Transportation, medical, and life critical systems
- IPM isolation
- Isolated IGBT/MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters

1. See Selection Guide–Lead Configuration Options for available extensions.

Schematic Diagram



Truth Table	
LED	V_O
ON	L
OFF	H

NOTE The connection of a 0.1-µF bypass capacitor between pins 5 and 8 is recommended.

Selection Guide–Lead Configuration Options

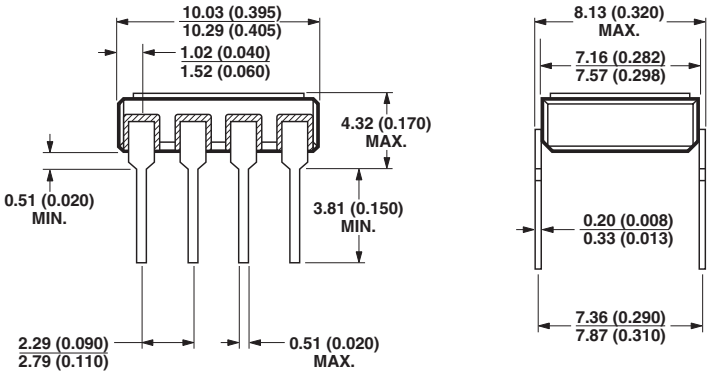
Part Numbers and Options	
Commercial	HCPL-5300
MIL-PRF-38534, Class H	HCPL-5301
MIL-PRF-38534, Class K	HCPL-530K
Standard Lead Finish[a]	Gold Plate
Solder Dipped[b]	Option #200
Butt Cut/Gold Plate[a]	Option #100
Gull Wing/Soldered[b]	Option #300
Class H SMD Part #	
Prescript for all below	5962-
Gold Plate[a]	9685201HPC
Solder Dipped[b]	9685201HPA
Butt Cut/Gold Plate[a]	9685201HYC
Butt Cut/Soldered[b]	9685201HYA
Gull Wing/Soldered[b]	9685201HXA
Class K SMD Part #	
Prescript for all below	5962-
Gold Plate[a]	9685201KPC
Solder Dipped[b]	9685201KPA
Butt Cut/Gold Plate[a]	9685201KYC
Butt Cut/Soldered[b]	9685201KYA
Gull Wing/Soldered[b]	9685201KXA

a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.

b. Solder lead finish: Sn63/Pb37.

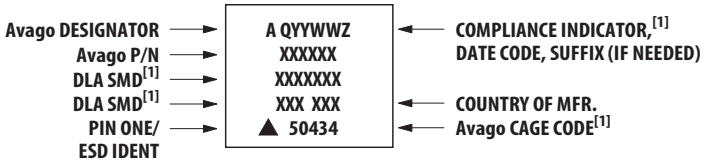
Outline Drawing

8-Pin DIP, Through Hole, 1 Channel



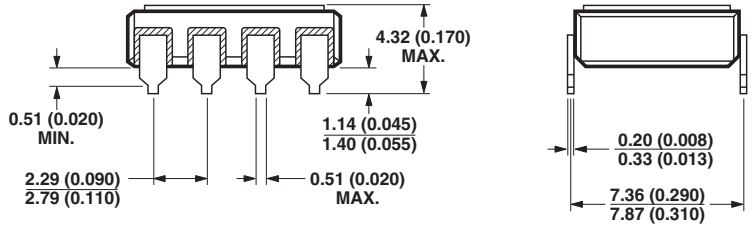
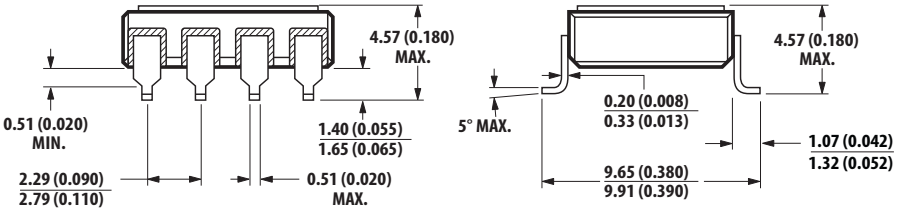
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



[1] QML PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	Surface-mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H and Class K product in 8-pin DIP.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H and Class K product in 8-pin DIP. DLA Drawing (SMD) part numbers contain provisions for lead finish.
300	Surface-mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H and Class K product in 8-pin DIP. This option has solder-dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_S	–65	+150	°C
Operating Temperature	T_A	–55	+125	°C
Junction Temperature	T_J	—	+175	°C
Lead Solder Temperature		—	260 for 10 sec	°C
Average Input Current	$I_{F(AVG)}$	—	25	mA
Peak Input Current (50% duty cycle, ≤1 µs pulse width)	$I_{F(PEAK)}$	—	50	mA
Peak Transient Input Current (≤1 µs pulse width, 300 pps)		—	1.0	A
Reverse Input Voltage (Pin 3-2)	V_R	—	5	V
Average Output Current (Pin 6)	$I_{O(AVG)}$	—	15	mA
Resistor Voltage (Pin 7)	V_7	–0.5	V_{CC}	V
Output Voltage (Pin 6-5)	V_O	–0.5	30	V
Supply Voltage (Pin 8-5)	V_{CC}	–0.5	30	V
Output Power Dissipation	P_O	—	100	mW
Total Power Dissipation	P_T	—	145	mW

ESD Classification

(MIL-STD-883, Method 3015)	▲, Class 1

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	30	V
Output Voltage	V_O	0	30	V
Input Current (ON)	$I_{F(ON)}$	10	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	–5	0.8	V

Electrical Specifications

Over recommended operating conditions (T_A = –55°C to +125°C, V_{CC} = +4.5V to 30V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = –5V to 0.8V) unless otherwise specified.

Parameter	Symbol	Group A Subgroups[a]	Min	Typ[b]	Max	Unit	Test Conditions	Fig	Note
Current Transfer Ratio	CTR	1, 2, 3	30	90	—	%	I_F = 10 mA, V_O = 0.6V		c
Low Level Output Current	I_{OL}	1, 2, 3	3.0	9.0	—	mA	I_F = 10 mA, V_O = 0.6V	1, 2	
Low Level Output Voltage	V_{OL}	1, 2, 3	—	0.3	0.6	V	I_O = 2.4 mA		
Input Threshold Current	I_{TH}	1, 2, 3	—	1.5	5.0	mA	V_O = 0.8V, I_O = 0.75 mA	1	d
High Level Output Current	I_{OH}	1, 2, 3	—	5	75	µA	V_F = 0.8V	3	
High Level Supply Current	I_{CCH}	1, 2, 3	—	0.6	1.5	mA	V_F = 0.8V, V_O = Open		d
Low Level Supply Current	I_{CCL}	1, 2, 3	—	0.6	1.5	mA	I_F = 10 mA, V_O = Open		d
Input Forward Voltage	V_F	1, 2, 3	1.0	1.5	1.8	V	I_F = 10 mA	4	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		—	–1.6	—	mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	1, 2, 3	5	—	—	V	I_R = 100 µA		
Input Capacitance	C_{IN}		—	90	—	pF	f = 1 MHz, V_F = 0V		
Input-Output Insulation Leakage Current	I_{I-O}	1	—	—	1.0	µA	RH ≤ 65%, t = 5 sec, V_{I-O} = 1500 Vdc, T_A = 25°C		e
Resistance (Input-Output)	R_{I-O}		—	1012	—	Ω	V_{I-O} = 500 Vdc		e
Capacitance (Input-Output)	C_{I-O}		—	2.4	—	pF	f = 1 MHz		e
Internal Pull-up Resistor	R_L	1	14	20	28	kΩ	T_A = 25°C		f, g, h
Internal Pull-up Resistor Temperature Coefficient	$\Delta R_L/\Delta T_A$		—	0.014	—	kΩ/°C			

a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD, Class H and K parts receive 100% testing at 25°C, +125°C, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11 respectively).

b. All typical values at 25°C, V_{CC} = 15V.

c. Current Transfer Ratio in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.

d. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.

e. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.

f. The internal 20 kΩ resistor can be used by shorting pins 6 and 7 together.

g. Due to the tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external 20 kΩ 1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 8.

h. The RL = 20 kΩ, C_L = 100 pF represents a typical IPM (Intelligent Power Module) load.

Switching Specifications (R_L= 20 kΩ External)

Over recommended operating conditions (T_A = –55°C to +125°C, V_{CC} = +4.5V to 30V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = –5V to 0.8V) unless otherwise specified.

Parameter	Symbol	Group A Subgroups[a]	Min	Typ[b]	Max	Unit	Test Conditions		Fig	Note
Propagation Delay Time to Low Output Level	t_{PHL}	9, 10, 11	30	180	450	ns	C_L = 100 pF	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8V, V_{CC} = 15.0V, V_{THLH} = 2.0V, V_{THHL} = 1.5V	5, 7, 9,-12	c, d, e, f, g
			—	100	—	ns	C_L = 10 pF			
Propagation Delay Time to High Output Level	t_{PLH}	9, 10, 11	250	350	650	ns	C_L = 100 pF			
			—	130	—	ns	C_L = 10 pF			
Pulse Width Distortion	PWD	9, 10, 11	—	150	450	ns	C_L = 100 pF			h
Propagation Delay Difference Between Any Two Parts	t_{PLH} -t_{PHL}	9, 10, 11	–170	140	500	ns				i
Output High Level Common Mode Immunity Transient	$\|CM_H\|$	9	10	17	—	kV/µs	I_F = 0 mA, V_O > 3.0V	V_{CC} = 15.0V, C_L = 100 pF, V_{CM} = 1000 V_{P-P} T_A = 25°C	6, 17, 18, 21	j, k
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	9	10	17	—	kV/µs	I_F = 10 mA V_O < 1.0V			l, k

a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD, Class H and K parts receive 100% testing at 25°C, +125°C, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11 respectively).

b. All typical values at 25°C, V_{CC} = 15V.

c. Pulse: f = 20 kHz, Duty Cycle = 10%.

d. The internal 20 kΩ resistor can be used by shorting pins 6 and 7 together.

e. Due to the tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external 20 kΩ 1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 8.

f. The R_L = 20 kΩ, C_L = 100 pF represents a typical IPM (Intelligent Power Module) load.

g. Use of a 0.1-µF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.

h. Pulse Width Distortion (PWD) is defined as the difference between t_{PLH} and t_{PHL} for any given device.

i. The difference in t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications.)

j. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output remains in a Logic High state (i.e., V_O > 3.0V).

k. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

l. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output remains in a Logic Low state (i.e., V_O < 1.0V).

Switching Specifications (R_L = Internal Pull-up)

Over recommended operating conditions (T_A = –55°C to +125°C, V_{CC} = +4.5V to 30V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = –5V to 0.8V) unless otherwise specified.

Parameter	Symbol	Group A Subgroups[a]	Min	Typ[b]	Max	Unit	Test Conditions		Fig	Note
Propagation Delay Time to Low Output Level	t_{PHL}	9, 10, 11	20	185	500	ns	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8V, V_{CC} = 15.0V, C_L = 100 pF, V_{THLH} = 2.0V V_{THHL} = 1.5V		5, 8	c, d, e, f, g
Propagation Delay Time to High Output Level	t_{PLH}	9, 10, 11	220	415	750	ns				
Pulse Width Distortion	PWD	9, 10, 11	—	150	600	ns				h
Propagation Delay Difference Between Any Two Parts	t_{PLH} -t_{PHL}	9, 10, 11	–225	150	650	ns				i
Output High Level Common Mode Transient Immunity	$\|CM_H\|$		—	10	—	kV/µs	I_F = 0 mA, V_O > 3.0V	V_{CC} = 15.0V, C_L = 100 pF, V_{CM} = 1000 V_{P-P} T_A = 25°C	6, 21	j
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$		—	10	—	kV/µs	I_F = 16 mA V_O < 1.0V			k
Power Supply Rejection	PSR		—	1.0	—	V_{P-P}	Square Wave, t_{RISE}, t_{FALL} > 5 ns, no bypass capacitors.			g

a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD, Class H and K parts receive 100% testing at 25°C, +125°C, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11 respectively).

b. All typical values at 25°C, V_{CC} = 15V.

c. Pulse: f = 20 kHz, Duty Cycle = 10%.

d. The internal 20 kΩ resistor can be used by shorting pins 6 and 7 together.

e. Due to the tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external 20 kΩ 1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 8.

f. The R_L = 20 kΩ, C_L = 100 pF represents a typical IPM (Intelligent Power Module) load.

g. Use of a 0.1-µF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.

h. Pulse Width Distortion (PWD) is defined as the difference between t_{PLH} and t_{PHL} for any given device.

i. The difference in t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications.)

j. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output remains in a Logic High state (i.e., V_O > 3.0V).

k. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output remains in a Logic Low state (i.e., V_O < 1.0V).

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 14. The HCPL-530x improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pins and output ground as shown in Figure 15. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 13), can achieve 10 kV/µs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 13 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through C_{LEDO1} and C_{LEDO2} in Figure 15. Many factors influence the effect and magnitude of the direct coupling including the use of an internal or external output pull-up resistor, the position of the LED current setting resistor, the connection of the unused input package pins, and the value of the capacitor at the optocoupler output (CL).

Techniques to keep the LED in the proper state and minimize the effect of the direct coupling are discussed in the next two sections.

CMR With the LED on (CMR_L)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum I_{TH} of 5.0 mA (see Figure 1) to achieve 10 kV/µs CMR. Capacitive coupling is higher when the internal load resistor is used (due to C_{LEDO2}) and an I_F = 16 mA is required to obtain 10 kV/µs CMR.

The placement of the LED current setting resistor affects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 16 is connected to the anode. Figure 17 shows the AC equivalent circuit for Figure 16 during common mode transients. During a $+dV_{CM/dt}$ in Figure 17, the current available at the LED anode (I_{TOTAL}) is limited by the series resistor. The LED current (I_F) is reduced from its DC value by an amount equal to the current that flows through C_{LEDP} and C_{LEDO1}. The situation is made worse because the current through C_{LEDO1} has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 13) places the current setting resistor in series with the LED cathode. Figure 18 is the AC equivalent circuit for Figure 13 during common mode transients. In this case, the LED current is not reduced during a $+dV_{CM/dt}$ transient because the current flowing through the package capacitance is supplied by the power supply. During a $dV_{CM/dt}$ transient, however, the LED current is reduced by the amount of current flowing through C_{LEDN}. But better CMR performance is achieved since the current flowing in C_{LEDO1} during a negative transient acts to keep the output low.

Coupling to the LED and output pins is also affected by the connection of pins 1 and 4. If CMR is limited by perturbations in the LED on current, as it is for the recommended drive circuit (Figure 13), pins 1 and 4 should be connected to the input circuit common. However, if CMR performance is limited by direct coupling to the output when the LED is off, pins 1 and 4 should be left unconnected.

CMR with the LED Off (CMR_H)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $+dV_{CM/dt}$ transient in Figure 18, the current flowing through C_{LEDN} is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$, the LED remains off and no common mode failure occurs. Even if the LED momentarily turns on, the 100 pF capacitor from pins 6-5 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 13) provides about 10V of margin between the lowest optocoupler output voltage and a 3V IPM threshold during a 10 kV/µs transient with V_{CM} = 1000V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 18, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 19, cannot keep the LED off during a $+dV_{CM/dt}$ transient, it is not desirable for applications requiring ultra high CMR_H performance. Figure 20 is the AC equivalent circuit for Figure 16 during common mode transients. Essentially all the current flowing through C_{LEDN} during a $+dV_{CM/dt}$ transient must be supplied by the LED. CMR_H failures can occur at dv/dt rates where the current through the LED and C_{LEDN} exceeds the input threshold. Figure 21 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.

IPM Dead Time and Propagation Delay Specifications

These devices include a Propagation Delay Difference specification intended to help designers minimize *dead time* in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction results in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time, the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst-case optocoupler propagation delay waveforms, as shown in Figure 23. A minimum dead time of zero is achieved in Figure 23 when the signal to turn on LED2 is delayed by (t_{PLHmax} - t_{PHLmin}) from the LED1 turn off. This delay is the maximum value for the propagation delay difference specification which is specified at 500 ns for the HCPL-530x over an operating temperature range of –55°C to +125°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest t_{PLH} and another with the slowest t_{PHL} are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the t_{PLH} and t_{PHL} propagation delays as shown in Figure 24. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the HCPL-530x is 670 ns (= 500 ns – (–170 ns)) over an operating temperature range of –55°C to +125°C.

Figure 1 Typical Transfer Characteristics

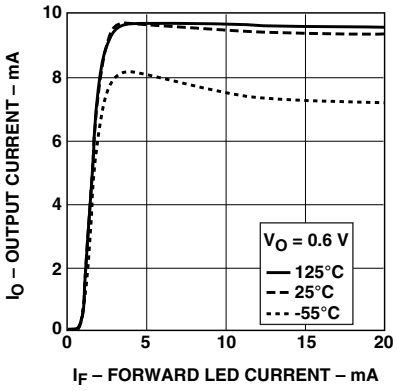


Figure 2 Normalized Output Current vs. Temperature

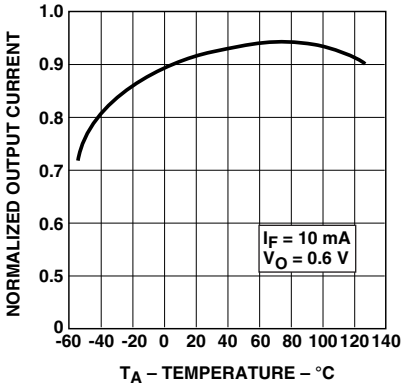


Figure 3 High Level Output Current vs. Temperature

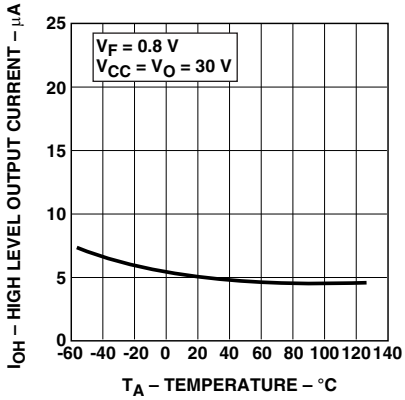


Figure 4 Input Current vs. Forward Voltage

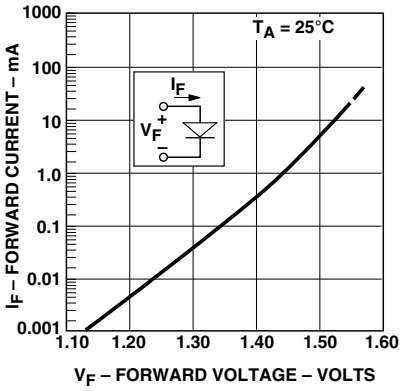
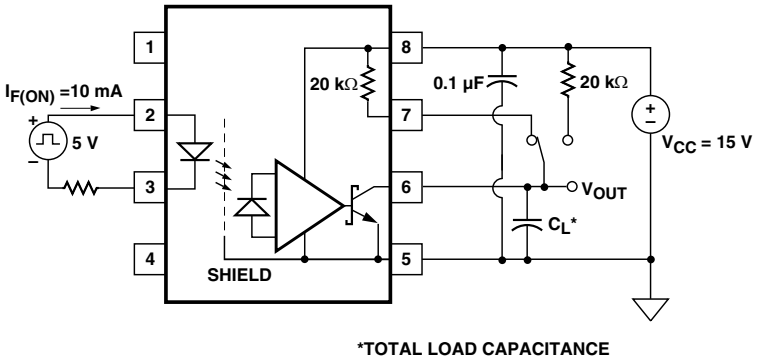


Figure 5 Propagation Delay Test Circuit



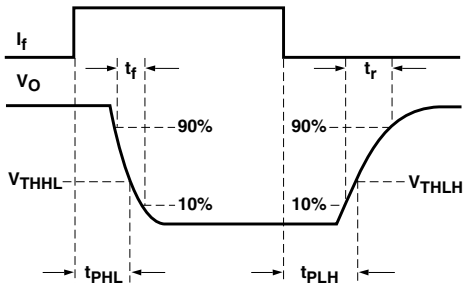


Figure 6 CMR Test Circuit. Typical CMR Waveform

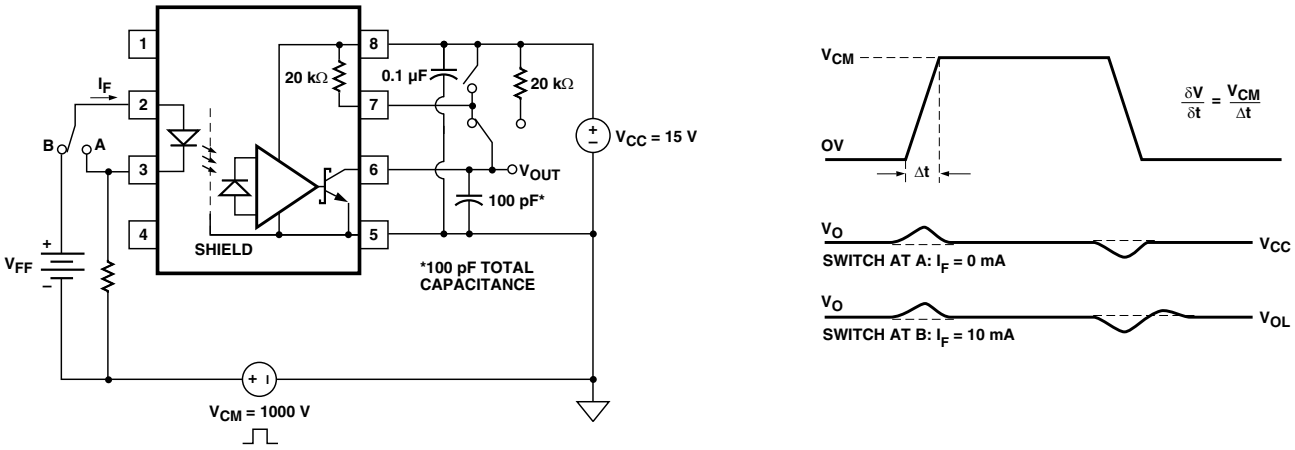


Figure 7 Propagation Delay with External 20 kΩ R_L vs. Temperature

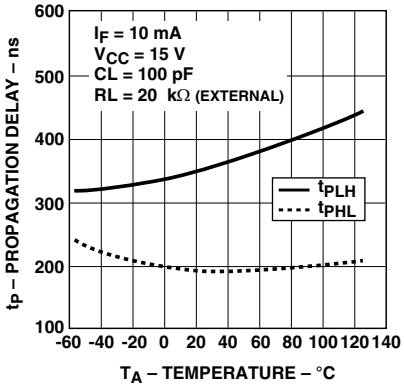


Figure 8 Propagation Delay with Internal 20 kΩ R_L vs. Temperature

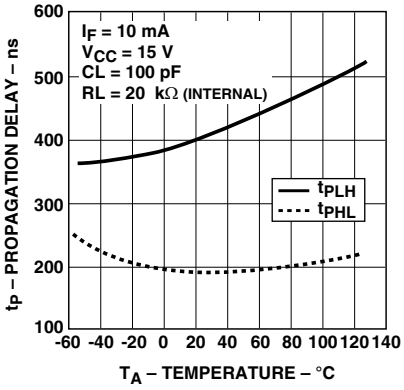


Figure 9 Propagation Delay vs. Load Resistance

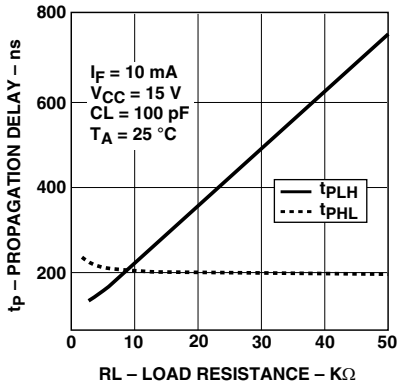


Figure 10 Propagation Delay vs. Load Capacitance

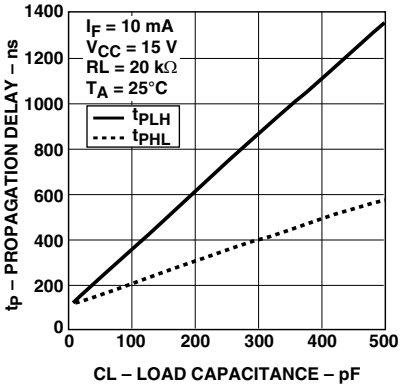


Figure 11 Propagation Delay vs. Supply Voltage

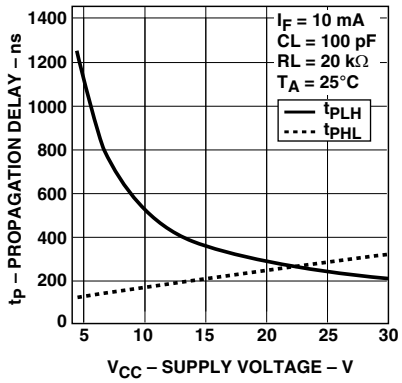


Figure 12 Propagation Delay vs. Input Current

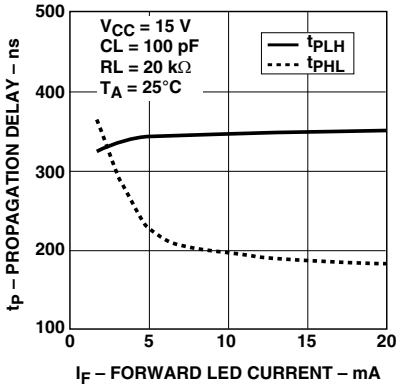


Figure 13 Recommended LED Drive Circuit

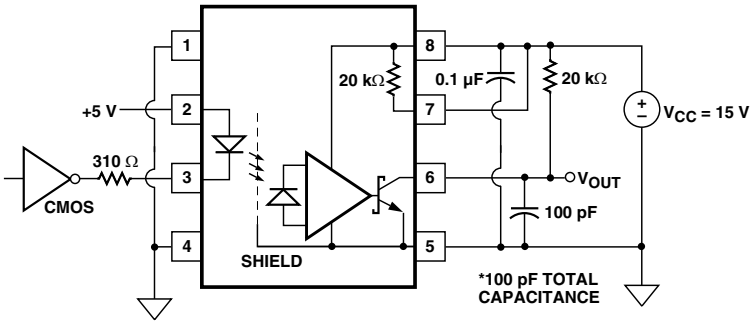


Figure 14 Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers

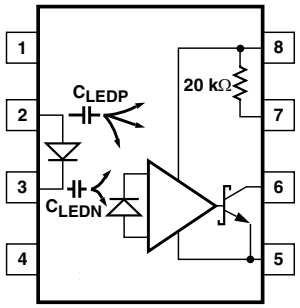


Figure 15 Optocoupler Input to Output Capacitance Model for Shielded Optocouplers

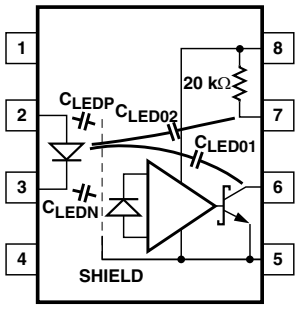


Figure 16 LED Drive Circuit with resistor Connected to LED Anode (not recommended)

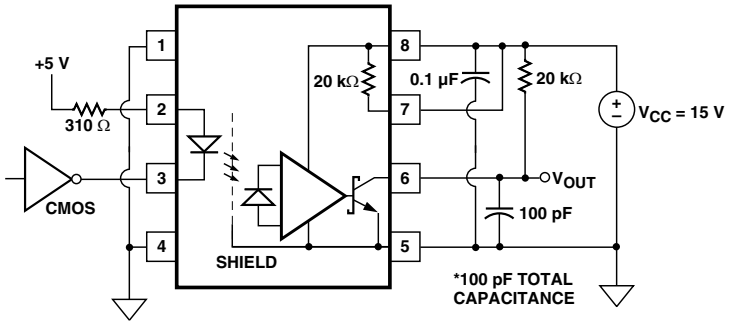


Figure 17 AC Equivalent Circuit for Figure 16 During Common Mode Transients

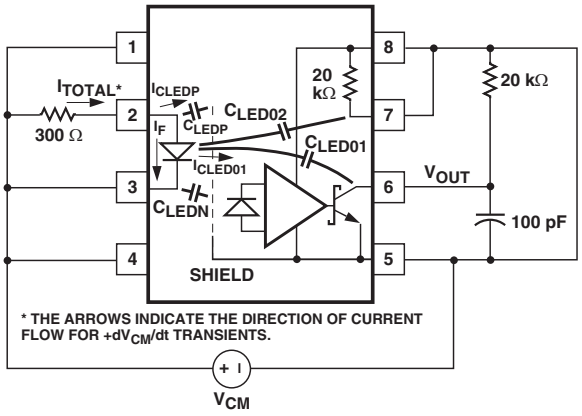


Figure 18 AC Equivalent Circuit for Figure 13 During Common Mode Transients

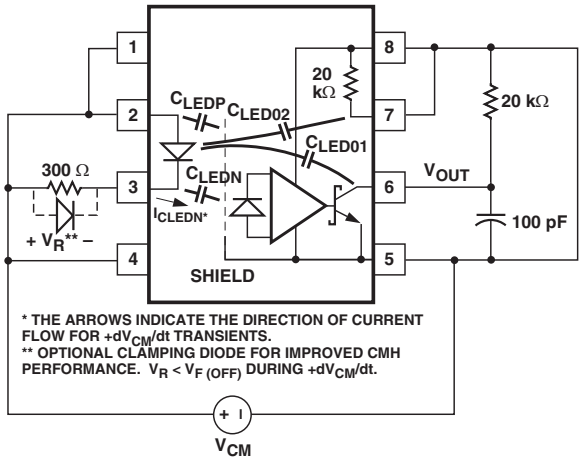


Figure 19 Not Recommended Open Collector LED Drive Circuit

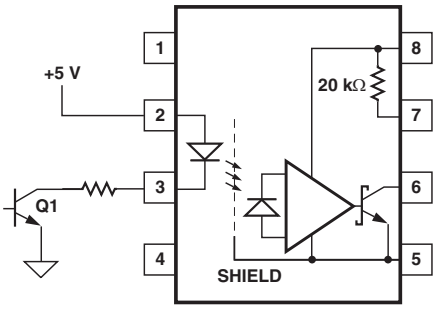


Figure 20 AC Equivalent Circuit for Figure 19 During Common Mode Transients

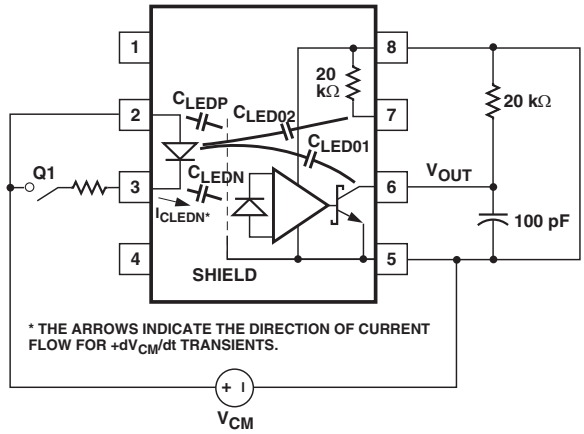


Figure 21 Recommended LED Drive Circuit for Ultra High CMR

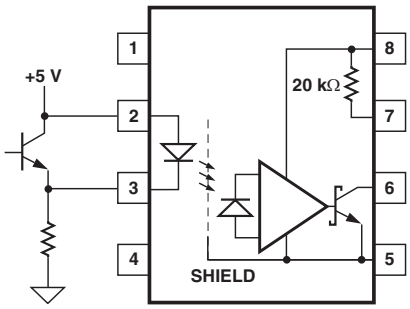


Figure 22 Typical Application Circuit

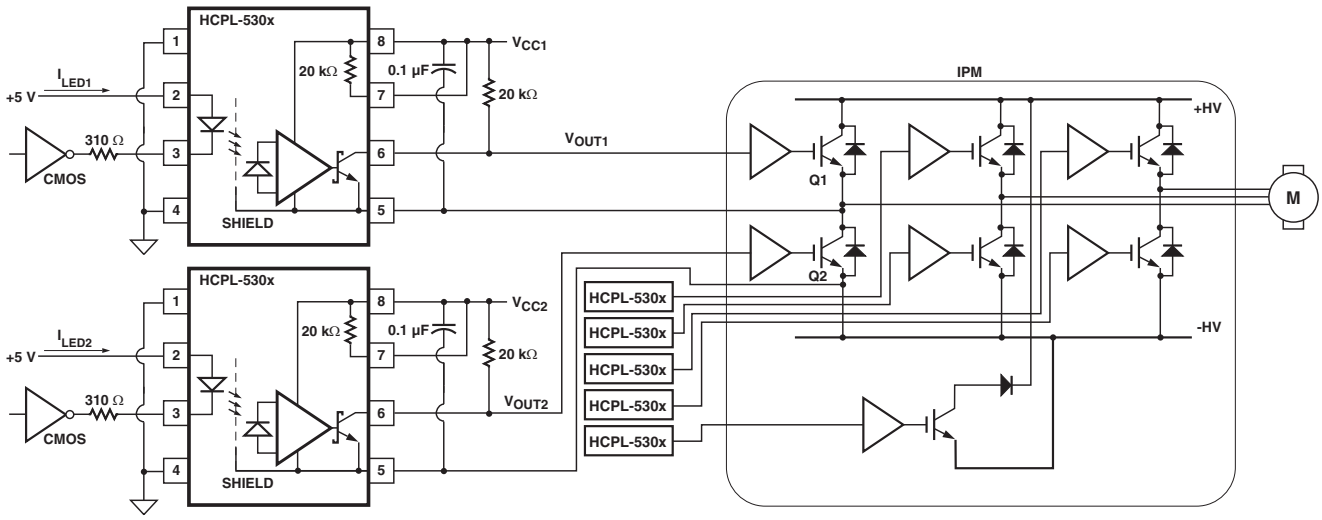
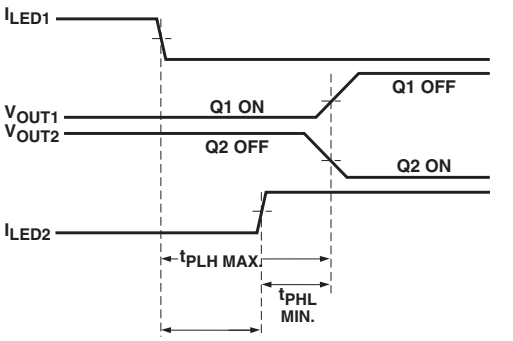


Figure 23 Minimum LED Skew for Zero Dead Time

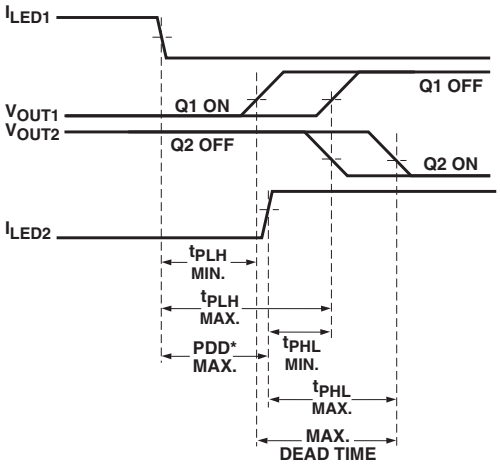


PDD* MAX. =
$(t_{PLH}-t_{PHL})$ MAX. = t_{PLH} MAX. - t_{PHL} MIN.

***PDD = PROPAGATION DELAY DIFFERENCE**

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE PDD ARE TAKEN AT EQUAL TEMPERATURES.

Figure 24 Waveforms for Dead Time Calculations



MAXIMUM DEAD TIME (DUE TO OPTOCOUPLER)

$= (t_{PLH\ MAX.} - t_{PLH\ MIN.}) + (t_{PHL\ MAX.} - t_{PHL\ MIN.})$

$= (t_{PLH\ MAX.} - t_{PHL\ MIN.}) - (t_{PLH\ MIN.} - t_{PHL\ MAX.})$

= PDD* MAX. - PDD* MIN.

*PDD = PROPAGATION DELAY DIFFERENCE

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE THE MAXIMUM DEAD TIME ARE TAKEN AT EQUAL TEMPERATURES.

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