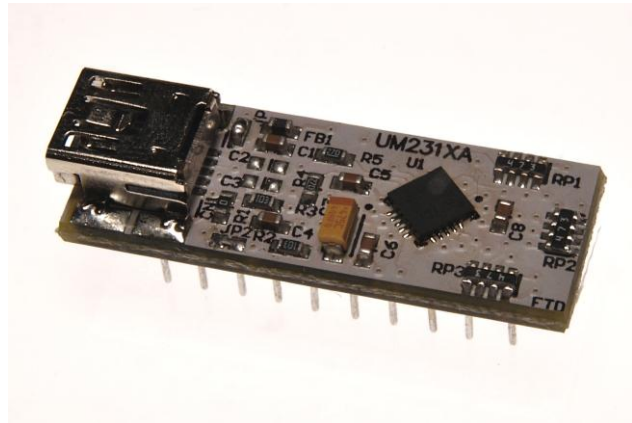


Future Technology Devices International Ltd

Datasheet

UMFT231XA USB to Full- Handshake UART Development Module



UMFT231XA is a USB to serial Full-Handshake UART DIP module with a 0.3" row pitch.

1 Introduction

The UMFT231XA is a development module for FTDI's FT231XQ, one of the devices from FTDI's range of USB interface bridging integrated circuit devices. FT231X is a USB to UART interface with a battery charger detection feature, which can allow batteries to be charged with a higher current from a dedicated charger port (without the FT231X being enumerated). In addition, asynchronous and synchronous bit bang interface modes are available. The internally generated clock (6MHz, 12MHz and 24MHz) can be brought out of the on one of the CBUS pin to be used to drive a microprocessor or external logic.

The UMFT231XA is a module which is designed to plug into a standard 0.3" wide 20 pin DIP socket. All components used, including the FT231XQ are Pb-free (RoHS compliant).

1.1 Features

The UMFT231XA is fitted with a FT231XQ, all the features of the FT231X can be utilized with the UMFT231XA. For a full list of the FT231X's features please see the FT231X datasheet which can be found at the [FTDI website](#). In addition to the features listed in the FT231X datasheet, the UMFT231XA has the following features:

- Small PCB assembly module designed to fit a standard 7.62mm (0.3") wide 20 pin DIP socket. Pins are on a 2.54mm (0.1") pitch.
- On board USB 'mini-B' socket allows module to be connected to a PC via a standard A to mini-B USB cable.
- Functionally configurable using solder links. The default solder links setup enables the module to function without peripheral wires or application board. Other configurations enable external power supply options and variation of logic reference levels.



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2 Driver Support

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for:

- Windows 7 32,64-bit
- Windows Vista
- Windows XP 32,64-bit
- Windows XP Embedded
- Windows CE.NET 4.2 , 5.0 and 6.0
- MAC OS OS-X
- Linux 3.0 and greater
- Android

Royalty-Free D2XX Direct Drivers (USB Drivers + DLL S/W Interface):

- Windows 7 32,64-bit
- Windows Vista
- Windows XP 32,64-bit
- Windows XP Embedded
- Windows CE.NET 4.2, 5.0 and 6.0
- MAC OS OS-X
- Linux 3.0 and greater
- Android

The drivers listed above are all available to download for free from www.ftdichip.com. Various 3rd Party Drivers are also available for various other operating systems - visit www.ftdichip.com for details.

3 Ordering Information & TID

Module Code	Utilised IC Code	TID	Description
UMFT201XA-01	FT201XQ	10006629	USB to I ² C evaluation module.
UMFT220XA-01	FT220XQ	10006630	USB to 4-bit SPI/FT1248 evaluation module.
UMFT221XA-01	FT221XQ	10006631	USB to 8-bit SPI/FT1248 evaluation module.
UMFT230XA-01	FT230XQ	10006632	USB to Basic UART evaluation module.
<u>UMFT231XA-01</u>	FT231XQ	<u>10006633</u>	<u>USB to Full-Handshake UART evaluation module. Pin length: 5.6mm. Rev B silicon.</u>
<u>UMFT231XA-02</u>	FT231XQ	<u>TBC</u>	<u>USB to Full-Handshake UART evaluation module. Pin length: 4.6mm. Rev C silicon. Available at a later date.</u>
UMFT240XA-01	FT240XQ	10006634	USB to 8-bit 245 FIFO evaluation module.

TID is the test identification code.

4 UMFT231XA Signals and Configurations

4.1 UMFT231XA Pin Out

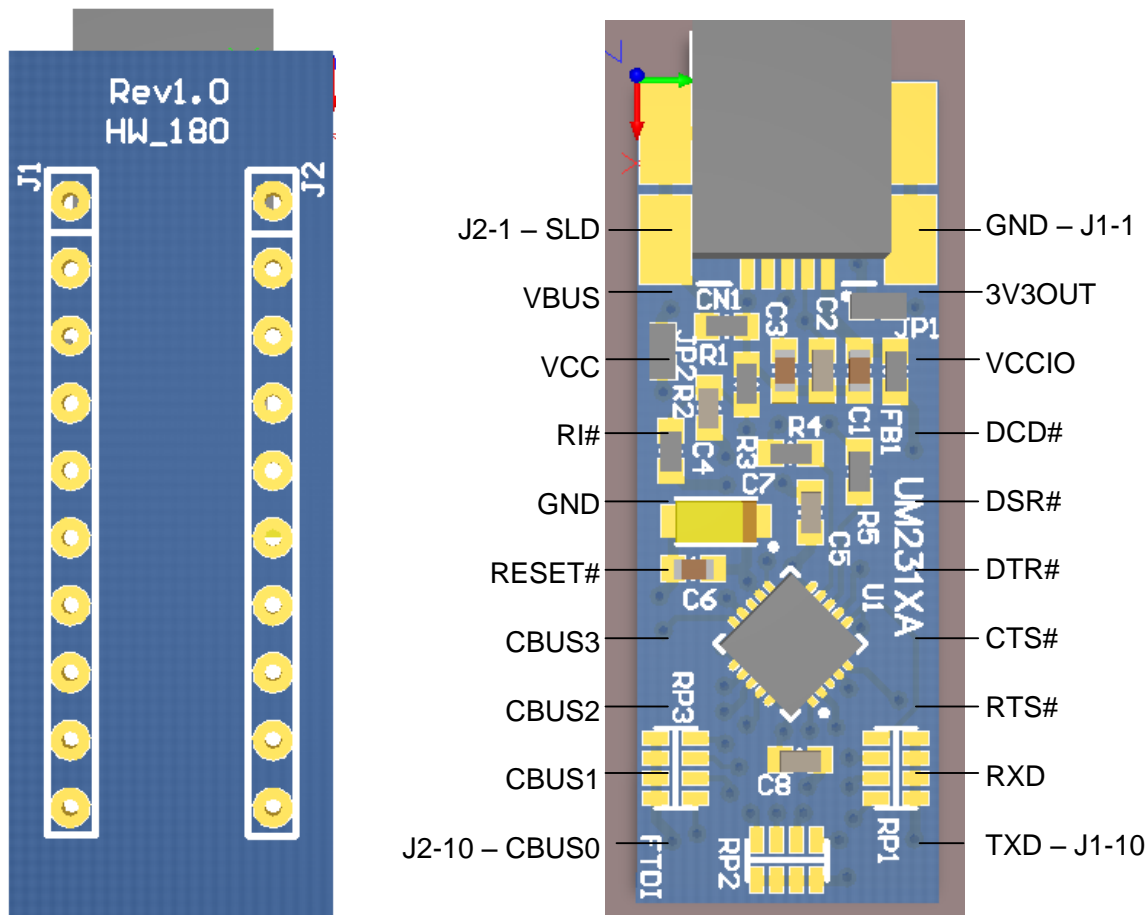


Figure 4.1 – Module Pin Out

Figure 4.1 illustrates the signals available on the DIL pins. The LHS shows the pinout when the module is viewed from the bottom. The RHS shows what signals are available (on the pins below) when viewed from the top. The pins do not go completely through the PCB.

4.2 Signal Descriptions

Pin No.	Name	Type	Description
J1-1, J2-5	GND	PWR	Module Ground Supply Pins
J1-2	3V3OUT	Power Input/ Output	3.3V output from integrated L.D.O. regulator. This pin is decoupled with a 100nF capacitor to ground on the PCB module. The prime purpose of this pin is to provide the 3.3V supply that can be used internally. For power supply configuration details see section 5.
J1-3	VCCIO	Power Input	+1.8V to +3.3V supply to the UART Interface and CBUS I/O pins. For power supply configuration details see section 5.
J1-4	DCD#	Input	Data Carrier Detect Control Input.
J1-5	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
J1-6	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
J1-7	CTS#	Input	Clear To Send Control Input / Handshake Signal.
J1-8	RTS#	Output	Request to Send Control Output / Handshake Signal.
J1-9	RXD	Input	Receiving Asynchronous Data Input.
J1-10	TXD	Output	Transmit Asynchronous Data Output.
J2-1	SLD	GND	USB Cable Shield. Connected to GND via a 0ohm resistor.
J2-2	VBUS	Power Output	5V Power output from the USB bus. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply and applied to the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design. Currents up to 1A can be sourced from a dedicated charger and applied to the USB bus.
J2-3	VCC	Power Input	5V power input for FT231X. For power supply configuration details see section 5.
J2-4	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal MTP ROM taking RI# low >20ms can be used to resume the PC USB host controller from suspend.
J2-6	RESET#	Input	FT231X active low reset line. Configured with an on board pull-up and recommended filter capacitor. When no power is applied to the USB bus reset, will be held low, this prevents current from flowing to the host or hub when in self-powered mode.
J2-7	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal MTP ROM. Factory Default pin Function is SLEEP#. See CBUS Signal Options, Table 4.2.
J2-8	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal MTP ROM. Factory Default pin function is TXLED. See CBUS Signal Options, Table 4.2.
J2-9	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal MTP ROM. Factory Default pin Function is RXLED#. See CBUS Signal Options, Table 4.2.
J2-10	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal MTP ROM. Factory Default pin Function is TXDED. See CBUS Signal Options, Table 4.2.

Table 4.1 – Module Pin Out Description

4.3 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. These options are all configured in the internal MTP ROM using the utility software FT_PROG, which can be downloaded from the www.ftdichip.com. The default configuration is described in [Section 9](#).

CBUS Signal Option	Available On CBUS Pin	Description
Tristate	CBUS0-CBUS3	IO Pad is tristated
DRIVE_1	CBUS0-CBUS3	Output a constant 1
DRIVE_0	CBUS0-CBUS3	Output a constant 0
TXDEN	CBUS0-CBUS3	Enable transmit data for RS485
PWREN#	CBUS0-CBUS3	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. NOTE: This function is driven by an open-drain to ground with no internal pull-up, this is specially designed to aid battery charging applications. UMFT231XA connects an external 47K pull-up.
TXLED#	CBUS0-CBUS3	Transmit data LED drive – open drain pulses low when transmitting data via USB.
RXLED#	CBUS0-CBUS3	Receive data LED drive – open drain pulses low when receiving data via USB.
TX&RXLED#	CBUS0-CBUS3	LED drive – open drain pulses low when transmitting or receiving data via USB.
SLEEP#	CBUS0-CBUS3	Goes low during USB suspend mode. Typically used to power down an external logic to RS232 level converter IC in USB to RS232 converter designs. Cancel SLEEP# option for when connected to a dedicated charger port, this can be selected when configuring the MTP ROM. When this option is enabled SLEEP# is driven high when FT231X is connected to a Dedicated Charger Port.
CLK24MHz	CBUS0-CBUS3	24 MHz Clock output.**
CLK12MHz	CBUS0-CBUS3	12 MHz Clock output.**
CLK6MHz	CBUS0-CBUS3	6 MHz Clock output.**
GPIO	CBUS0-CBUS3	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal MTP ROM. A separate application note, AN232R-01 , available from FTDI website (www.ftdichip.com) describes in more detail how to use CBUS bit bang mode.
BCD_Charger	CBUS0-CBUS3	Battery Charge Detect indicates when the device is connected to a dedicated battery charger host. Active high output. NOTE: Requires a 10K pull-down to remove power up toggling.
BCD_Charger#	CBUS0-CBUS3	Active low BCD Charger, driven by an open drain to ground with no internal pull-up (4.7K on board pull-up present).
BitBang_WR#	CBUS0-CBUS3	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBang_RD#	CBUS0-CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.
VBUS_Sense	CBUS0-CBUS3	Input to detect when VBUS is present.
Time_Stamp	CBUS0-CBUS3	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS0-CBUS3	Active Low input, prevents the chip from going into suspend.

Table 4.2 – CBUS Signal Options

**When in USB suspend mode the outputs clocks are also suspended.

5 Module Configurations

5.1 Solder Link Configuration Options

Solder Link No.	Setting	Status	Description
JP1	Shorted	Default	Connects internal 3.3V regulator to VCCIO. This restricts signal drive to only 3.3V level signals.
JP1	Opened	Non-Default	Disconnects internal 3.3V regulator connection to VCCIO. This mode allows for the supply of 1.8V-3.3V power from an external power supply, thus allows the processing of signals with logic levels between 1.8V and 3.3V. VCCIO can be adjusted to match the interface requirements of external circuitry.

Table 5.1 – Solder Links JP1 Pin Description

Solder Link No.	Setting	Status	Description
JP2	Shorted	Default	Connects VBUS to VCC. This mode is known as “USB-Powered” mode.
JP2	Opened	Non-Default	Disconnects VBUS to VCC. This allows the supply of power form an external power supply. This mode is known as “Self-Powered” mode.

Table 5.2 – Solder Links JP2 Pin Description

Note: There should never be more than one power output supplied to the same net. Failure to properly remove solder from JP1 and JP2 can cause a direct short between two different power supplies (when a self-powered set-up is applied and the USB bus is connected) resulting in damage to the UMFT231XA module and the target circuit.

5.2 Solder Link Modifications

The UMFT231XA has two solder links fixed to the top side of the PCB. These solder link can be adjusted by removing the solder linking the two PADS to produce an open or by placing a solder bridge to produce a short.

By default the UMFT231XA has both solder links shorting their pads. To allow for enhanced flexibility of this module remove both solder links and wire the header pins according to the power setup required.

5.6 Variable IO Voltage Supply

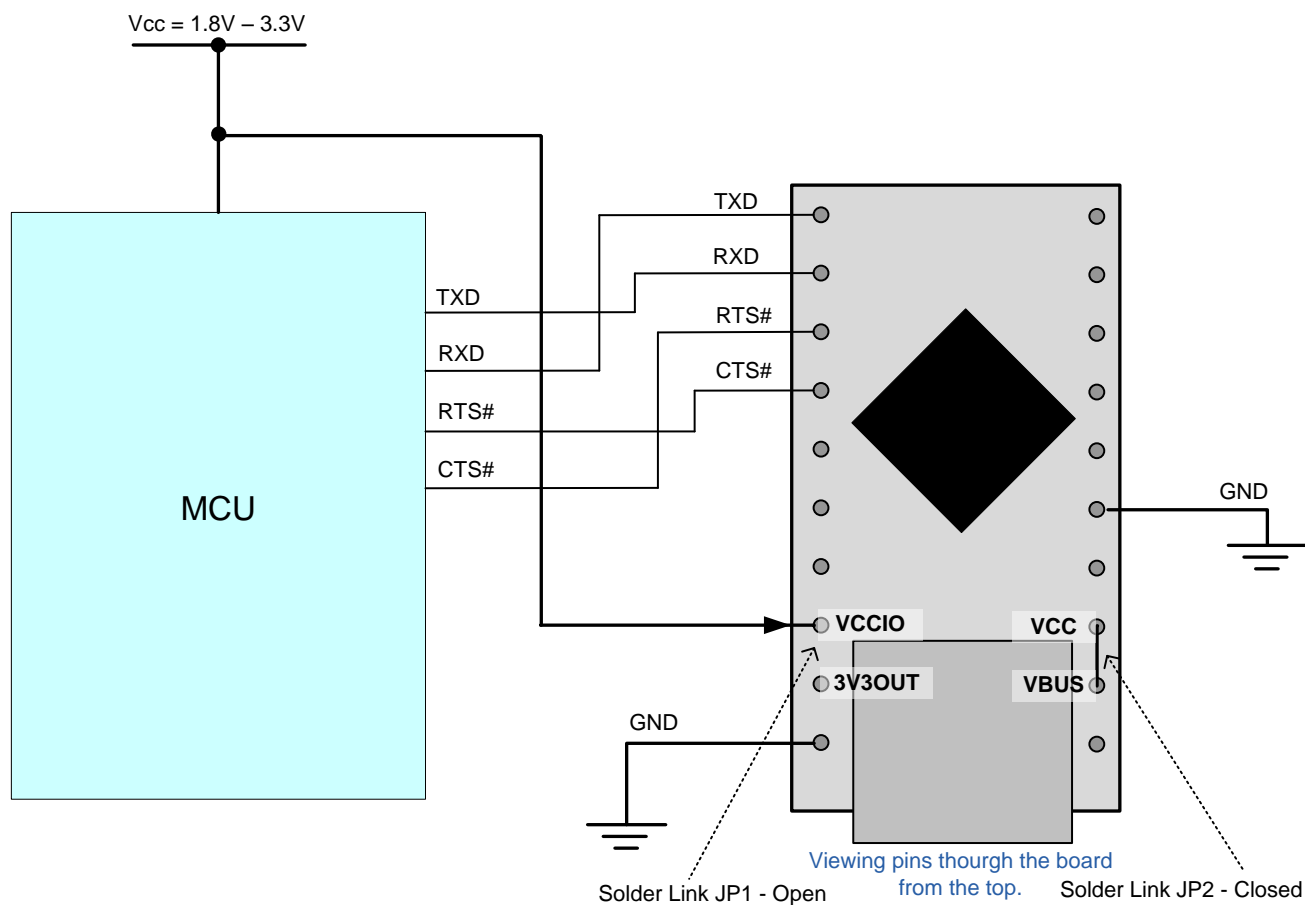


Figure 5.4 – USB Bus Powered 3.3V Logic Drive

The FT231X can process signals at CMOS/TTL logic levels in the range of 1.8V to 3.3V. This section describes how to utilise this feature.

Figure 5.4 shows a configuration where the FT231X is interfaced to a device with IOs operating in the range of 1.8V - 3.3V. The IO ports of this module need to be powered with a voltage level that is equal to the level of the signals it is processing. Since the FT231X's embedded voltage regulator only outputs 3V3 the IO ports will need to be powered from another power source when operating at voltage levels other than 3.3V. (Note that Figure 5.4 is for illustration only and that the pins do not actually go all the way through the PCB)

By default, a short is present between 3V3OUT (embedded voltage regulator) and VCCIO (IO port's power input) by solder links JP1. If an external power supply is used to power the IO ports this solder links needs to be open. This can be done by removing the solder linking the two pads of the solder links.

The configuration described in this section can be implemented in either bus-powered mode or self-powered mode.

Note 1: The CBUS and DBUS pins are 5V tolerant; however these signals cannot drive signals at 5V TTL/CMOS. VCCIO is not 5V tolerant; applying 5V to VCCIO will damage the chip.

Note 2: If power is applied to VCCIO and no power is applied to VCC all IOs will be at an unknown state, this however will not damage the chip. The FT231X also has protective circuitry to prevent the chip being damaged by a voltage discrepancy between VCCIO and the level of the signal being processed.

Note 3: When using VCCIO less than 3V3 on a chip from FTDI's X-chip range, it is recommended to uses pull up resistors (47K) to VCCIO on the data lines, all of the UMFT2xxXA devices include an on-board pull-up for these lines.

5.7 3.3V Voltage Supply

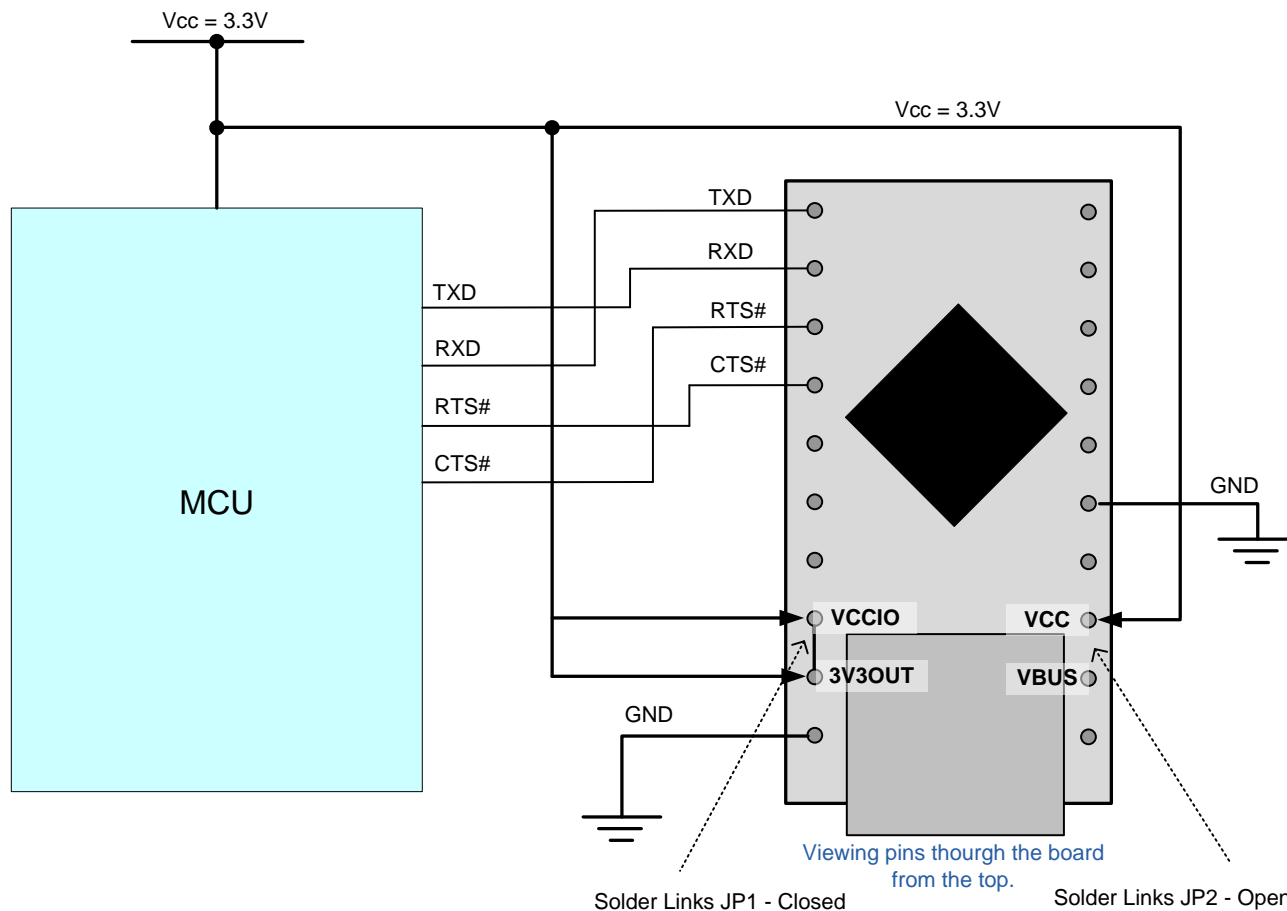


Figure 5.5 – USB Self Powered 3.3V Logic Drive

The FT231X can be powered from a single 3.3V supply. This feature is an alternative to having the FT231X powered at 5V in standard self-powered configuration.

The 3.3V Self Powered configuration is illustrated in Figure 5.5. Note that the 3.3V input is connected to VCC, VCCIO and 3V3OUT. (Note that Figure 5.5 is for illustration only and that the pins do not actually go all the way through the PCB)

5.8 Configuring the MTP ROM

The FT231X contains an embedded MTP ROM. This can be used to configure the functions of each CBUS pin, the current drive on each signal pin, current limit for the USB bus and the other descriptors of the device. For details on using the MTP ROM/EEPROM programming utility FT_PROG, please see the FT_PROG User Guide [and the FT231X datasheet](#).

When programming the MTP ROM please note:

- i) One of the CBUS Pins can be configured as PWREN# in the internal MTP ROM. This can be used to switch the power supply to the external circuitry.
- ii) The Max Bus Power setting of the MTP ROM should specify the maximum current to be drawn from the USB host/hub when enumerated. For high-powered USB devices the current limit when enumerated is between 100mA and 500mA, for low-powered USB devices the current limit is 100mA.

6 Module Dimensions

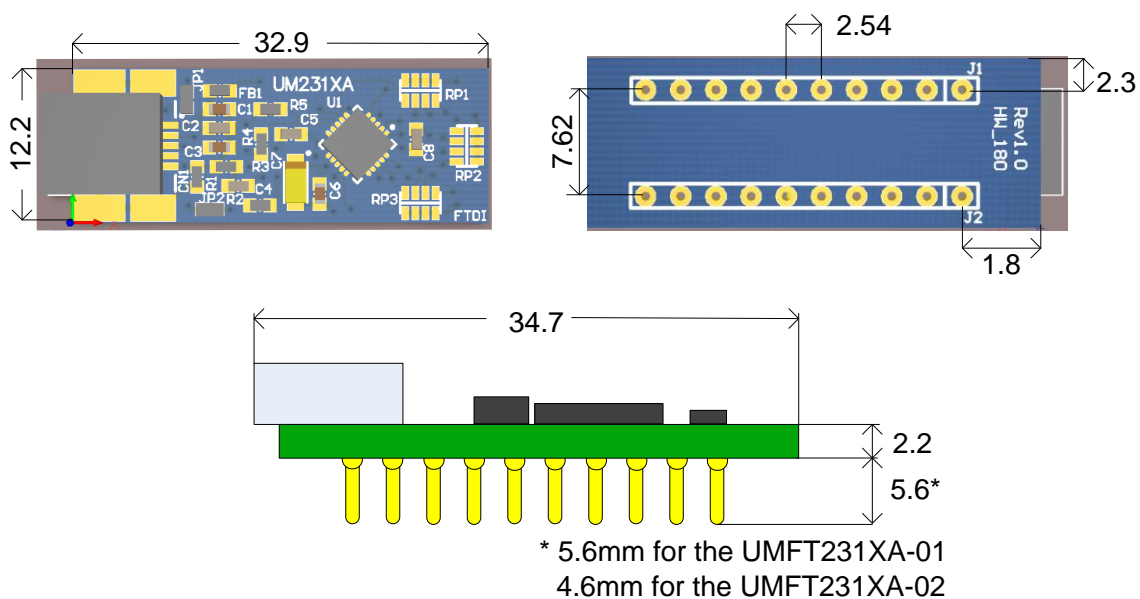


Figure 6.1 – UMFT231XA Module Dimensions

All dimensions are given in millimetres.

The UMFT231XA module exclusively uses lead free components, and is fully compliant with European Union directive 2002/95/EC.

8 Internal MTP ROM Configuration

Following a power-on reset or a USB reset the FT231X will scan its internal MTP ROM and read the USB configuration descriptors stored there. The default values programmed into the internal MTP ROM in the FT231XQ used on the UMFT231XA are shown in Table 8.1.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6015h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the MTP ROM during final test of the UM232R module.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when the power is shut off (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	UMFT231XA	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT231X	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Enabled	Taking RI# low will wake up the USB host controller from suspend.
High Current I/Os	Disabled	Enables the high drive level on the UART and CBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the CVP driver interface for the device.
CBUS0	GPIO	
CBUS1	GPIO	
CBUS2	GPIO	
CBUS3	GPIO	
Invert UART	Disabled	Signal on this pin becomes TXD# if enable.

Table 8.1 – Default Internal MTP ROM Configuration

The internal MTP ROM in the FT231X can be programmed over USB using the utility program FT_PROG. FT_PROG can be downloaded from the www.ftdichip.com. Users who do not have their own USB vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact [FTDI Support](mailto:support1@ftdichip.com) (support1@ftdichip.com) for this service, also see [TN_100](#) and [TN_101](#).

9 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 1103, No. 666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 (0)21 6235 1596
Fax: +86 (0)21 6235 1595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

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Appendix B – Revision History

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Document Feedback: [Send Feedback](#)

Version 1.0	Initial Datasheet Created	09/02/12
Version 1.1	Added links, referances to silicon revision, TID and logos.	12/06/12

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А