

LTM4619EV: 4.5V-28V, Dual 4A Step-Down μ Module Regulator

DESCRIPTION

Demonstration circuit 1453A features the LTM[®]4619EV, the high input voltage, high efficiency, high density, dual 4A step-down power module. Derating is necessary for certain V_{IN} , V_{OUT} , and thermal conditions. The two outputs are interleaved with 180° phase to minimize the input ripple and reduce the input capacitors. A minimum design only requires the bulk input and output capacitors and voltage setting resistors. The LTM4619EV features output voltage tracking, power good indicator, RUN pin control, clock synchronization and soft-start programming. Protection

features include foldback current limiting and overvoltage protection. Burst Mode[®] operation or pulse skipping mode can be selected for better light load efficiency. The LTM4619 data sheet must be read in conjunction with this demo manual for working on or modifying the demo circuit 1453A.

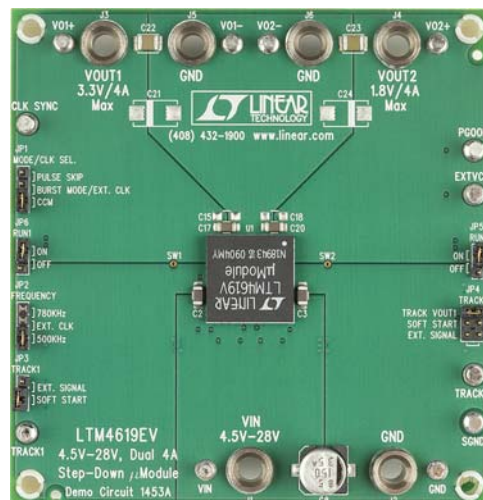
Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY ($T_A = 25^\circ\text{C}$)

PARAMETER	CONDITION	VALUE
Input Voltage Range		4.5V to 28V
Output Voltage V_{OUT1} , V_{OUT2}		3.3V \pm 2%, 1.8V \pm 2%
Maximum Continuous Output Current	Derating Is Necessary for Certain V_{IN} , V_{OUT} , and Thermal Conditions, See Datasheet for Details.	4A _{DC} for V_{OUT1} , V_{OUT2}
Default Operating Frequency	JP2 on the 500kHz position.	500kHz
Efficiency of Channel 1	$V_{IN} = 12\text{V}$, $V_{OUT1} = 3.3\text{V}$, $I_{OUT1} = 4\text{A}$, Switching Frequency = 500kHz.	89.4%, See Figure 3
Efficiency of Channel 2	$V_{IN} = 12\text{V}$, $V_{OUT2} = 1.8\text{V}$, $I_{OUT2} = 4\text{A}$, Switching Frequency = 500kHz.	84.1% See Figure 3

BOARD PHOTO



dc1453af

QUICK START PROCEDURE

Demonstration circuit 1453A is an easy way to evaluate the LTM4619. If V_{IN} is always below 5.5V, stuff a 0Ω resistor at R16. Do not stuff R16 if V_{IN} is higher than 5.5V. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical 3.3V and 1.8V application:

MODE/ CLK SEL.	RUN1	FREQUENCY	TRACK1	RUN2	TRACK2
CCM	On	500kHz	Soft-Start	On	Soft-Start

2. With power off, preset the loads to 0A and V_{IN} supply to be less than 28V. Connect the input power supply, load and meters as shown in Figure 1.

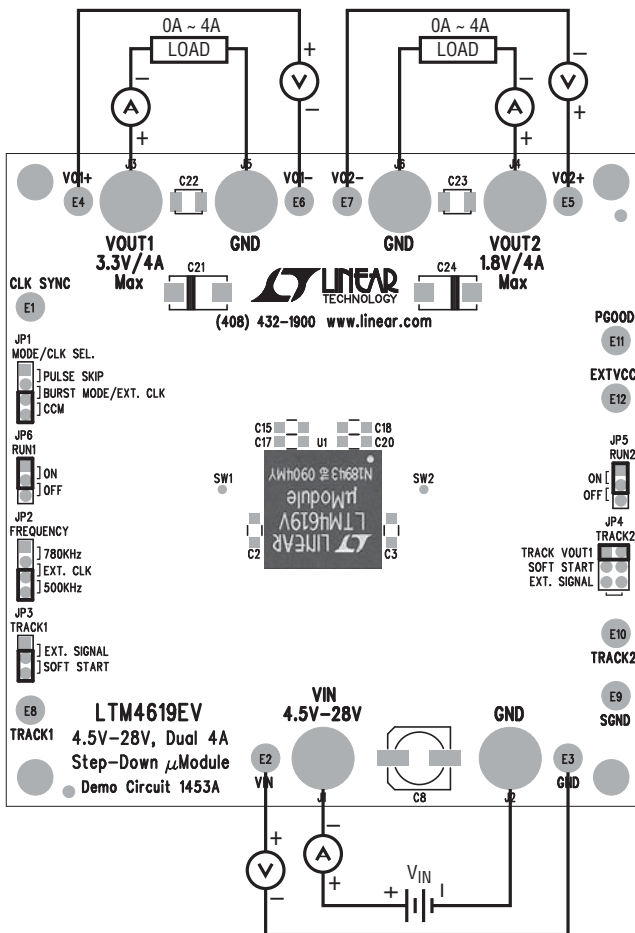


Figure 1. Test Setup of DC1453A

3. Turn on the power at the input. The output voltage between V_{O1}^+ and V_{O1}^- should be $3.3V \pm 2\%$, and the voltage between V_{O2}^+ and V_{O2}^- should be $1.8V \pm 2\%$.
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

To measure input and output ripple, please refer to Figure 2 for proper setup. Keep in mind at high switching frequencies and/or high input voltages, lower output voltage may not regulate properly due to the minimum on time of the regulator. Refer to the data sheet for more details.

5. For output voltage tracking during start-up and shut-down, set jumpers JP3 and JP4 to EXT SIGNAL and apply a valid voltage signal to E8 and E10.
6. To synchronize the switching frequency to an external clock set jumper JP2 in the EXT. CLK position and the jumper JP1 in the BURST MODE / EXT. CLK position. Apply a valid clock signal on the CLK SYNC test point.

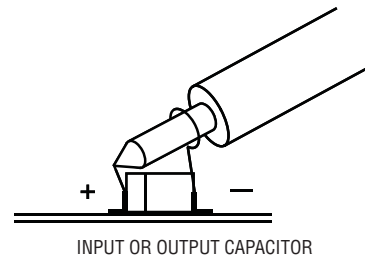
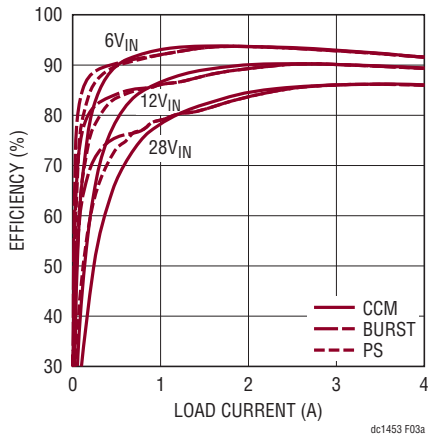


Figure 2. Proper Scope Probe Placement for Measuring Input or Output Ripple

QUICK START PROCEDURE

3.3V V_{OUT1} Efficiency at 500kHz Frequency



1.8V V_{OUT2} Efficiency at 500kHz Frequency

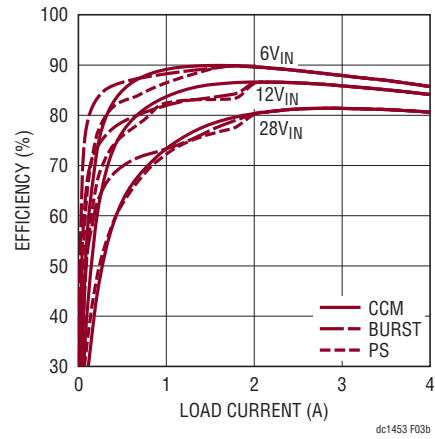
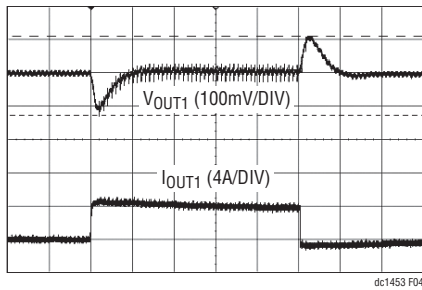
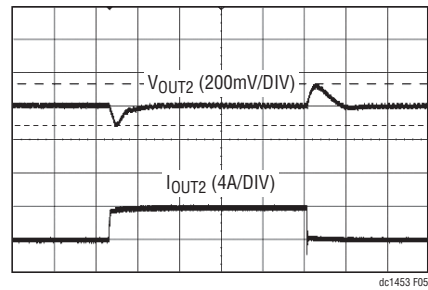


Figure 3. Measured Efficiency for Two Outputs on DC1453A



$V_{IN} = 12V$
 $V_{OUT1} = 3.3V$
 CONTINUOUS CURRENT MODE (CCM)
 0A TO 4A LOAD STEP ON V_{OUT1}
 $C_{OUT1} = 100\mu F$ CERAMIC (1210, X5R, 6.3V) +
 $22\mu F$ CERAMIC (1206, X5R, 6.3V)

Figure 4. Measured Load Transient Response for V_{OUT1}



$V_{IN} = 12V$
 $V_{OUT2} = 1.8V$
 CONTINUOUS CURRENT MODE (CCM)
 0A TO 4A LOAD STEP ON V_{OUT2}
 $C_{OUT2} = 100\mu F$ CERAMIC (1210, X5R, 6.3V) +
 $22\mu F$ CERAMIC (1206, X5R, 6.3V)

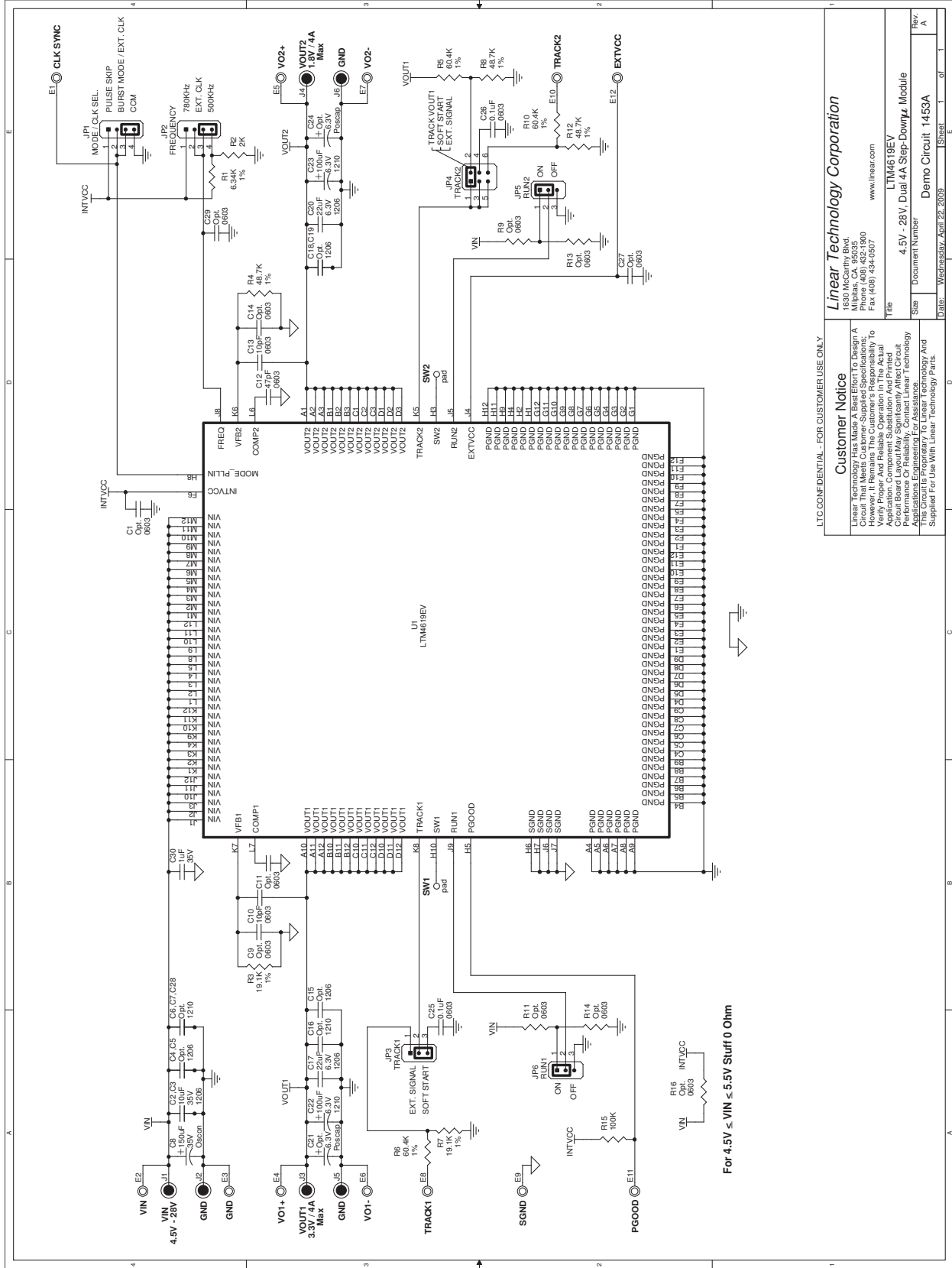
Figure 5. Measured Load Transient Response for V_{OUT2}

DEMO MANUAL DC1453A

PARTS LIST

ITEM	QUANTITY	REFERENCE	PART DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components:				
1	1	C8	Capacitor, Alum, 150µF, 35V	Sanyo, 35CE150AX
2	2	C2, C3	Capacitor, X5R, 10µF, 35V, 1206	Taiyo Yuden, GMK316BJ106MA-T
3	2	C17, C20	Capacitor, X5R, 22µF, 6.3V, 1206	Taiyo Yuden, JMK316BJ226ML-T
4	2	C22, C23	Capacitor, X5R, 100µF, 6.3V, 1210	Taiyo Yuden, JMK325BJ107MM-T
5	2	C10, C13	Capacitor, NPO, 10pF, 50V, 0603	AVX, 06035A100KAT2A
6	1	C12	Capacitor, NPO, 47pF, 50V, 0603	AVX, 06035A470KAT2A
7	2	C25, C26	Capacitor, X7R, 0.1µF, 50V, 0603	TDK, C1608X7R1H104K
8	1	R2	Resistor, Chip, 2k, 1/10W, 5%	Vishay, CRCW06032K00JKEA
9	1	R1	Resistor, Chip, 6.34k, 1/10W, 1%	Vishay, CRCW06036K34FKEA
10	1	R3	Resistor, Chip, 19.1k, 1/10W, 1%	Vishay, CRCW060319K1FKEA
11	1	R15	Resistor, Chip, 100k, 1/10W, 5%	Vishay, CRCW0603100KJNEA
12	1	R4	Resistor, Chip, 48.7k, 1/10W, 1%	Vishay, CRCW060348K7FKEA
13	1	U1	I.C., Dual 4A Step-Down Module	Linear, Technology LTM4619EV LGA
Additional Demo Board Circuit Components:				
1	1	C30	Capacitor, X5R, 1µF, 35V, 0603	Taiyo Yuden, GMK107BJ105KA-T
2	0	C1, C4-C7, C9, C11, C12, C14, C16-C18, C19, C21, C24, C27-C29	OPT	OPT
3	1	R7	Resistor, Chip, 19.1k, 1/10W, 1%	Vishay, CRCW060319K1FKEA
4	3	R5, R6, R10	Resistor, Chip, 60.4k, 1/10W, 1%	Vishay, CRCW060360K4FKEA
5	2	R8, R12	Resistor, Chip, 48.7k, 1/10W, 1%	Vishay, CRCW060348K7FKEA
6	0	R9, R11, R13, R14, R16	OPT	OPT
Hardware for Demo Board Only:				
1	12	E1-E12	Testpoint, Turret, 0.094"	Mill-Max, 2501-2-00-80-00-00-07-0
2	4	4 Corners	Stand-Off, Nylon, 0.5"	Keystone, 8833 (SNAP ON)
3	3	JP3, JP5, JP6	Header, 3-Pin, 1-Row, 0.079CC	Samtec, TMM-103-02-L-S
4	2	JP1, JP2	Header, 4-Pin, 1-Row, 0.079CC	Samtec, TMM-104-02-L-S
5	1	JP4	Header, 3-Pin, 2-Row, 0.079CC	Samtec, TMM-103-02-L-D
6	6	JP1-JP6	Shunt, 0.079" Center	Samtec, 2SN-BK-G
7	6	J1-J6	Banana Jack	Keystone, 575-4

SCHEMATIC DIAGRAM



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DEMO MANUAL DC1453A

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