

# NB6N239S

## 3.3 V, 3.0 GHz Any Differential Clock IN to LVDS OUT $\div 1/2/4/8$ , $\div 2/4/8/16$ Clock Divider



ON Semiconductor®

<http://onsemi.com>

### Description

The NB6N239S is a high-speed, low skew clock divider with two divider circuits, each having selectable clock divide ratios;  $\div 1/2/4/8$  and  $\div 2/4/8/16$ . Both divider circuits drive LVDS compatible outputs. (More device information on page 7). The NB6N239S is a member of the ECLinPS MAX™ family of high performance clock products.

### Features

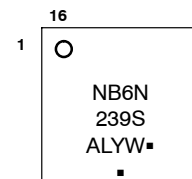
- Maximum Clock Input Frequency, 3.0 GHz (1.5 GHz with  $\div 1$ )
- Input Compatibility with LVDS/LVPECL/CML/HSTL
- Rise/Fall Time 120 ps Typical
- < 5 ps Typical Within Device Output Skew
- Example; 622.08 MHz Input Generates 38.88 MHz to 622.08 MHz Outputs
- Internal 50  $\Omega$  Termination Provided
- Random Clock Jitter < 2 ps RMS
- QA  $\div 1$  Edge Aligned to QB  $\div n$  Edge
- Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.465\text{ V}$  with  $GND = 0\text{ V}$
- Master Reset for Synchronization of Multiple Chips
- $V_{BBAC}$  Reference Output
- Synchronous Output Enable/Disable
- TIA/EIA – 644 Compliant
- Pb-Free Packages are Available



Bottom View

QFN-16  
MN SUFFIX  
CASE 485G

### MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

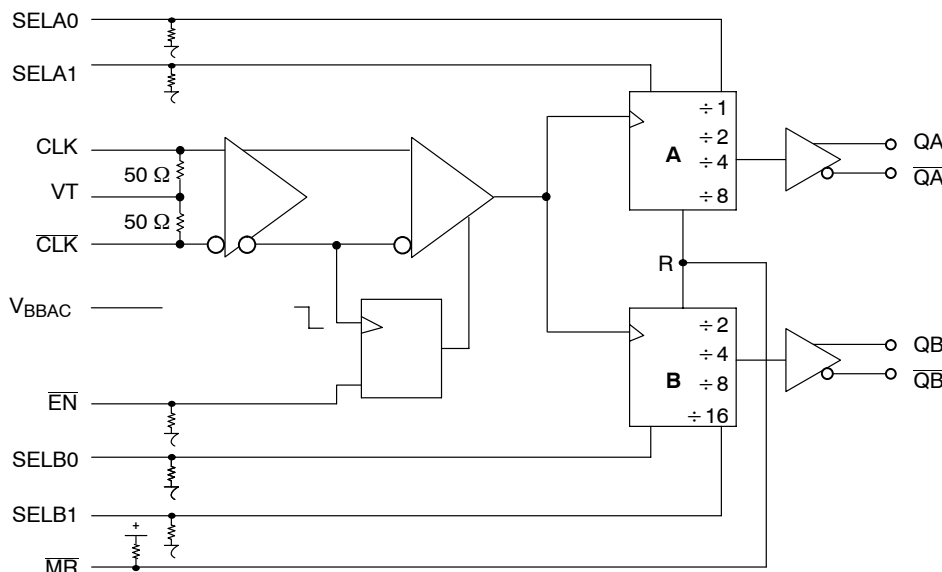


Figure 1. Simplified Logic Diagram

# NB6N239S

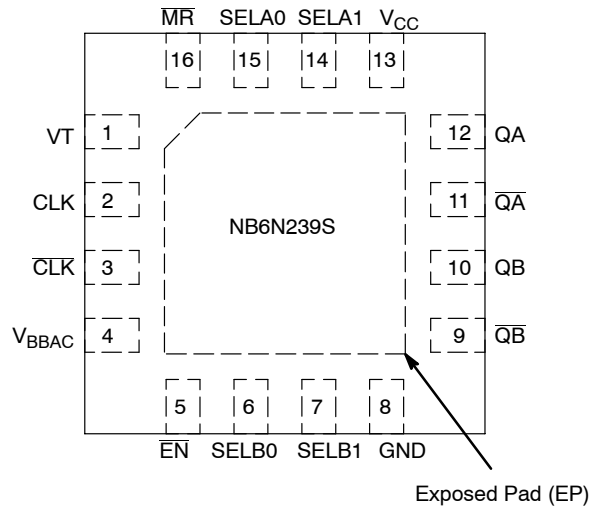


Figure 2. Pinout: QFN-16 (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name                      | I/O                           | Description   |
|-----|---------------------------|-------------------------------|---|
| 1   | VT                        |                               | Internal 100 $\Omega$ Center-Tapped Termination Pin for CLK and $\overline{\text{CLK}}$ .   |
| 2   | CLK                       | LVDS, LVPECL, CML, HSTL Input | Noninverted Differential CLOCK Input.   |
| 3   | $\overline{\text{CLK}}$   | LVDS, LVPECL, CML, HSTL Input | Inverted Differential CLOCK Input.  |
| 4   | $V_{\text{BBAC}}$         |                               | Output Voltage Reference for Capacitor Coupled Inputs, only.  |
| 5   | EN*                       | LVC MOS/LVTTL Input           | Synchronous Output Enable   |
| 6   | SELB0*                    | LVC MOS/LVTTL Input           | Clock Divide Select Pin   |
| 7   | SELB1*                    | LVC MOS/LVTTL Input           | Clock Divide Select Pin   |
| 8   | GND                       | Power Supply                  | Negative Supply Voltage   |
| 9   | $\overline{\text{QB}}$    | LVDS Output                   | Inverted Differential Output. Typically terminated with 100 $\Omega$ across differential outputs.   |
| 10  | QB                        | LVDS Output                   | Noninverted Differential Output. Typically terminated with 100 $\Omega$ across differential outputs.  |
| 11  | $\overline{\text{QA}}$    | LVDS Output                   | Inverted Differential Output. Typically terminated with 100 $\Omega$ across differential outputs.   |
| 12  | QA                        | LVDS Output                   | Noninverted Differential Output. Typically terminated with 100 $\Omega$ across differential outputs.  |
| 13  | $V_{\text{CC}}$           | Power Supply                  | Positive Supply Voltage.  |
| 14  | SELA1*                    | LVC MOS/LVTTL Input           | Clock Divide Select Pin   |
| 15  | SELA0*                    | LVC MOS/LVTTL Input           | Clock Divide Select Pin   |
| 16  | $\overline{\text{MR}}$ ** | LVC MOS/LVTTL Input           | Master Reset Asynchronous, Default Open High, Asserted LOW  |
|     | EP                        | Power Supply (OPT)            | The Exposed Pad on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board. |

\*Pins will default LOW when left OPEN.

\*\*Pins will default HIGH when left OPEN.

# NB6N239S

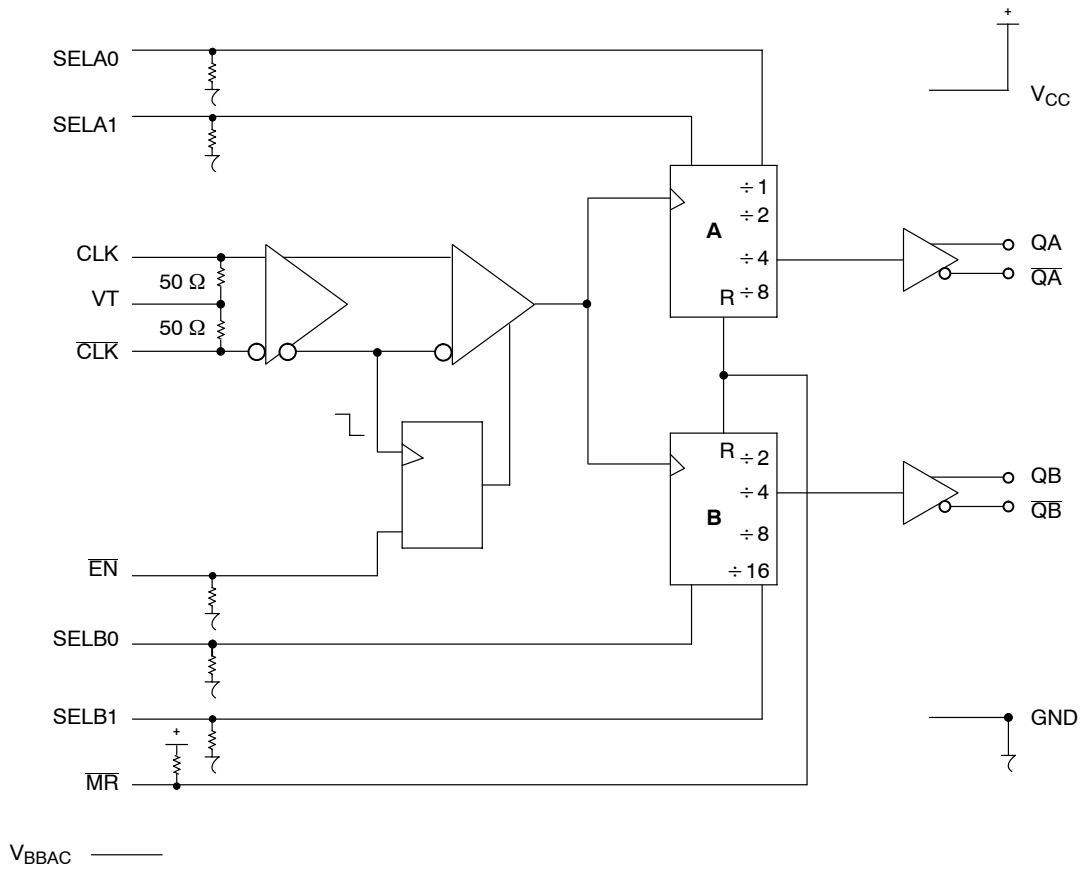


Figure 3. Logic Diagram

Table 2. FUNCTION TABLE

| CLK | EN* | MR** | FUNCTION |
|-----|-----|------|----------|
| ⌋   | L   | H    | Divide   |
| ⌋   | H   | H    | Hold Q   |
| X   | X   | L    | Reset Q  |

Table 3. CLOCK DIVIDE SELECT, QA OUTPUTS

| SELA1* | SELA0* | QA Outputs  |
|--------|--------|-------------|
| L      | L      | Divide by 1 |
| L      | H      | Divide by 2 |
| H      | L      | Divide by 4 |
| H      | H      | Divide by 8 |

Table 4. CLOCK DIVIDE SELECT, QB OUTPUTS

| SELB1* | SELB0* | QB Outputs   |
|--------|--------|--------------|
| L      | L      | Divide by 2  |
| L      | H      | Divide by 4  |
| H      | L      | Divide by 8  |
| H      | H      | Divide by 16 |

⌋ = Low-to-High Transition

⌋ = High-to-Low Transition

X = Don't Care

\*Pins will default LOW when left OPEN.

\*\*Pins will default HIGH when left OPEN.

# NB6N239S

**Table 5. ATTRIBUTES**

| Characteristics   |                        | Value                |             |
|---|------------------------|----------------------|-------------|
| Internal Input Pulldown Resistor                              |                        | 75 k $\Omega$        |             |
| Internal Input Pullup Resistor                                |                        | 75 k $\Omega$        |             |
| ESD Protection  | Human Body Model       | > 1500 V             |             |
|   | Machine Model          | > 100 V              |             |
|   | Charged Device Model   | > 1000 V             |             |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) |                        | Pb Pkg               | Pb-Free Pkg |
| QFN-16  |                        | Level 1              | Level 1     |
| Flammability Rating   | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |             |
| Transistor Count  |                        | 370                  |             |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                        |                      |             |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

**Table 6. MAXIMUM RATINGS**

| Symbol            | Parameter  | Condition 1    | Condition 2                                      | Rating      | Unit           |
|-------------------|--|----------------|--|-------------|----------------|
| V <sub>CC</sub>   | Positive Mode Power Supply   | GND = 0 V      |  | 3.6         | V              |
| V <sub>I</sub>    | Input Voltage  | GND = 0 V      | GND $\leq$ V <sub>I</sub> $\leq$ V <sub>CC</sub> | 3.6         | V              |
| I <sub>SC</sub>   | Output Short Circuit Current<br>Line-to-Line<br>Line-to-GND<br>TIA/EIA - 644 Compliant |                |  | 12          | mA<br>mA       |
|                   |  |                |  | 24          |                |
| I <sub>BBAC</sub> | V <sub>BBAC</sub> Sink/Source Current  |                |  | $\pm$ 0.5   | mA             |
| T <sub>A</sub>    | Operating Temperature Range  |                |  | -40 to +85  | $^{\circ}$ C   |
| T <sub>stg</sub>  | Storage Temperature Range  |                |  | -65 to +150 | $^{\circ}$ C   |
| $\theta_{JA}$     | Thermal Resistance (Junction-to-Ambient)   | 0 lfp/m        |  | 41.6        | $^{\circ}$ C/W |
|                   |  | 500 lfp/m      |  | 35.2        | $^{\circ}$ C/W |
| $\theta_{JC}$     | Thermal Resistance (Junction-to-Case)  | Standard Board |  | 4.0         | $^{\circ}$ C/W |
| T <sub>sol</sub>  | Wave Solder  | Pb             |  | 265         | $^{\circ}$ C   |
|                   |  | Pb-Free        |  | 265         |                |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# NB6N239S

**Table 7. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS**

( $V_{CC} = 3.0\text{ V to }3.465\text{ V}$ ,  $GND = 0\text{ V}$ )

| Symbol          | Characteristic                                 | -40°C |     |      | 25°C |     |      | 85°C |     |      | Unit |
|-----------------|--|-------|-----|------|------|-----|------|------|-----|------|------|
|                 |  | Min   | Typ | Max  | Min  | Typ | Max  | Min  | Typ | Max  |      |
| $I_{CC}$        | Power Supply Current (Inputs and Outputs OPEN) |       |     |      | 35   | 45  | 55   |      |     |      | mA   |
| $V_{OH}$        | Output HIGH Voltage (Notes 2)                  |       |     | 1600 |      |     | 1600 |      |     | 1600 | mV   |
| $V_{OL}$        | Output LOW Voltage (Notes 2)                   | 900   |     |      | 900  |     |      | 900  |     |      | mV   |
| $V_{OD}$        | Differential Output Voltage (Figure 21)        | 250   |     | 450  | 250  |     | 450  | 250  |     | 450  | mV   |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change                      | 0     |     | 50   | 0    |     | 50   | 0    |     | 50   | mV   |
| $V_{OS}$        | Offset Voltage (Figure 21)                     | 1125  |     | 1375 | 1125 |     | 1375 | 1125 |     | 1375 | mV   |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change                      | 0     |     | 50   | 0    |     | 50   | 0    |     | 50   | mV   |

**DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED** (Figures 7, 10)

|            |  |                         |                         |                         |                         |                         |                         |                         |                         |                         |    |
|------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|----|
| $V_{th}$   | Input Threshold Reference Voltage (Note 3)                                       | 100                     |                         | $V_{CC} - 100$          | 100                     |                         | $V_{CC} - 100$          | 100                     |                         | $V_{CC} - 100$          | mV |
| $V_{IH}$   | Single-ended Input HIGH Voltage  | $V_{th} + 100$          |                         | $V_{CC}$                | $V_{th} + 100$          |                         | $V_{CC}$                | $V_{th} + 100$          |                         | $V_{CC}$                | mV |
| $V_{IL}$   | Single-ended Input LOW Voltage   | GND                     |                         | $V_{th} - 100$          | GND                     |                         | $V_{th} - 100$          | GND                     |                         | $V_{th} - 100$          | mV |
| $V_{BBAC}$ | Output Voltage Reference @ 100 $\mu\text{A}$ (Note 6)<br>$V_{CC} = 3.3\text{ V}$ | $V_{CC} - 1460$<br>1840 | $V_{CC} - 1330$<br>1970 | $V_{CC} - 1200$<br>2100 | $V_{CC} - 1460$<br>1840 | $V_{CC} - 1340$<br>1960 | $V_{CC} - 1200$<br>2100 | $V_{CC} - 1460$<br>1840 | $V_{CC} - 1350$<br>1950 | $V_{CC} - 1200$<br>2100 | mV |

**DIFFERENTIAL INPUT DRIVEN DIFFERENTIALLY** (Figures 8, 9, 11) (Note 5)

|           |  |     |    |                |     |    |                |     |    |                |          |
|-----------|--|-----|----|----------------|-----|----|----------------|-----|----|----------------|----------|
| $V_{IHD}$ | Differential Input HIGH Voltage  | 100 |    | $V_{CC}$       | 100 |    | $V_{CC}$       | 100 |    | $V_{CC}$       | mV       |
| $V_{ILD}$ | Differential Input LOW Voltage   | GND |    | $V_{CC} - 100$ | GND |    | $V_{CC} - 100$ | GND |    | $V_{CC} - 100$ | mV       |
| $V_{CMR}$ | Input Common Mode Range (Differential Cross-point Voltage) (Note 4)                                | 50  |    | $V_{CC} - 50$  | 50  |    | $V_{CC} - 50$  | 50  |    | $V_{CC} - 50$  | mV       |
| $V_{ID}$  | Differential Input Voltage ( $V_{IHD(CLK)} - V_{ILD(CLK)}$ ) and ( $V_{IHD(CLK)} - V_{ILD(CLK)}$ ) | 100 |    | $V_{CC} - GND$ | 100 |    | $V_{CC} - GND$ | 100 |    | $V_{CC} - GND$ | mV       |
| $R_{TIN}$ | Internal Input Termination Resistor  | 45  | 50 | 55             | 45  | 50 | 55             | 45  | 50 | 55             | $\Omega$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Outputs loaded with 100  $\Omega$  across LVDS outputs.
3.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.
4.  $V_{CMR_{MIN}}$  varies 1:1 with GND,  $V_{CMR_{MAX}}$  varies 1:1 with  $V_{CC}$ .
5. Input and output voltage swing is a single-ended measurement operating in differential mode.
6.  $V_{BBAC}$  used to rebias capacitor-coupled inputs only (see Figures 16 and 17).

# NB6N239S

**Table 8. DC CHARACTERISTICS, LVTTTL/LVCMOS INPUTS** ( $V_{CC} = 3.0\text{ V to }3.465\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

| Symbol   | Characteristic                     | Min  | Typ | Max      | Unit          |
|----------|------------------------------------|------|-----|----------|---------------|
| $V_{IH}$ | Input HIGH Voltage (LVCMOS/LVTTTL) | 2.0  |     | $V_{CC}$ | V             |
| $V_{IL}$ | Input LOW Voltage (LVCMOS/LVTTTL)  | GND  |     | 0.8      | V             |
| $I_{IH}$ | Input HIGH Current                 | -150 |     | 150      | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                  | -150 |     | 150      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 9. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.465\text{ V}$ ;  $GND = 0\text{ V}$  (Note 7)

| Symbol                   | Characteristic   | -40°C      |               |                  | 25°C       |               |                  | 85°C       |               |                  | Unit |
|--------------------------|--|------------|---------------|------------------|------------|---------------|------------------|------------|---------------|------------------|------|
|                          |  | Min        | Typ           | Max              | Min        | Typ           | Max              | Min        | Typ           | Max              |      |
| $f_{inMAX}$              | Maximum Input CLOCK Frequency<br>QA/QB = ( $\div 2$ , $\div 4$ , $\div 8$ , $\div 16$ )<br>QA = ( $\div 1$ )   | 3.0<br>1.5 |               |                  | 3.0<br>1.5 |               |                  | 3.0<br>1.5 |               |                  | GHz  |
| $V_{OUTPP}$              | Output Voltage Amplitude (Notes 9, 10)<br>QA ( $\div 2$ , 4, 8), QB ( $\div n$ )<br>QA ( $\div 1$ ), QB ( $\div n$ )<br>$f_{in} \leq 3.0\text{ GHz}$<br>$f_{in} \leq 1.5\text{ GHz}$ | 200<br>200 | 350<br>350    | 450<br>450       | 200<br>200 | 350<br>350    | 450<br>450       | 200<br>200 | 350<br>350    | 450<br>450       | mV   |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to<br>Output Differential @ 50 MHz<br>CLK, Qn<br>MR, Qn  | 550<br>420 |               | 780<br>660       | 550<br>420 |               | 780<br>660       | 550<br>420 |               | 780<br>660       | ps   |
| $t_{RR}$                 | Reset Recovery   | 0          | -90           |                  | 0          | -90           |                  | 0          | -90           |                  | ps   |
| $t_s$                    | Setup Time @ 50 MHz<br>EN, CLK<br>SELA/B, CLK  | 0<br>0     | -60<br>-300   |                  | 0<br>0     | -60<br>-300   |                  | 0<br>0     | -60<br>-300   |                  | ps   |
| $t_h$                    | Hold Time @ 50 MHz<br>CLK, EN<br>CLK, SELA/B   | 150<br>700 | 65<br>200     |                  | 150<br>700 | 65<br>200     |                  | 150<br>700 | 65<br>200     |                  | ps   |
| $t_{skew}$               | Within-Device Skew @ 50 MHz<br>Device-to-Device Skew<br>Duty Cycle Skew<br>(Note 8)<br>(Note 8)<br>(Note 8)  |            | 5<br>25<br>25 | 30<br>80<br>40   |            | 5<br>30<br>30 | 30<br>90<br>45   |            | 6<br>30<br>30 | 35<br>90<br>45   | ps   |
| $t_{PW}$                 | Minimum Pulse Width<br>MR  | 550        |               |                  | 550        |               |                  | 550        |               |                  | ps   |
| $t_{JITTER}$             | RMS Random Clock Jitter  |            |               | 2                |            |               | 2                |            |               | 2                | ps   |
| $V_{INPP}$               | Input Voltage Swing (Differential Configuration)<br>(Note 9)   | 100        |               | $V_{CC}$<br>-GND | 100        |               | $V_{CC}$<br>-GND | 100        |               | $V_{CC}$<br>-GND | mV   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times @ 50 MHz<br>(20% - 80%)<br>Qn, Qn   | 70         | 120           | 190              | 70         | 120           | 190              | 70         | 120           | 190              | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured using a 750 mV, 50% duty cycle clock source. All loading with 100  $\Omega$  across LVDS outputs.
8. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
9. Input and output voltage swing is a single-ended measurement operating in differential mode.
10. Output Voltage Amplitude ( $V_{OHCLK} - V_{OLCLK}$ ) at input CLOCK frequency,  $f_{in}$ . The output frequency,  $f_{out}$ , is the input CLOCK frequency divided by  $n$ ,  $f_{out} = f_{in} \div n$ . Input CLOCK frequency is  $\leq 3.0\text{ GHz}$ .

Application Information

The NB6N239S is a high-speed, low skew clock divider with two divider circuits, each having selectable clock divide ratios;  $\div 1/2/4/8$  and  $\div 2/4/8/16$ . Both divider circuits drive differential LVDS compatible outputs. The internal dividers are synchronous to each other. Therefore, the common output edges are precisely aligned.

The NB6N239S clock inputs can be driven by a variety of differential signal level technologies including LVDS, LVPECL, HSTL, or CML. The differential clock input buffer employs a pair of internal 50  $\Omega$  termination resistors in a 100  $\Omega$  center-tapped configuration and accessible via the VT pin. This feature provides transmission line termination on-chip, at the receiver end, eliminating external components. The  $V_{BBAC}$  reference output is recommended to be used to rebias differential or

single-ended input capacitor-coupled CLOCK signals. For the capacitor-coupled CLK and/or  $\overline{CLK}$  inputs,  $V_{BBAC}$  should be connected to the  $V_T$  pin and bypassed to ground with a 0.01  $\mu F$  capacitor. Inputs CLK and  $\overline{CLK}$  must be signal driven or auto oscillation may result.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal divider flip-flops will only be enabled/disabled when the internal clock is in the LOW state. This avoids any chance of generating a runt pulse on the internal clock when the device is enabled/disabled, as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

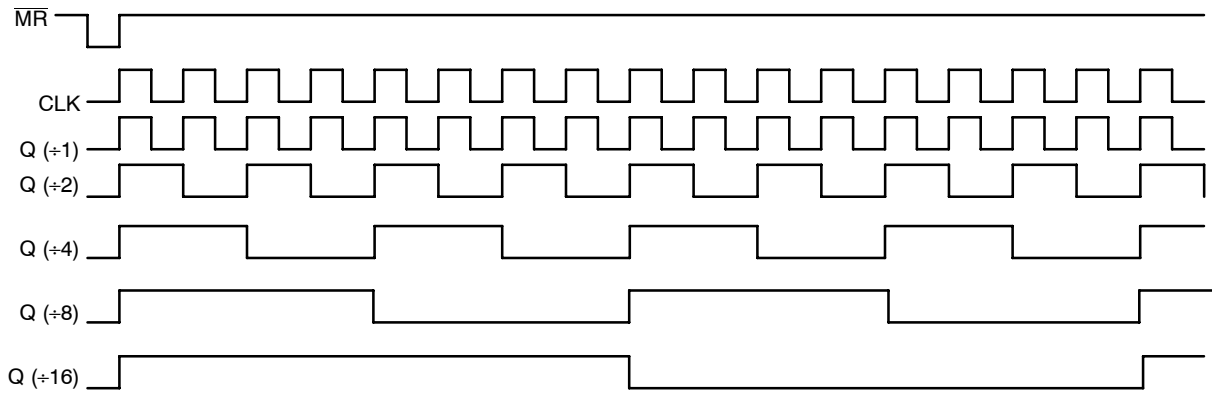
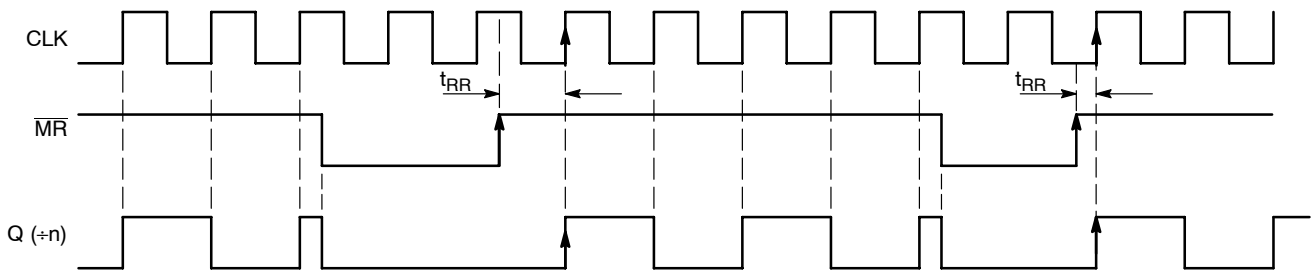


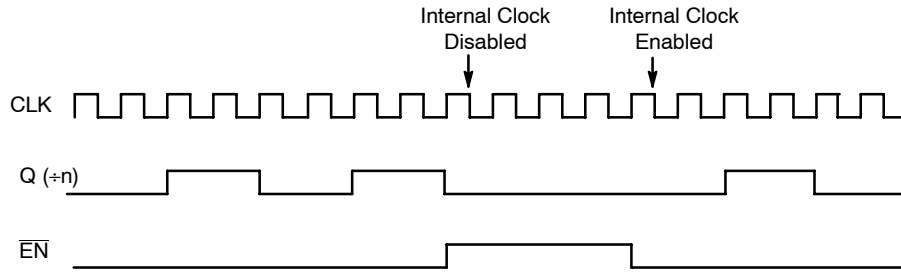
Figure 4. Timing Diagram



NOTE: On the rising edge of  $\overline{MR}$ , Q goes HIGH after the first rising edge of CLK.

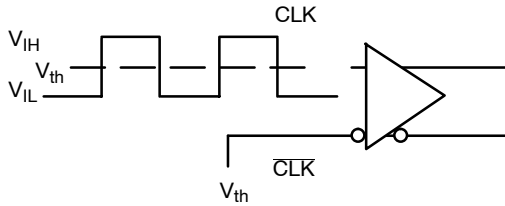
Figure 5. Master Reset Timing Diagram

# NB6N239S

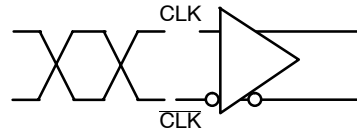


**Figure 6. Output Enable Timing Diagrams**

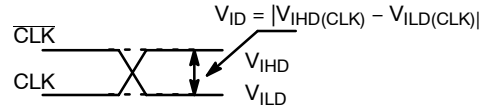
The  $\overline{EN}$  signal will “freeze” the internal divider flip-flops on the first falling edge of CLK after its assertion. The internal divider flip-flops will maintain their state during the freeze. When  $\overline{EN}$  is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip-flops will “unfreeze” and continue to their next state count with proper phase relationships.



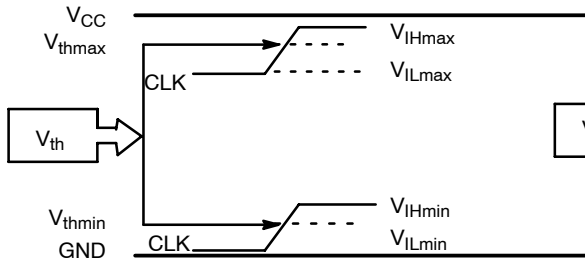
**Figure 7. Differential Input Driven Single-Ended**



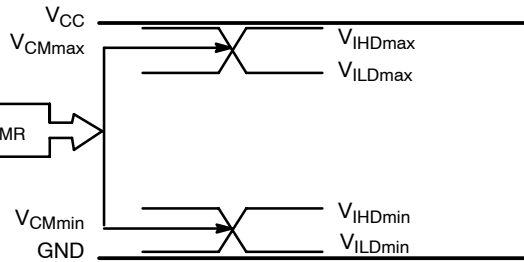
**Figure 8. Differential Inputs Driven Differentially**



**Figure 9. Differential Inputs Driven Differentially**



**Figure 10.  $V_{th}$  Diagram**



**Figure 11.  $V_{CMR}$  Diagram**



# NB6N239S

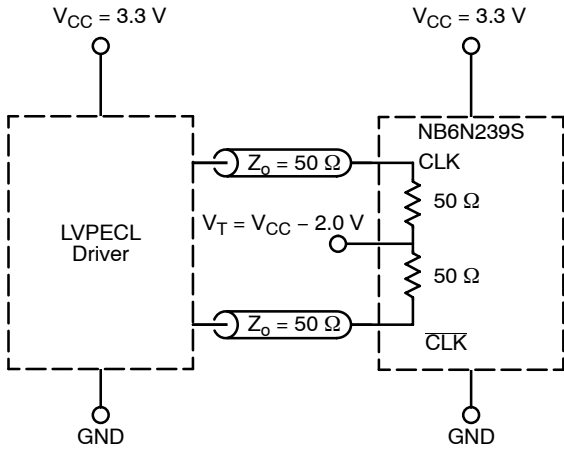


Figure 12. LVPECL Interface

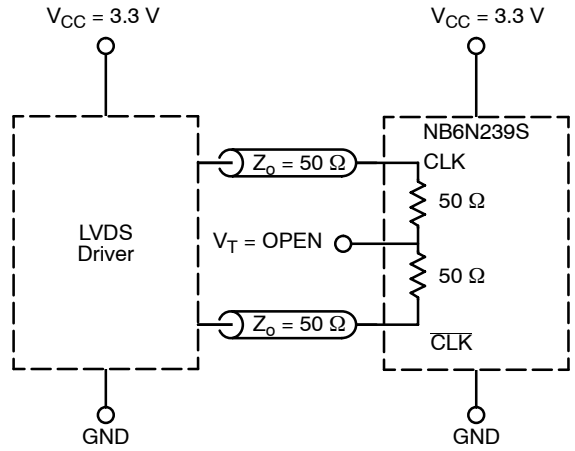


Figure 13. LVDS Interface

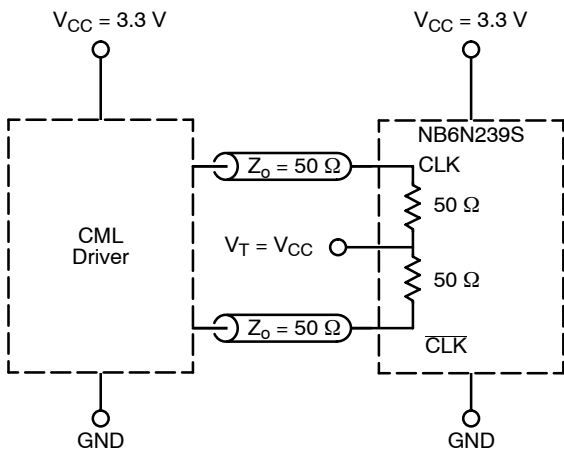


Figure 14. Standard 50 Ω Load CML Interface

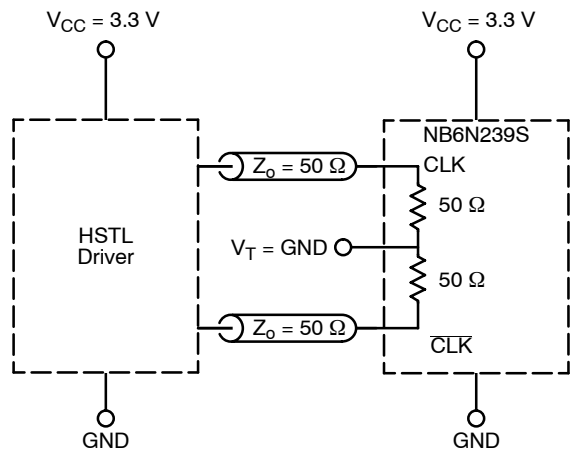


Figure 15. Standard 50 Ω Load HSTL Interface

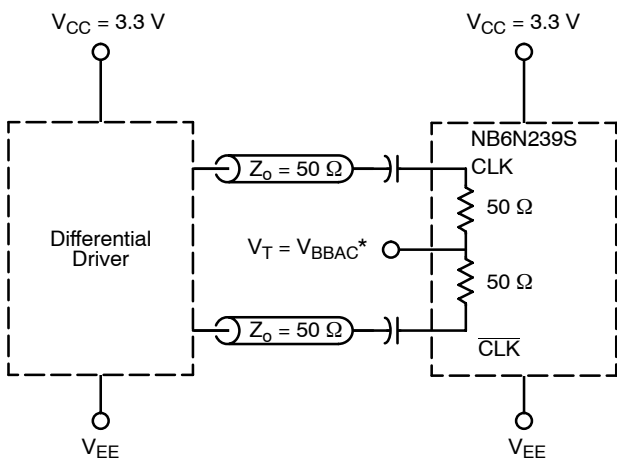


Figure 16. Capacitor-Coupled Differential Interface ( $V_T$  Connected to  $V_{BBAC}$ )

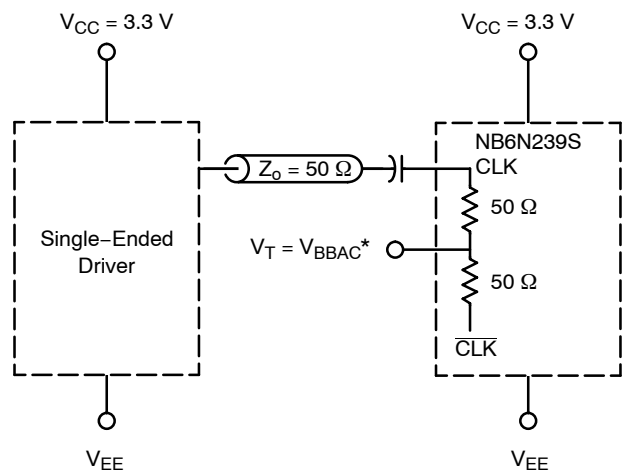
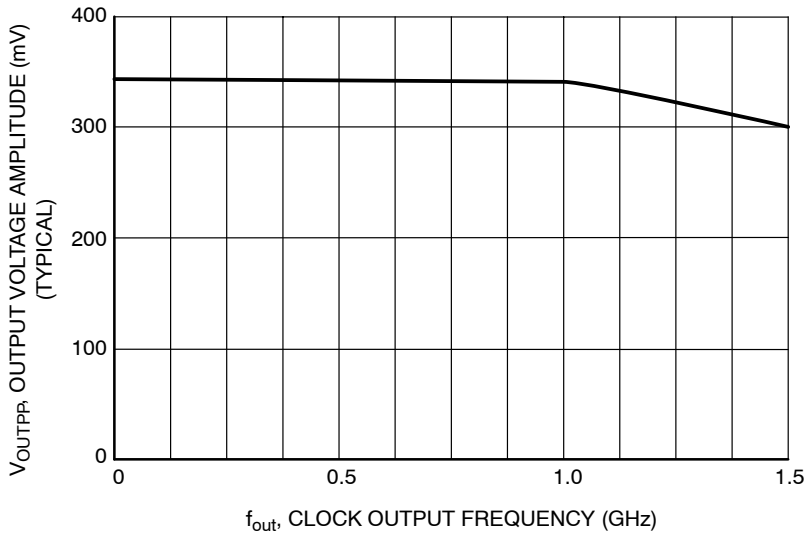


Figure 17. Capacitor-Coupled Single-Ended Interface ( $V_T$  Connected to  $V_{BBAC}$ )

\* $V_{BBAC}$  bypassed to ground with a 0.01  $\mu$ F capacitor.

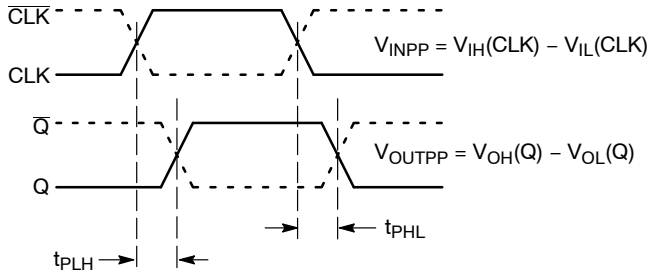
# NB6N239S



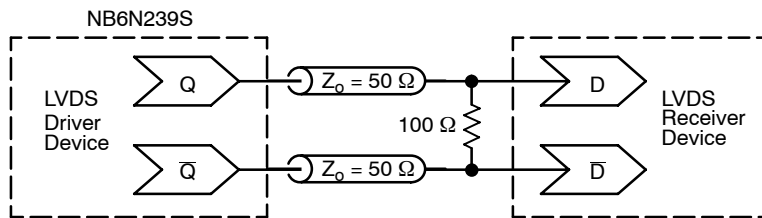
**Figure 18. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Output Clock Frequency at 25°C (Typical)**

$$f_{out} (QA/QB) = f_{in} \div n;$$

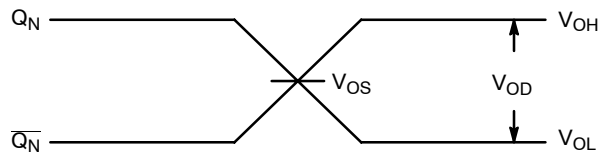
For  $n = 2, 4, 8, 16$ ;  $f_{in} \leq 3.0$  GHz  
 For  $n = 1$ ;  $f_{in} \leq 1.5$  GHz



**Figure 19. AC Reference Measurement**



**Figure 20. Typical LVDS Termination for Output Driver and Device Evaluation, If Receiver Has On-chip Termination, 100  $\Omega$  Resistor is Not Needed**



**Figure 21. LVDS Output**

# NB6N239S

## ORDERING INFORMATION

| Device        | Package                       | Shipping†          |
|---------------|-------------------------------|--------------------|
| NB6N239SMN    | QFN-16, 3 x 3 mm              | 123 Units / Rail   |
| NB6N239SMNG   | QFN-16, 3 x 3 mm<br>(Pb-Free) | 123 Units / Rail   |
| NB6N239SMNR2  | QFN-16, 3 x 3 mm              | 3000 / Tape & Reel |
| NB6N239SMNR2G | QFN-16, 3 x 3 mm<br>(Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

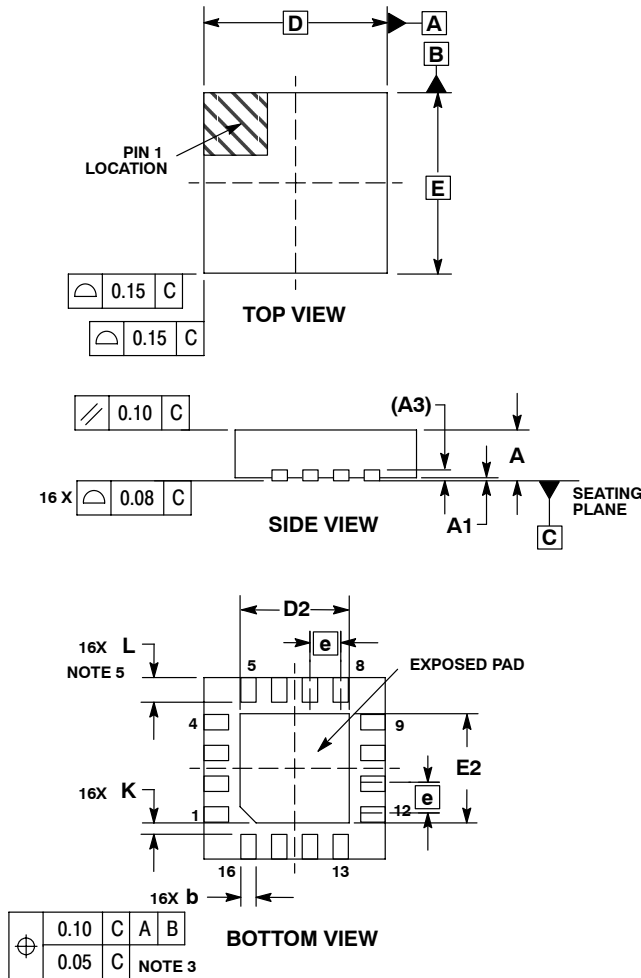
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# NB6N239S

## PACKAGE DIMENSIONS

16 PIN QFN  
CASE 485G-01  
ISSUE C

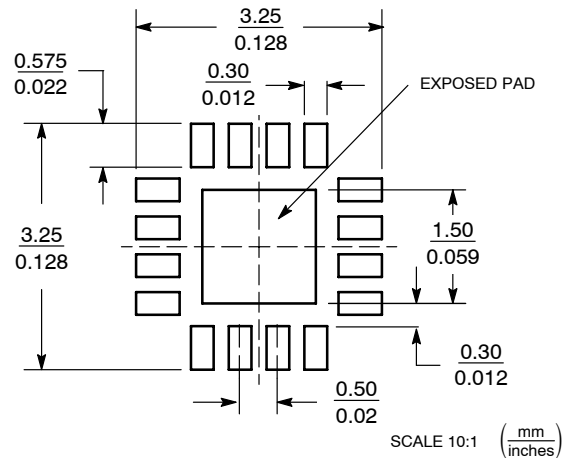


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5.  $L_{max}$  CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.18 | 0.30 |
| D           | 3.00 | BSC  |
| D2          | 1.65 | 1.85 |
| E           | 3.00 | BSC  |
| E2          | 1.65 | 1.85 |
| e           | 0.50 | BSC  |
| K           | 0.18 | TYP  |
| L           | 0.30 | 0.50 |

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ECLinPS and ECLinPS MAX are trademarks of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А