

144-Ball μ BGA
Commercial Temp
Industrial Temp

64M x 9, 32M x 18, 16M x 36
576Mb CIO Low Latency DRAM (LLDRAM II)

533 MHz–300 MHz
2.5 V V_{EXT}
1.8 V V_{DD}
1.5 V or 1.8 V V_{DDQ}

Features

- Pin- and function-compatible with Micron RLDRAM® II
- 533 MHz DDR operation (1.067Gb/s/pin data rate)
- 38.4 Gb/s peak bandwidth (x36 at 533 MHz clock frequency)
- 16M x 36, 32M x 18, and 64M x 9 organizations available
- 8 banks
- Reduced cycle time (15 ns at 533 MHz)
- Address Multiplexing (Nonmultiplexed address option available)
- SRAM-type interface
- Programmable Read Latency (RL), row cycle time, and burst sequence length
- Balanced Read and Write Latencies in order to optimize data bus utilization
- Data mask for Write commands
- Differential input clocks (CK, \overline{CK})
- Differential input data clocks (DKx, \overline{DKx})
- On-chip DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32 ms refresh (16K refresh for each bank; 128K refresh command must be issued in total each 32 ms)
- 144-ball μ BGA package
- HSTL I/O (1.5 V or 1.8 V nominal)
- 25 Ω –60 Ω matched impedance outputs
- 2.5 V V_{EXT} , 1.8 V V_{DD} , 1.5 V or 1.8 V V_{DDQ} I/O
- On-die termination (ODT) R_{TT}
- Commercial and Industrial Temperature
 - Commercial (+0° $\leq T_C \leq$ +95°C)
 - Industrial (–40° $\leq T_C \leq$ +95°C)

Introduction

The GSI Technology 576Mb Low Latency DRAM (LLDRAM II) is a high speed memory device designed for high address rate data processing typically found in networking and telecommunications applications. The 8-bank architecture and low tRC allows access rates formerly only found in SRAMs.

The Double Data Rate (DDR) I/O interface provides high bandwidth data transfers, clocking out two beats of data per clock cycle at the I/O balls. Source-synchronous clocking can be implemented on the host device with the provided free-running data output clock.

Commands, addresses, and control signals are single data rate signals clocked in by the True differential input clock transition, while input data is clocked in on both crossings of the input data clock(s).

Read and Write data transfers always in short bursts. The burst length is programmable to 2, 4 or 8 by setting the Mode Register.

The device is supplied with 2.5 V V_{EXT} and 1.8 V V_{DD} for the core, and 1.5 V or 1.8 V for the HSTL output drivers.

Internally generated row addresses facilitate bank-scheduled refresh.

The device is delivered in an efficient μ BGA 144-ball package.



64M x 9 Mb Ball Assignments—144-Ball μ BGA—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|-------------------------|------------------------|------------------|------------------|---|---|---|---|------------------|-------------------------|------------------|------------------------|
| A | V _{REF} | V _{SS} | V _{EXT} | V _{SS} | | | | | V _{SS} | V _{EXT} | TMS | TCK |
| B | V _{DD} | DNU ³ | DNU ³ | V _{SS} | | | | | V _{SS} | DQ0 | DNU ³ | V _{DD} |
| C | V _{TT} | DNU ³ | DNU ³ | V _{DDQ} | | | | | V _{DDQ} | DQ1 | DNU ³ | V _{TT} |
| D | A22 ¹ | DNU ³ | DNU ³ | V _{SS} | | | | | V _{SS} | $\overline{\text{QK0}}$ | QK0 | V _{SS} |
| E | A21 | DNU ³ | DNU ³ | V _{DDQ} | | | | | V _{DDQ} | DQ2 | DNU ³ | A20 |
| F | A5 | DNU ³ | DNU ³ | V _{SS} | | | | | V _{SS} | DQ3 | DNU ³ | QVLD |
| G | A8 | A6 | A7 | V _{DD} | | | | | V _{DD} | A2 | A1 | A0 |
| H | B2 | A9 | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A4 | A3 |
| J | NF ² | NF ² | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B0 | CK |
| K | DK | $\overline{\text{DK}}$ | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B1 | $\overline{\text{CK}}$ |
| L | $\overline{\text{REF}}$ | $\overline{\text{CS}}$ | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A14 | A13 |
| M | $\overline{\text{WE}}$ | A16 | A17 | V _{DD} | | | | | V _{DD} | A12 | A11 | A10 |
| N | A18 | DNU ³ | DNU ³ | V _{SS} | | | | | V _{SS} | DQ4 | DNU ³ | A19 |
| P | A15 | DNU ³ | DNU ³ | V _{DDQ} | | | | | V _{DDQ} | DQ5 | DNU ³ | DM |
| R | V _{SS} | DNU ³ | DNU ³ | V _{SS} | | | | | V _{SS} | DQ6 | DNU ³ | V _{SS} |
| T | V _{TT} | DNU ³ | DNU ³ | V _{DDQ} | | | | | V _{DDQ} | DQ7 | DNU ³ | V _{TT} |
| U | V _{DD} | DNU ³ | DNU ³ | V _{SS} | | | | | V _{SS} | DQ8 | DNU ³ | V _{DD} |
| V | V _{REF} | ZQ | V _{EXT} | V _{SS} | | | | | V _{SS} | V _{EXT} | TDO | TDI |

Notes:

1. Reserved for future use. This pin may be connected to ground.
2. No function. This pin may have parasitic characteristics of a clock input signal. It may be connected to GND.
3. Do not use. This pin may have parasitic characteristics of an I/O. It may be connected to GND.

32M x 18 Ball Assignments—144-Ball μ BGA—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|-------------------------|------------------------|-------------------------|------------------|---|---|---|---|------------------|-------------------------|------------------|------------------------|
| A | V _{REF} | V _{SS} | V _{EXT} | V _{SS} | | | | | V _{SS} | V _{EXT} | TMS | TCK |
| B | V _{DD} | DNU ⁴ | DQ4 | V _{SS} | | | | | V _{SS} | DQ0 | DNU ⁴ | V _{DD} |
| C | V _{TT} | DNU ⁴ | DQ5 | V _{DDQ} | | | | | V _{DDQ} | DQ1 | DNU ⁴ | V _{TT} |
| D | A22 ¹ | DNU ⁴ | DQ6 | V _{SS} | | | | | V _{SS} | $\overline{\text{QK0}}$ | QK0 | V _{SS} |
| E | A21 ² | DNU ⁴ | DQ7 | V _{DDQ} | | | | | V _{DDQ} | DQ2 | DNU ⁴ | A20 |
| F | A5 | DNU ⁴ | DQ8 | V _{SS} | | | | | V _{SS} | DQ3 | DNU ⁴ | QVLD |
| G | A8 | A6 | A7 | V _{DD} | | | | | V _{DD} | A2 | A1 | A0 |
| H | B2 | A9 | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A4 | A3 |
| J | NF ³ | NF ³ | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B0 | CK |
| K | DK | $\overline{\text{DK}}$ | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B1 | $\overline{\text{CK}}$ |
| L | $\overline{\text{REF}}$ | $\overline{\text{CS}}$ | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A14 | A13 |
| M | $\overline{\text{WE}}$ | A16 | A17 | V _{DD} | | | | | V _{DD} | A12 | A11 | A10 |
| N | A18 | DNU ⁴ | DQ14 | V _{SS} | | | | | V _{SS} | DQ9 | DNU ⁴ | A19 |
| P | A15 | DNU ⁴ | DQ15 | V _{DDQ} | | | | | V _{DDQ} | DQ10 | DNU ⁴ | DM |
| R | V _{SS} | QK1 | $\overline{\text{QK1}}$ | V _{SS} | | | | | V _{SS} | DQ11 | DNU ⁴ | V _{SS} |
| T | V _{TT} | DNU ⁴ | DQ16 | V _{DDQ} | | | | | V _{DDQ} | DQ12 | DNU ⁴ | V _{TT} |
| U | V _{DD} | DNU ⁴ | DQ17 | V _{SS} | | | | | V _{SS} | DQ13 | DNU ⁴ | V _{DD} |
| V | V _{REF} | ZQ | V _{EXT} | V _{SS} | | | | | V _{SS} | V _{EXT} | TDO | TDI |

Notes:

1. Reserved for future use. This pin may be connected to GND.
2. Reserved for future use. This pin may have parasitic characteristics of an address input signal. It may be connected to GND.
3. No function. This pin may have parasitic characteristics of a clock input signal. It may be connected to GND.
4. Do not use. This pin may have parasitic characteristics of an I/O. It may be connected to GND.

16M x 36 Ball Assignments—144-Ball μ BGA—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|-------------------------|-------------------------|-------------------------|------------------|---|---|---|---|------------------|-------------------------|------|------------------------|
| A | V _{REF} | V _{SS} | V _{EXT} | V _{SS} | | | | | V _{SS} | V _{EXT} | TMS | TCK |
| B | V _{DD} | DQ8 | DQ9 | V _{SS} | | | | | V _{SS} | DQ1 | DQ0 | V _{DD} |
| C | V _{TT} | DQ10 | DQ11 | V _{DDQ} | | | | | V _{DDQ} | DQ3 | DQ2 | V _{TT} |
| D | A22 ¹ | DQ12 | DQ13 | V _{SS} | | | | | V _{SS} | $\overline{\text{QK0}}$ | QK0 | V _{SS} |
| E | A21 ² | DQ14 | DQ15 | V _{DDQ} | | | | | V _{DDQ} | DQ5 | DQ4 | A20 ² |
| F | A5 | DQ16 | DQ17 | V _{SS} | | | | | V _{SS} | DQ7 | DQ6 | QVLD |
| G | A8 | A6 | A7 | V _{DD} | | | | | V _{DD} | A2 | A1 | A0 |
| H | B2 | A9 | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A4 | A3 |
| J | DK0 | $\overline{\text{DK0}}$ | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B0 | CK |
| K | DK1 | $\overline{\text{DK1}}$ | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B1 | $\overline{\text{CK}}$ |
| L | $\overline{\text{REF}}$ | $\overline{\text{CS}}$ | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A14 | A13 |
| M | $\overline{\text{WE}}$ | A16 | A17 | V _{DD} | | | | | V _{DD} | A12 | A11 | A10 |
| N | A18 | DQ24 | DQ25 | V _{SS} | | | | | V _{SS} | DQ35 | DQ34 | A19 |
| P | A15 | DQ22 | DQ23 | V _{DDQ} | | | | | V _{DDQ} | DQ33 | DQ32 | DM |
| R | V _{SS} | QK1 | $\overline{\text{QK1}}$ | V _{SS} | | | | | V _{SS} | DQ31 | DQ30 | V _{SS} |
| T | V _{TT} | DQ20 | DQ21 | V _{DDQ} | | | | | V _{DDQ} | DQ29 | DQ28 | V _{TT} |
| U | V _{DD} | DQ18 | DQ19 | V _{SS} | | | | | V _{SS} | DQ27 | DQ26 | V _{DD} |
| V | V _{REF} | ZQ | V _{EXT} | V _{SS} | | | | | V _{SS} | V _{EXT} | TDO | TDI |

Notes:

1. Reserved for future use. This pin may be connected to GND.
2. Reserved for future use. This pin may have parasitic characteristics of an address pin. It may be connected to GND.

Ball Descriptions

| Symbol | Type | Description |
|--|--------|---|
| A0–A21 | Input | Address Inputs —A0–A21 define the row and column addresses for Read and Write Operations. During a Mode Register Set (MRS), the address inputs define the register settings. They are sampled at the rising edge of CK. |
| BA0–B2 | Input | Bank Address inputs —Select to which internal bank a command is being applied. |
| CK, $\overline{\text{CK}}$ | Input | Input Clock —CK and $\overline{\text{CK}}$ are differential input clocks. Addresses and commands are latched on the rising edge of CK. $\overline{\text{CK}}$ is ideally 180° out of phase with CK. |
| $\overline{\text{CS}}$ | Input | Chip Select — $\overline{\text{CS}}$ enables the command decoder when Low and disables it when High. When the command decoder is disabled, new commands are ignored, but internal operations continue. |
| DQ0–DQ35 | Input | Data Input —The DQ signals form the 36-bit data bus. During Read commands, the data is referenced to both edges of QKx. During Write commands, the data is sampled at both edges of DK. |
| DK, $\overline{\text{DK}}$ | Input | Input Data Clock —DK and $\overline{\text{DK}}$ are the differential input data clocks. All input data is referenced to both edges of DK. $\overline{\text{DK}}$ is ideally 180° out of phase with DK. For the x36 device, DQ0–DQ17 are referenced to DK0 and $\overline{\text{DK0}}$ and DQ18–DQ35 are referenced to DK1 and $\overline{\text{DK1}}$. For the x9 and x18 devices, all DQs are referenced to DK and $\overline{\text{DK}}$. All DKx and $\overline{\text{DKx}}$ pins must always be supplied to the device. |
| DM | Input | Input Data Mask —The DM signal is the input mask signal for Write data. Input data is masked when DM is sampled High. DM is sampled on both edges of DK (DK1 for the x36 configuration). Tie signal to ground if not used. |
| TCK | Input | IEEE 1149.1 clock input —This ball must be tied to V_{SS} if the JTAG function is not used. |
| TMS, TDI | Input | IEEE 1149.1 test inputs —These balls may be left as no connects if the JTAG function is not used. |
| $\overline{\text{WE}}$, $\overline{\text{REF}}$ | Input | Command Inputs —Sampled at the positive edge of CK, $\overline{\text{WE}}$ and $\overline{\text{REF}}$ define (together with $\overline{\text{CS}}$) the command to be executed. |
| V_{REF} | Input | Input Reference Voltage —Nominally $V_{\text{DDQ}}/2$. Provides a reference voltage for the input buffers. |
| ZQ | I/O | External Impedance (25–60Ω) —This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to $0.2 * RQ$, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the Minimum Impedance mode. Connecting ZQ to V_{DD} invokes the Maximum Impedance mode. Refer to the Mode Register Definition diagrams (Mode Register Bit 8 (M8)) to activate or deactivate this function. |
| QKx, $\overline{\text{QKx}}$ | Output | Output Data Clocks —QKx and $\overline{\text{QKx}}$ are opposite polarity, output data clocks. They are free running, and during Reads, are edge-aligned with data output from the LLDRAM II. $\overline{\text{QKx}}$ is ideally 180° out of phase with QKx. For the x36 device, QK0 and $\overline{\text{QK0}}$ are aligned with DQ0–DQ17, and QK1 and $\overline{\text{QK1}}$ are aligned with DQ18–DQ35. For the x18 device, QK0 and $\overline{\text{QK0}}$ are aligned with DQ0–DQ8, while QK1 and $\overline{\text{QK1}}$ are aligned with Q9–Q17. For the x9 device, all DQs are aligned with QK0 and $\overline{\text{QK0}}$. |

Ball Descriptions (Continued)

| Symbol | Type | Description |
|------------------|--------|--|
| QVLD | Output | Data Valid —The QVLD pin indicates valid output data. QVLD is edge-aligned with QKx and \overline{QKx} . |
| TDO | Output | IEEE 1149.1 Test Output —JTAG output. This ball may be left as no connect if the JTAG function is not used. |
| V _{DD} | Supply | Power Supply —Nominally, 1.8 V. See the DC Electrical Characteristics and Operating Conditions section for range. |
| V _{DDQ} | Supply | DQ Power Supply —Nominally, 1.5 V or 1.8 V. Isolated on the device for improved noise immunity. See the DC Electrical Characteristics and Operating Conditions section for range. |
| V _{EXT} | Supply | Power Supply —Nominally, 2.5 V. See the DC Electrical Characteristics and Operating Conditions section for range. |
| V _{SS} | Supply | Ground |
| V _{TT} | — | Power Supply —Isolated termination supply. Nominally, V _{DDQ} /2. See the DC Electrical Characteristics and Operating Conditions section for range. |
| A22 | — | Reserved for Future Use —This signal is not connected and may be connected to ground. |
| DNU | — | Do Not Use —These balls may be connected to ground. |
| NF | — | No Function —These balls can be connected to ground. |

Not Recommended for New Design—Discontinued Product

Operations

Initialization

A specific power-up and initialization sequence must be observed. Other sequences may result in undefined operations or permanent damage to the device.

Power-up:

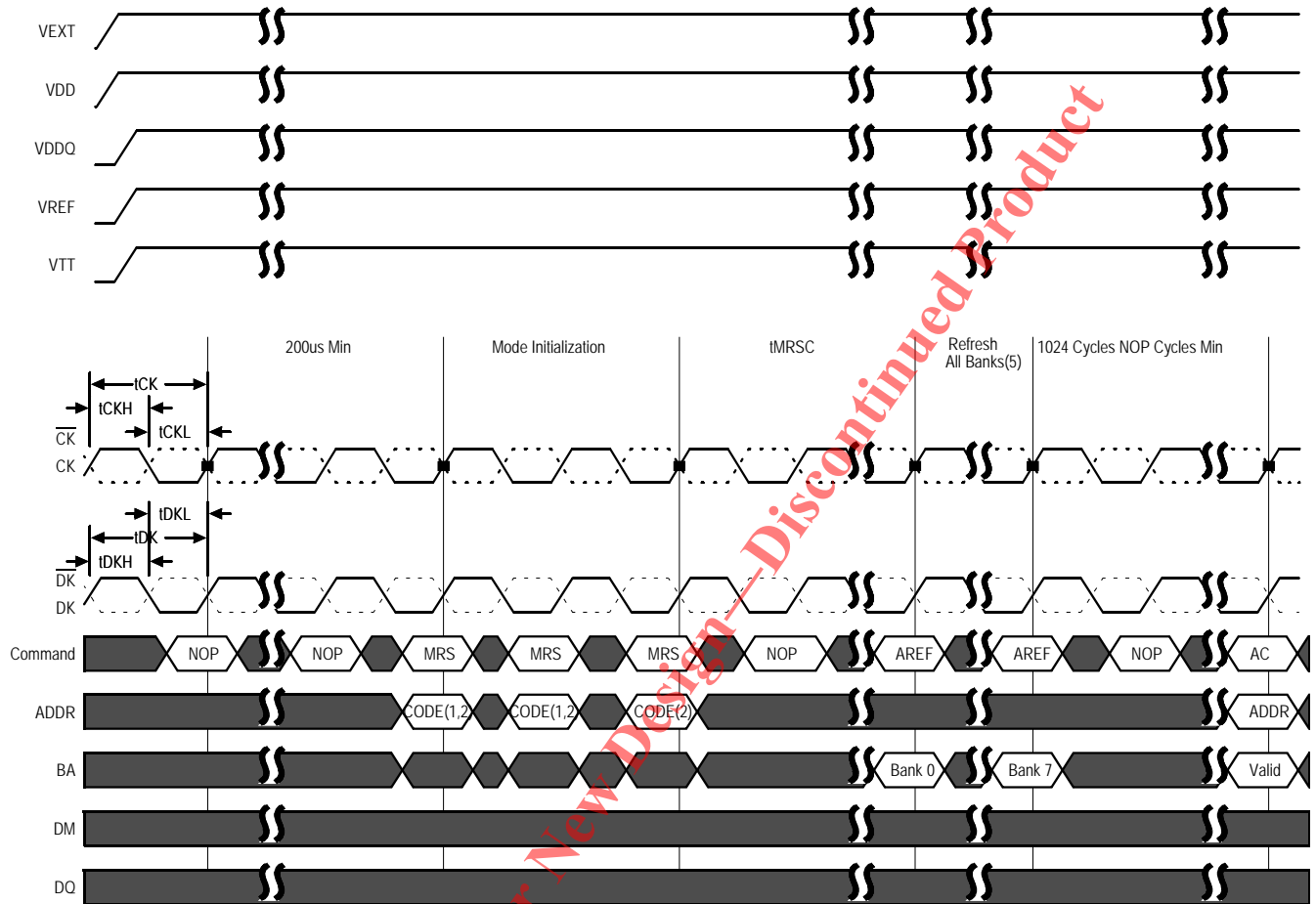
1. Apply power (V_{EXT} , V_{DD} , V_{DDQ} , V_{REF} , V_{TT}) . Start clock after the supply voltages are stable. Apply V_{DD} and V_{EXT} before or at the same time as V_{DDQ} ¹. Apply V_{DDQ} before or at the same time as V_{REF} and V_{TT} . The chip starts internal initialization only after both voltages approach their nominal levels. CK/\overline{CK} must meet $V_{ID(DC)}$ prior to being applied². Apply only NOP commands to start. Ensuring CK/\overline{CK} meet $V_{ID(DC)}$ while loading NOP commands guarantees that the LLDRAM II will not receive damaging commands during initialization.
2. Idle with continuing NOP commands for 200 μ s (MIN).
3. Issue three or more consecutive MRS commands: two or more dummies plus one valid MRS. The consecutive MRS commands will reset internal logic of the LLDRAM II. $tMRSC$ does not need to be met between these consecutive commands. Address pins should be held Low during the dummy MRS commands.
4. $tMRSC$ after the valid MRS, issues an AUTO REFRESH command to all 8 banks in any order (along with 1024 NOP commands) prior to normal operation. As always, tRC must be met between any AUTO REFRESH and any subsequent valid command to the same bank.

Notes:

1. It is possible to apply V_{DDQ} before V_{DD} . However, when doing this, the DQs, DM, and all other pins with an output driver, will go High instead of tri-stating. These pins will remain High until V_{DD} is at the same level as V_{DDQ} . Care should be taken to avoid bus conflicts during this period.
2. If $V_{ID(DC)}$ on CK/\overline{CK} can not be met prior to being applied to the LLDRAM II, placing a large external resistor from \overline{CS} to V_{DD} is a viable option for ensuring the command bus does not receive unwanted commands during this unspecified state.

Not Recommended for New Design - Discontinued Product

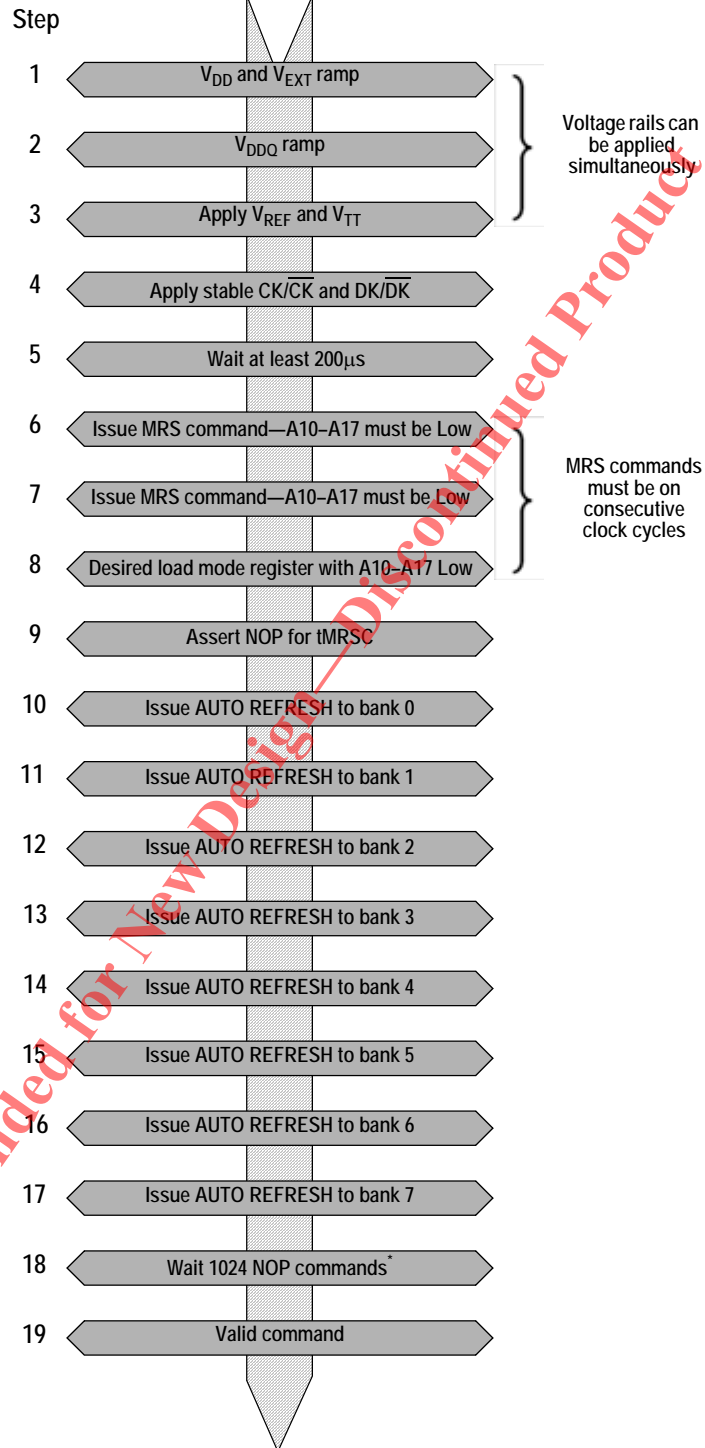
Power-Up Initialization Sequence



Notes:

1. Recommend all address pins held Low during dummy MRS commands.
2. A10–A17 must be Low.
3. DLL must be reset if tCK or V_{DD} are changed.
4. CK and \overline{CK} must be separated at all times to prevent bogus commands from being issued.
5. The sequence of the eight AUTO REFRESH commands (with respect to the 1024 NOP commands) does not matter. As is required for any operation, tRC must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank.

Power-Up Initialization Flow Chart


***Note:**

The sequence of the eight AUTO REFRESH commands (with respect to the 1024 NOP commands) does not matter. As is required for any operation, tRC must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank.

DLL Reset

Mode Register Bit 7 (M7) selects DLL Reset as is shown in the Mode Register Definition tables. The default setting for M7 is Low, whereby the DLL is disabled. Once M7 is set High, 1024 cycles (5 μ s at 200 MHz) are needed before a Read command can be issued. The delay allows the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tCKQK parameter. A reset of the DLL is necessary if tCK or V_{DD} is changed after the DLL has already been enabled. To reset the DLL, set M7 is Low. After waiting tMRSC, an MRS command should be issued to set M7 High. 1024 clock cycles must pass before loading the next Read command.

Driver Impedance Mapping

The LLDRAM II is equipped with programmable impedance output buffers. Setting Mode Register Bit 8 (M8) High during the MRS command activates the feature. Programmable impedance output buffers allow the user to match the driver impedance to the PCB trace impedance. To adjust the impedance, an external resistor (RQ) is connected between the ZQ ball and V_{SS}. The value of the resistor must be five times the desired impedance (e.g., a 300 Ω resistor produces an output impedance of 60 Ω). RQ values of 125 Ω –300 Ω are supported, allowing an output impedance range of 25–60 Ω (+/- 15 %).

The drive impedance of uncompensated output transistors can change over time due to changes in supply voltage and die temperature. When drive impedance control is enabled in the MRS, the value of RQ is periodically sampled and any needed impedance update is made automatically. Updates do not affect normal device operation or signal timing.

When Bit M8 is set Low during the MRS command, the output compensation circuits are still active but reference an internal resistance reference. The internal reference is imprecise and subject to temperature and voltage variations so output buffers are set to a nominal output impedance of 50 Ω , but are subject to a \pm 30 percent variance over the Commercial temperature range of the device.

Not Recommended for New Design—Discontinued Product

On-Die Termination (ODT)

Mode Register Bit 9 (M9) set to 1 during an MRS command enables ODT. With ODT on, the DQs and DM are terminated to V_{TT} with a resistance, R_{TT} . Command, address, QVLD, and clock signals are not terminated. The diagram below shows the equivalent circuit of a DQ receiver with ODT. When a tri-stated DQ begins to drive, the ODT function is briefly switched off. When a DQ stops driving at the end of a data transfer, ODT is switched back on. Two-state DM pin never deactivates ODT.

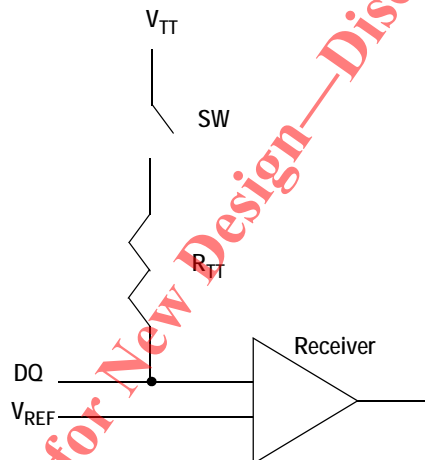
On-Die Termination DC Parameters

| Description | Symbol | Min | Max | Units | Notes |
|---------------------|----------|------------------|------------------|----------|-------|
| Termination Voltage | V_{TT} | $0.95 * V_{REF}$ | $1.05 * V_{REF}$ | V | 1, 2 |
| On-Die Termination | R_{TT} | 125 | 185 | Ω | 3 |

Notes:

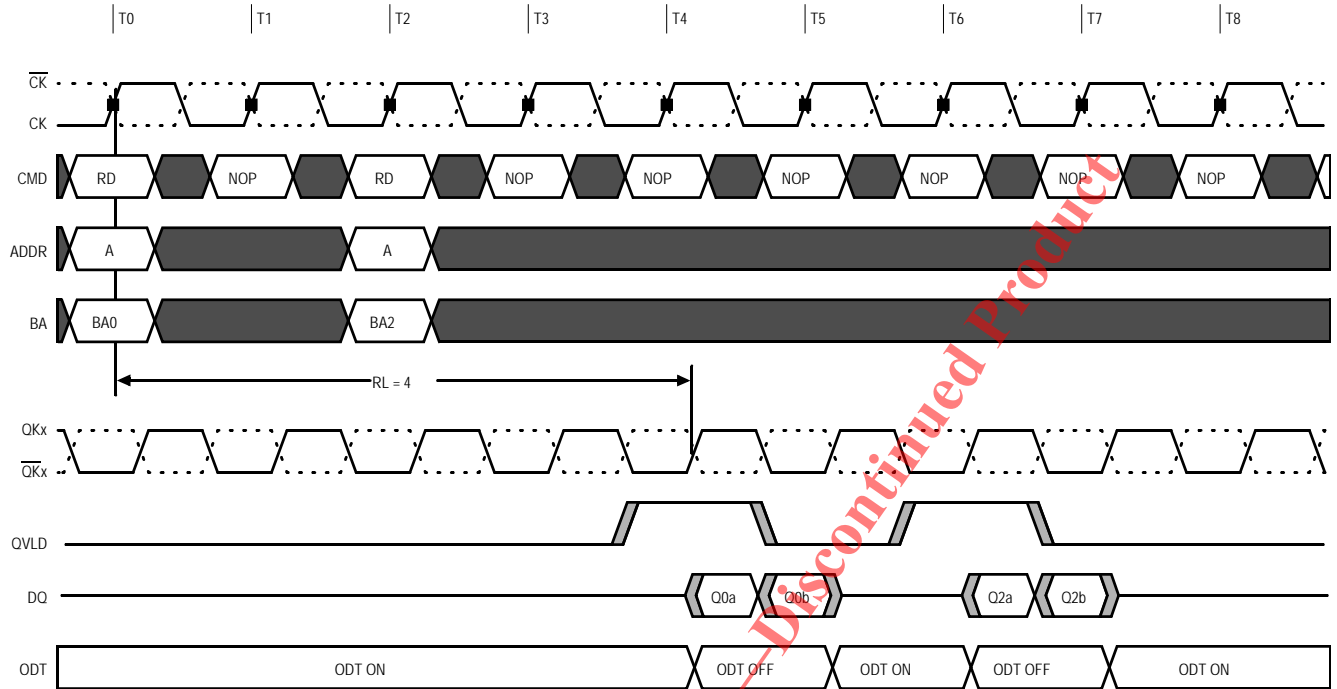
1. All voltages referenced to V_{SS} (GND).
2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF} .
3. The R_{TT} value is measured at 95°C T_C .

On-Die Termination-Equivalent Circuit

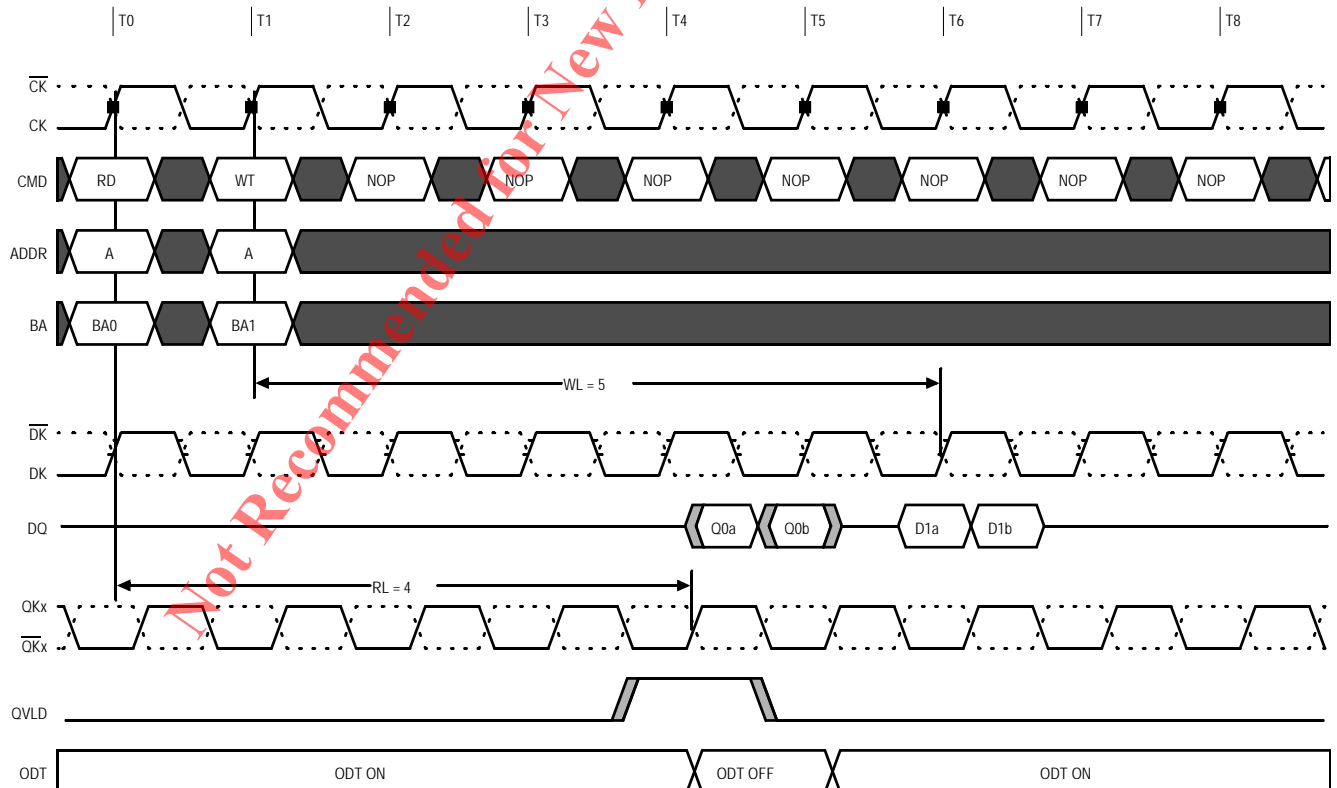


Not Recommended for New Design—Discontinued Product

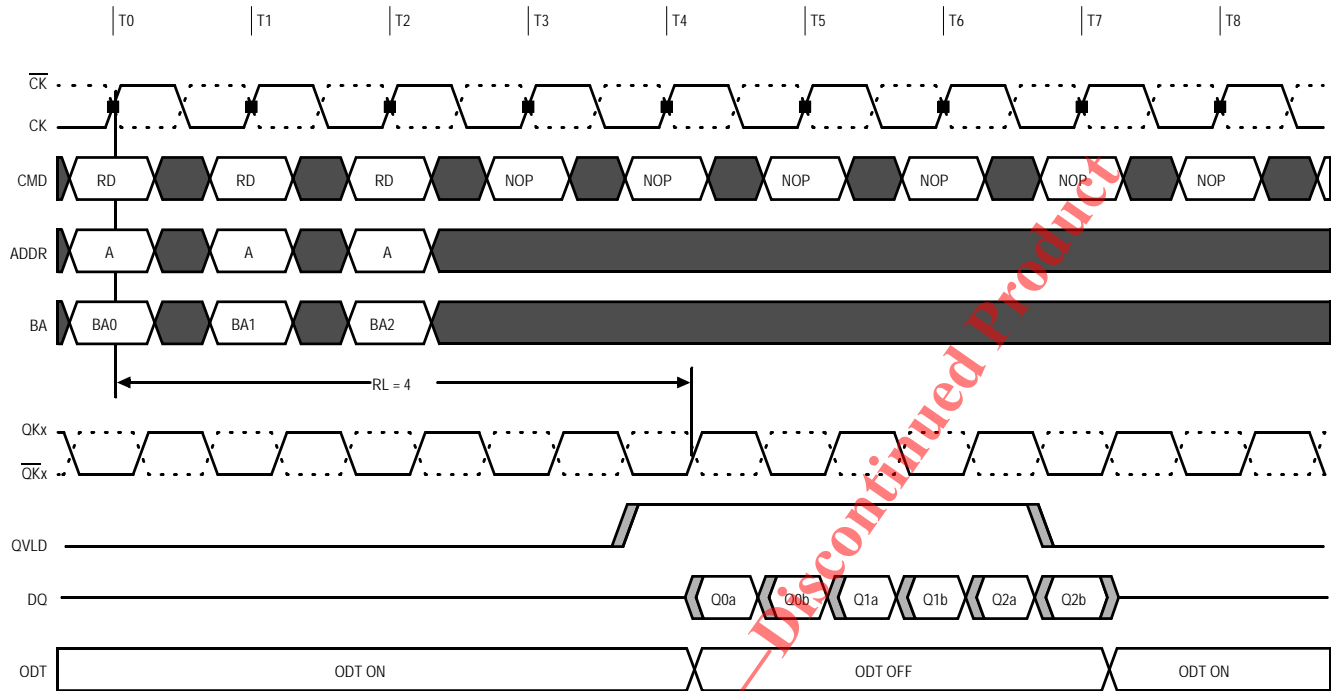
Read NOP Read On-Die Termination Burst Length 2, Configuration 1



Read-Write On-Die Termination Burst Length 2, Configuration 1



Read Burst On-die Termination Burst Length 2, Configuration 1



Not Recommended for New Design - Discontinued Product

Commands

Valid control commands are listed below. Any input commands not shown are illegal or reserved. All inputs must meet specified setup and hold times around the true crossing of CK.

Description of Commands

| Command | Description | Notes |
|----------|---|-------|
| DSEL/NOP | The NOP command is used to perform a no operation to the LLD RAM II, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during Idle or wait states. Operations already in progress are not affected. Output values depend on command history. | 1 |
| MRS | The Mode Register is set via the address inputs A0–A17. See the Mode Register Definition diagrams for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress. | — |
| READ | The Read command is used to initiate a burst read access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A _n selects the data location within the bank. | 2 |
| WRITE | The Write command is used to initiate a burst write access to a bank. The value on the BA0–BA2 inputs selects the bank, and the address provided on inputs A0–A _n selects the data location within the bank. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered Low, the corresponding data will be written to memory. If the DM signal is registered High, the corresponding data inputs will be ignored (that is, this part of the data word will not be written). | 2 |
| AREF | The AREF command is used during normal operation of the LLD RAM II to refresh the memory content of a bank. The command is non-persistent, so it must be issued each time a refresh is required. The value on the BA0–BA2 inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. See the Auto Refresh section for more details. | — |

Notes:

1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. For the value of "n", see Address Widths at Different Burst Lengths table.

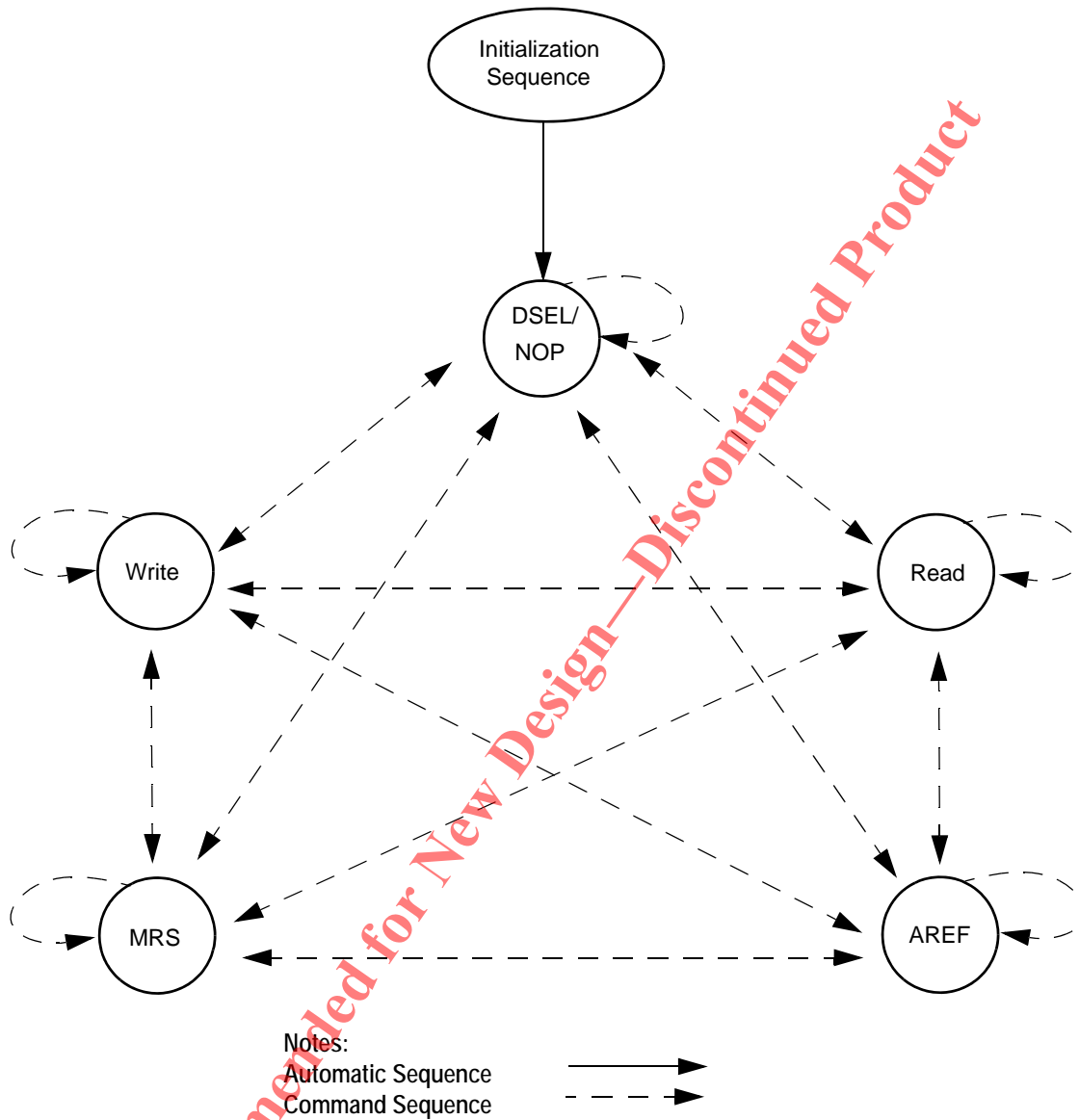
Command Table

| Operation | Command | \overline{CS} | \overline{WE} | \overline{REF} | A0–A _n | BA0–BA2 | Notes |
|------------------------------|----------|-----------------|-----------------|------------------|-------------------|---------|-------|
| Device Deselect/No Operation | DSEL/NOP | H | X | X | X | X | 1 |
| MRS | MRS | L | L | L | CODE | X | 1, 3 |
| Read | READ | L | H | H | A | BA | 1, 2 |
| Write | WRITE | L | L | H | A | BA | 1, 2 |
| Auto Refresh | AREF | L | H | L | X | BA | 1 |

Notes:

1. X= Don't Care; H= Logic High; L = Logic Low; A = Valid Address; BA = Valid Bank Address.
2. For the value of "n", see Address Widths at Different Burst Lengths table.
3. Only A0–A17 are used for the MRS command.

State Diagram



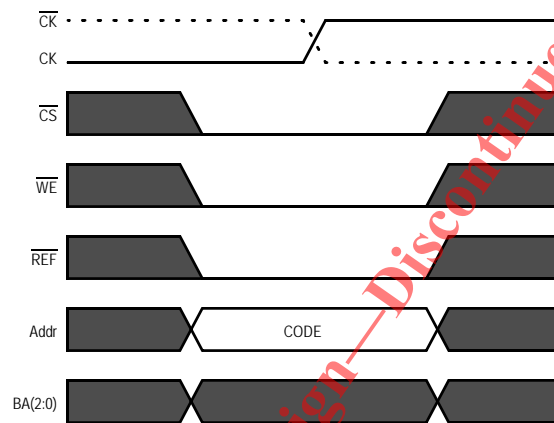
Not Recommended for New Design—Discontinued Product

Mode Register Set

Mode Register Set controls the operating modes of the memory, including configuration, burst length, test mode, and I/O options. During an MRS command, the address inputs A0–A17 are sampled and stored in the Mode Register. Except during initialization to force internal reset, after a valid MRS command, tMRSC must be met before any command except NOP can be issued to the LLDRAM II. All banks must be idle and no bursts may be in progress when an MRS command is loaded.

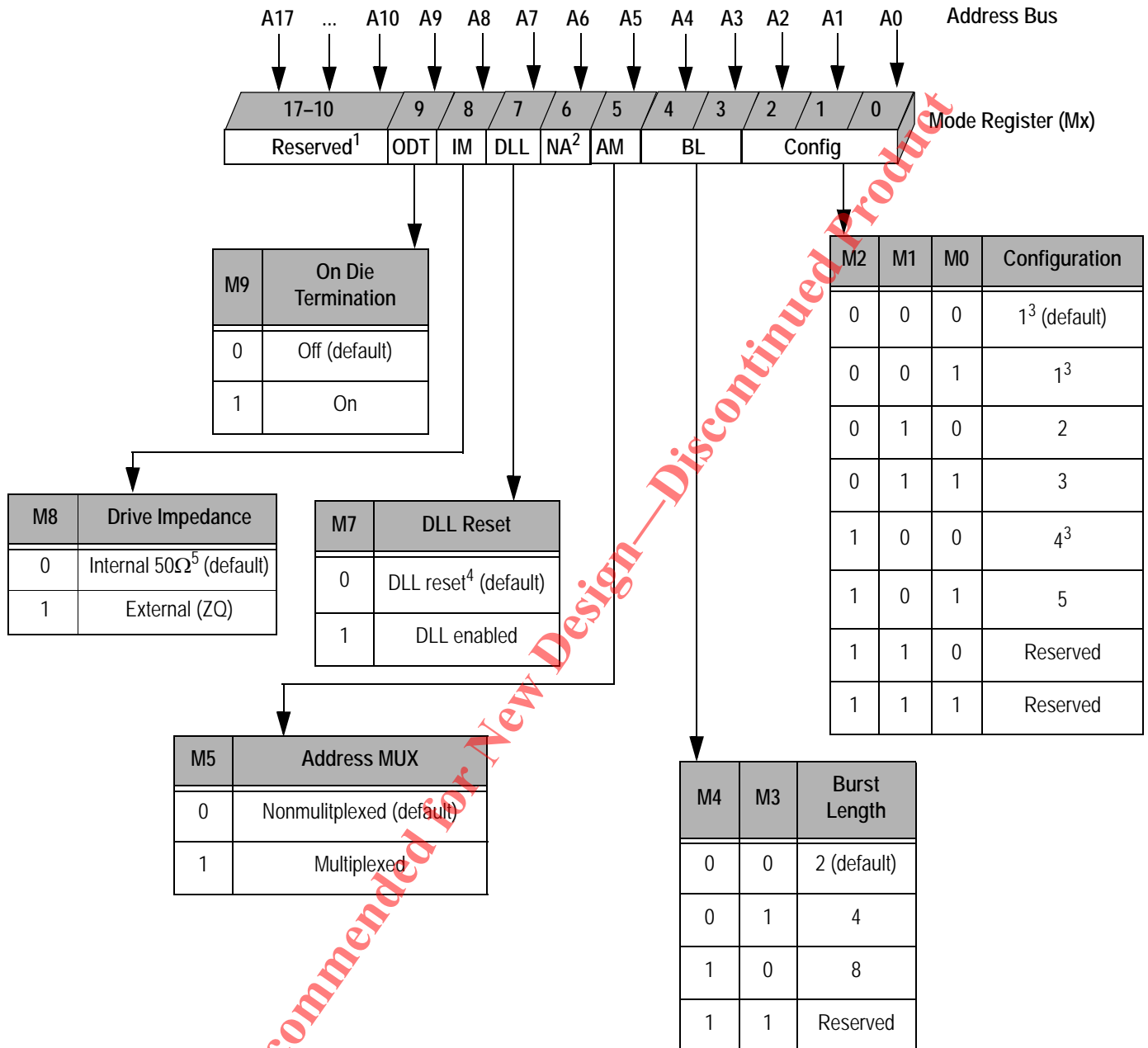
Note: Changing the burst length configuration may scramble previously written data. A burst length change must be assumed to invalidate all stored data.

Mode Register Set



Not Recommended for New Design - Discontinued Product

Mode Register Definition in Nonmultiplexed Address Mode



Notes:

1. A10–A17 must be set to zero; A18–An = “Don’t Care”.
2. A6 not used in MRS.
3. BL = 8 is not available.
4. DLL RESET turns the DLL off.
5. +/-30% over rated temperature range.

Configuration Tables

The relationship between cycle time and read/write latency is selected by the user. The configuration table below lists valid configurations available via Mode Register bits M0, M1, and M2 and the clock frequencies supported for each setting. Write Latency is equal to the Read Latency plus one in each configuration to reduce bus conflicts.

Cycle Time and Read/Write Latency Configuration Table

| Parameter | Configuration | | | | | Units |
|-----------------------|----------------|---------|---------|------------------|---------|-------|
| | 1 ² | 2 | 3 | 4 ^{2,3} | 5 | |
| tRC | 4 | 6 | 8 | 3 | 5 | tCK |
| tRL | 4 | 6 | 8 | 3 | 5 | tCK |
| tWL | 5 | 7 | 9 | 4 | 6 | tCK |
| Valid Frequency Range | 266–175 | 400–175 | 533–175 | 200–175 | 333–175 | MHz |

Notes:

- tRC < 20 ns in any configuration is only available with –18 and –24 speed grades.
- BL= 8 is not available.
- The minimum tRC is typically 3 cycles, except in the case of a Write followed by a Read to the same bank. In this instance the minimum tRC is 4 cycles.

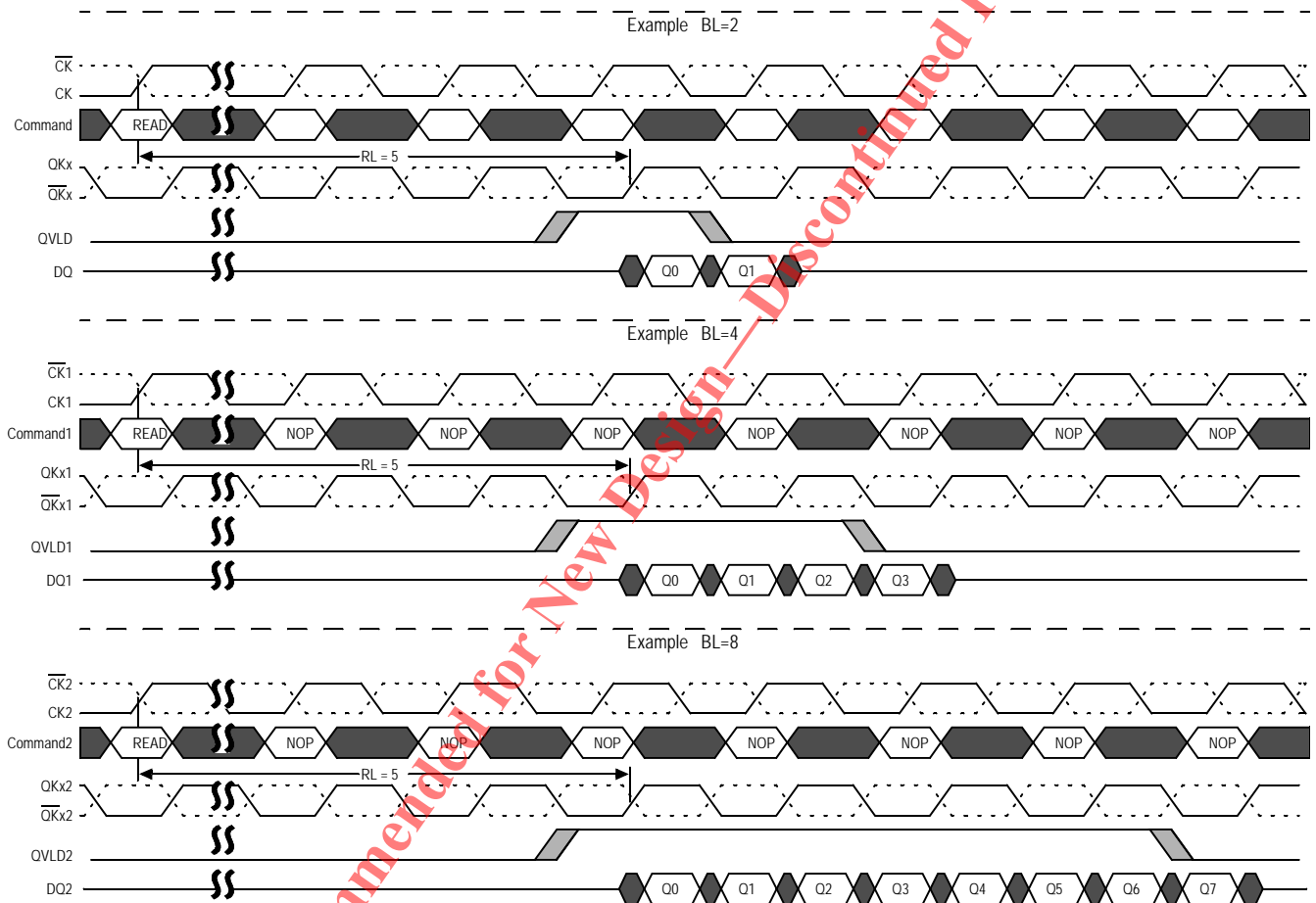
Not Recommended for New Design—Discontinued Product

Burst Length

Read and Write data transfers occur in bursts of 2, 4, or 8 beats. Burst Length is programmed by the user via Mode Register Bit 3 (M3) and Bit 4 (M4). The Read Burst Length diagrams illustrate the different burst lengths with respect to a Read Command. Changes in the burst length affect the width of the address bus.

Note: Changing the burst length configuration may scramble previously written data. A burst length change must be assumed to invalidate all stored data.

Read Burst Lengths



Address Widths at Different Burst Lengths

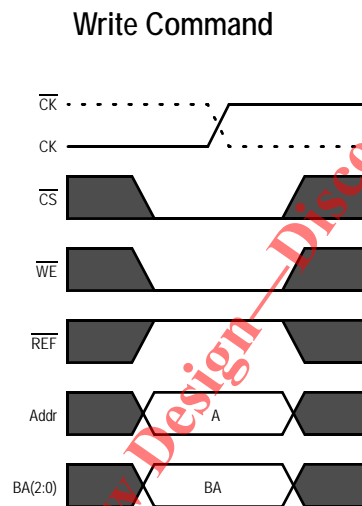
| Burst Length | Configuration | | |
|--------------|---------------|--------|--------|
| | x 9 | x 18 | x36 |
| 2 | A0-A21 | A0-A20 | A0-A19 |
| 4 | A0-A20 | A0-A19 | A0-A18 |
| 8 | A0-A19 | A0-A18 | A0-A17 |

Write

Write data transfers are launched with a Write command, as shown below. A valid address must be provided during the Write command.

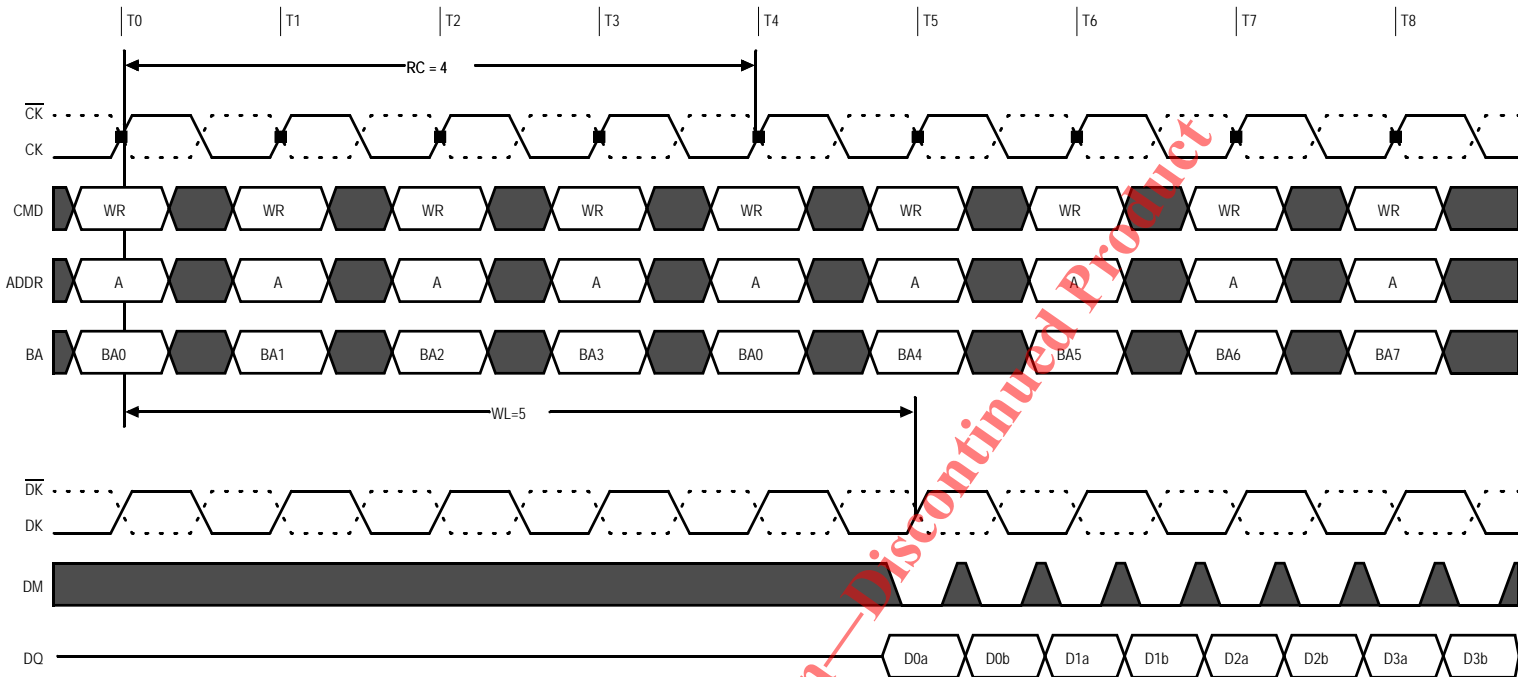
During Write data transfers, each beat of incoming data is registered on crossings of DK and \overline{DK} until the burst transfer is complete. Write Latency (WL) that is always one cycle longer than the programmed Read Latency (RL), so the first valid data registered at the first True crossing of the DK clocks WL cycles after the Write command.

A Write burst may be followed by a Read command (assuming t_{RC} is met). At least one NOP command is required between Write and Read commands to avoid data bus contention. The Write-to-Read timing diagrams illustrate the timing requirements for a Write followed by a Read. Setup and hold times for incoming DQ relative to the DK edges are specified as t_{DS} and t_{DH} . Input data may be masked a High on an associated DM pin. The setup and hold times for the DM signal are t_{DS} and t_{DH} .

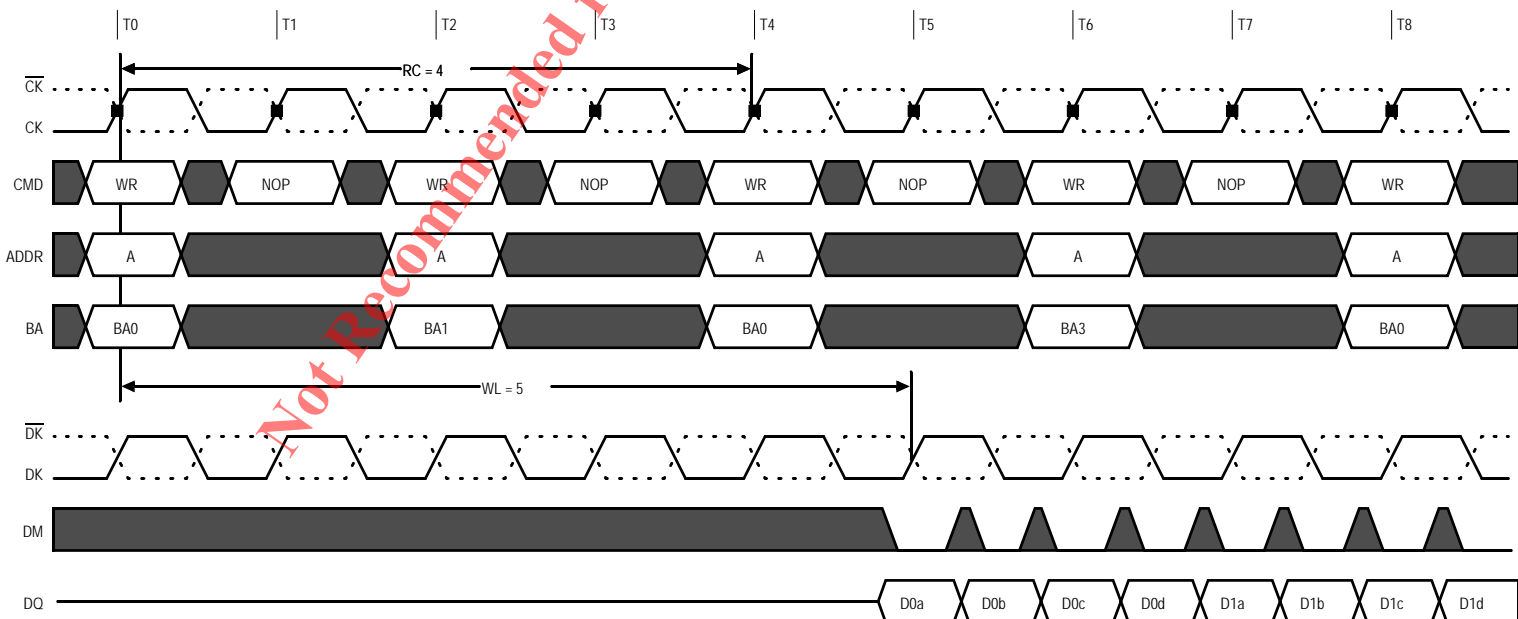


Not Recommended for New Design - Discontinued Product

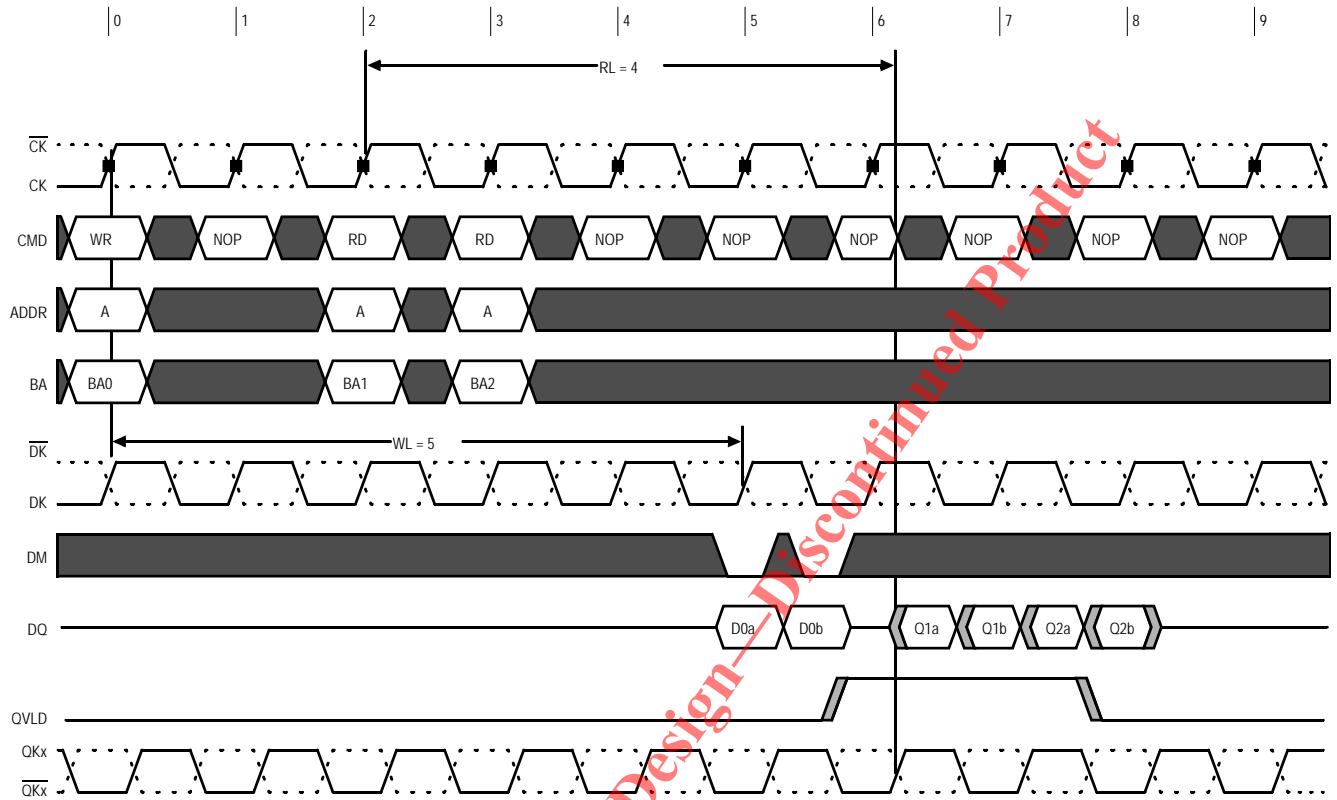
Write Burst Length 2, Configuration 1



Write Burst Length 4, Configuration 1

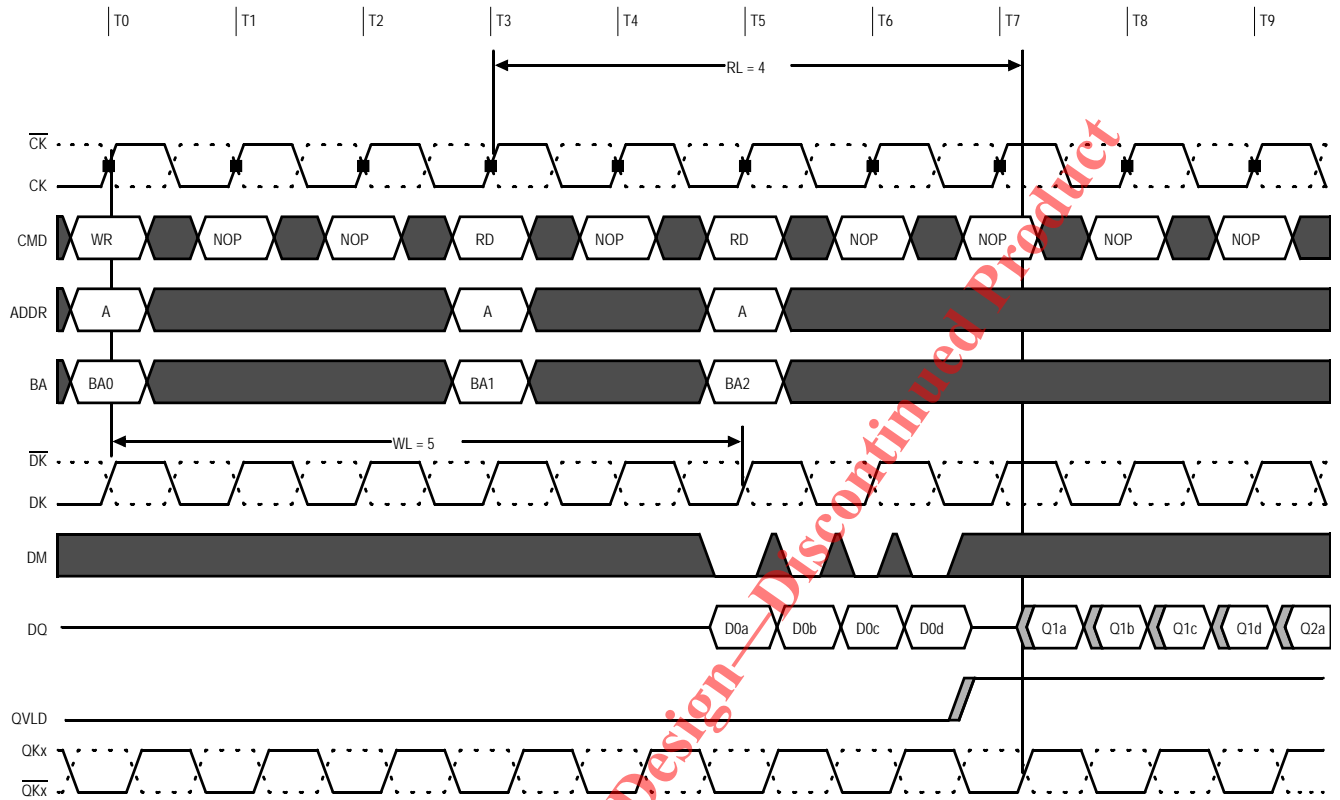


Write-Read Burst Length 2, Configuration 1



Not Recommended for New Design - Discontinued Product

Write-Read Burst Length 4, Configuration 1



Not Recommended for New Design - Discontinued Product

Read

Read data transfers are launched with a Read command, as shown below. Read Addresses must provided with the Read command.

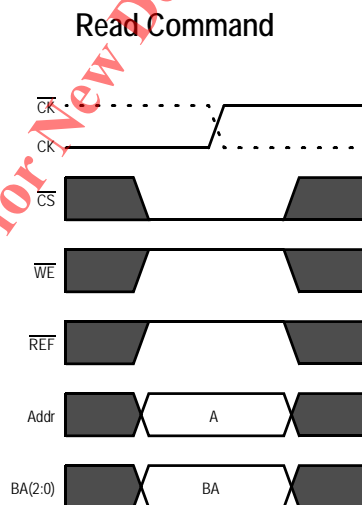
Each beat of a Read data transfer is edge-aligned with the QK_x signals. After a programmable Read Latency, data is available at the outputs. One half clock cycle prior to valid data on the read bus, the data valid signal (QVLD) is driven High. QVLD is also edge-aligned with the QK_x signals. The QK clocks are free-running.

The skew between QK and the crossing point of CK is specified as t_{CKQK} . t_{QKQ0} is the skew between QK0 and the last valid data edge generated at the DQ signals associated with QK0 (t_{QKQ0} is referenced to DQ0–DQ17 for the x36 configuration and DQ0–DQ8 for the x18 configuration). t_{QKQ1} is the skew between QK1 and the last valid data edge generated at the DQ signals associated with QK1 (t_{QKQ1} is referenced to DQ18–DQ35 for the x36 and DQ9–DQ17 for the x18 configuration). t_{QKQx} is derived at each QK_x clock edge and is not cumulative over time. t_{QKQ} is defined as the skew between either QK differential pair and any output data edge.

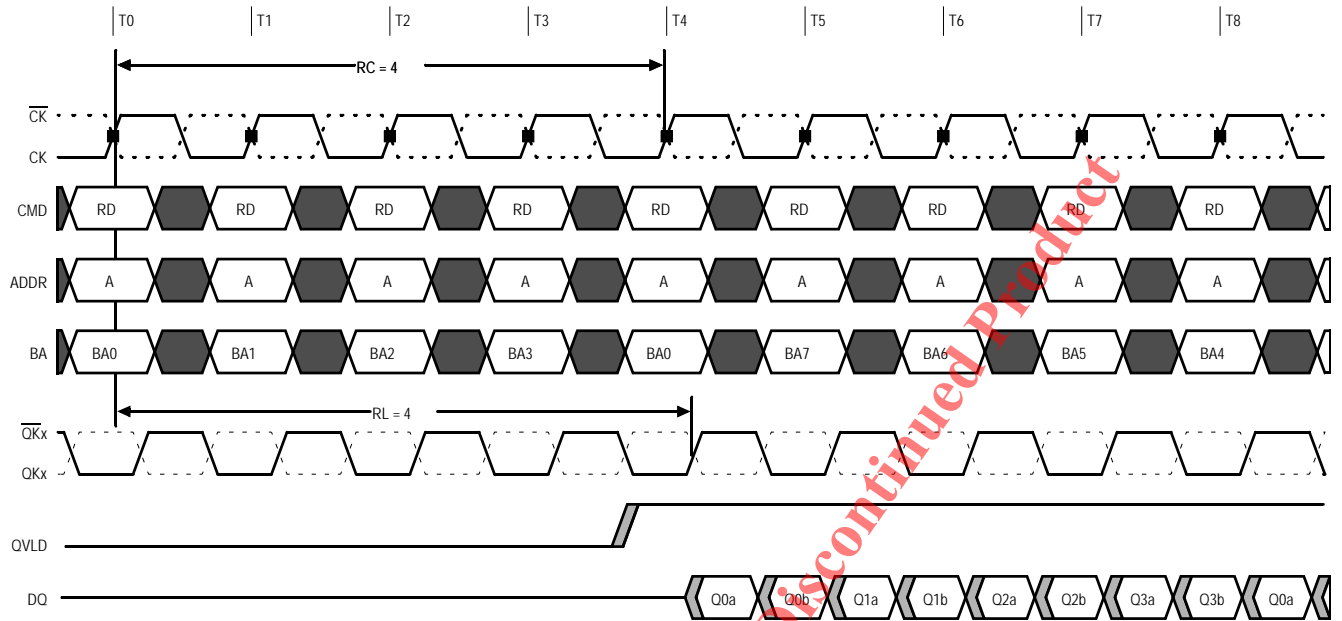
At the end of a burst transfer, assuming no other commands have been initiated, output data (DQ) will go High-Z. The QVLD signal transitions Low on the beat of a Read burst. Note that if CK/\overline{CK} violates the $V_{ID(DC)}$ specification while a Read burst is occurring, QVLD remains High until a dummy Read command is issued. Back-to-back Read commands are possible, producing a continuous flow of output data.

The data valid window specification is referenced to QK transitions and is defined as: $t_{QHP} - (t_{QKQ} [MAX] + |t_{QKQ} [MIN]|)$. See the Read Data Valid Window section for illustration.

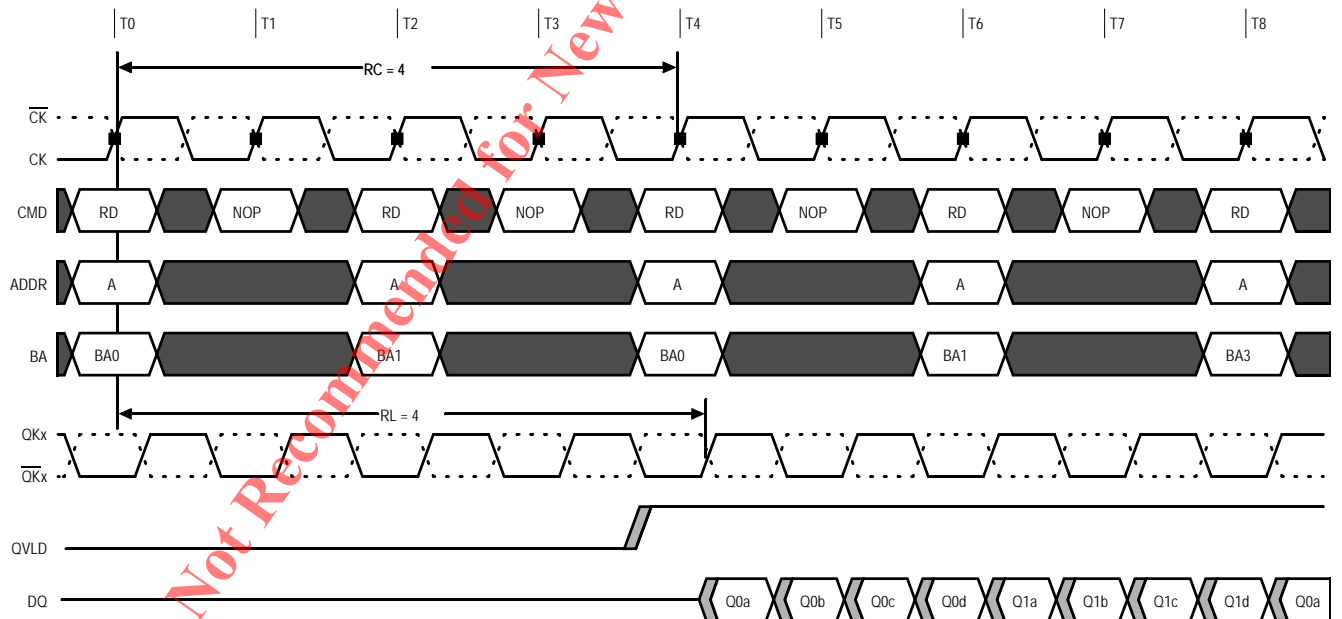
Any Read transfer may be followed by a subsequent Write command. The Read-to-Write timing diagram illustrates the timing requirements for a Read followed by a Write. Some systems having long line lengths or severe skews may need additional NOP cycles inserted between Read and Write commands to prevent data bus contention.



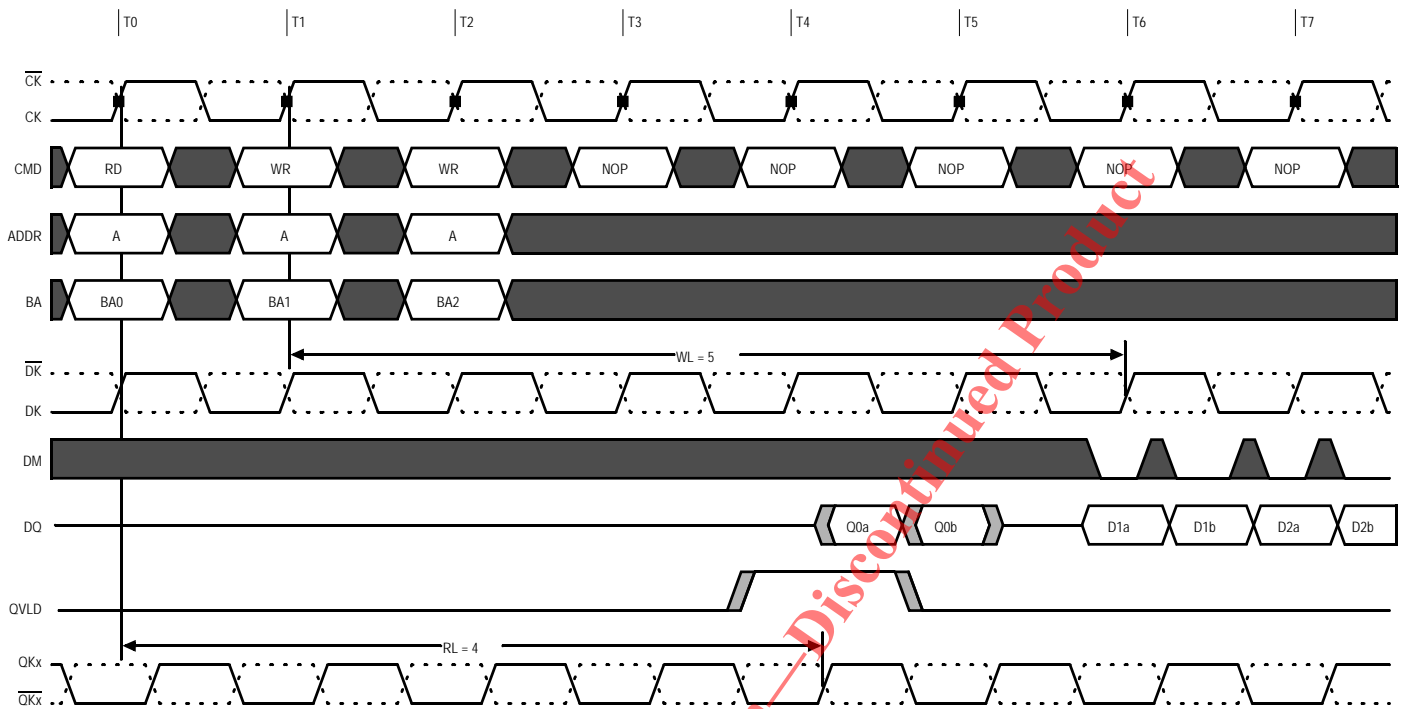
Read Burst Length 2, Configuration 1



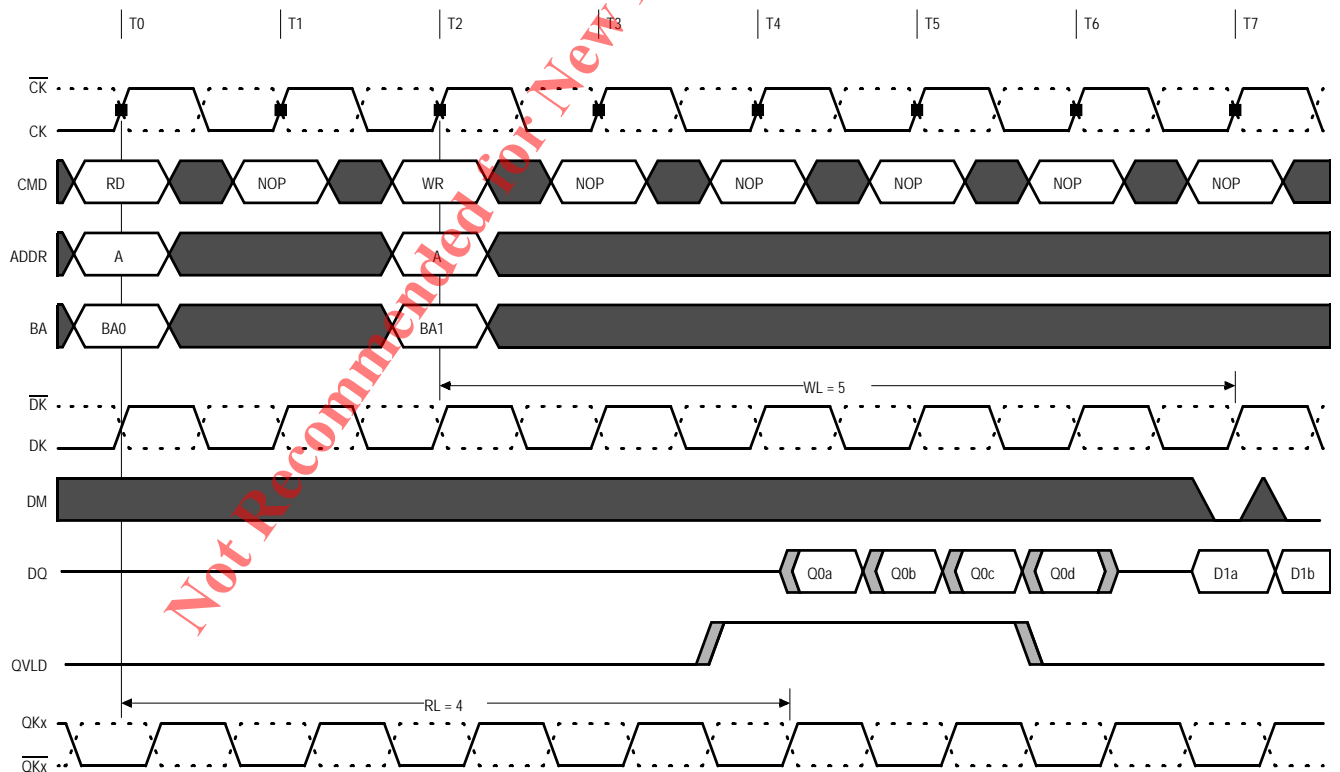
Read Burst Length 4, Configuration 1



Read-Write Burst Length 2, Configuration 1



Read-Write Burst Length 4, Configuration 1

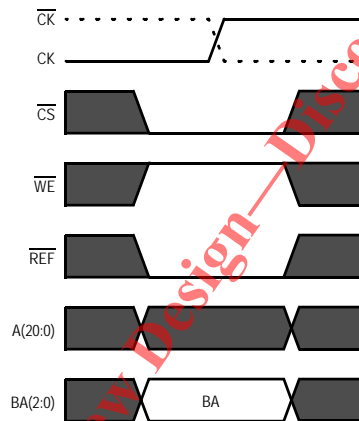


Auto Refresh

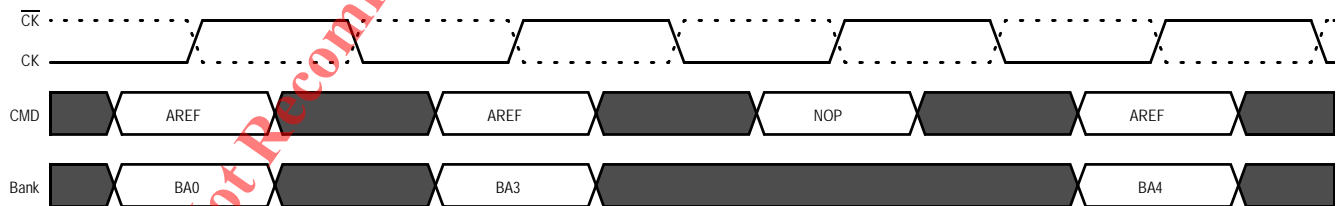
The Auto Refresh (AREF) command launches a REFRESH cycle on one row in the bank addressed. Refresh row addresses are generated by an internal refresh counter, so address inputs are Don't Care, but a bank addresses (BA 2:0) must be provided during the AREF command. A refresh may be continuing in one bank while other commands, including other AREF commands, are launched in other banks. The delay between the AREF command and a READ, WRITE or AREF command to the same bank must be at least t_{RC} .

The entire memory must be refreshed every 32 ms (t_{REF}). This means that this 576Mb device requires 128K refresh cycles at an average periodic interval of 0.24 μ s MAX (actual periodic refresh interval is 32 ms/16K rows/8 = 0.244 μ s). To improve efficiency, eight AREF commands (one for each bank) can be launched at periodic intervals of 1.95 μ s (32 ms/16K rows = 1.95 μ s). The Auto Refresh Cycle diagram illustrates an example of a refresh sequence.

Auto Refresh (AREF) Command



Auto Refresh Cycle



Address Multiplexing

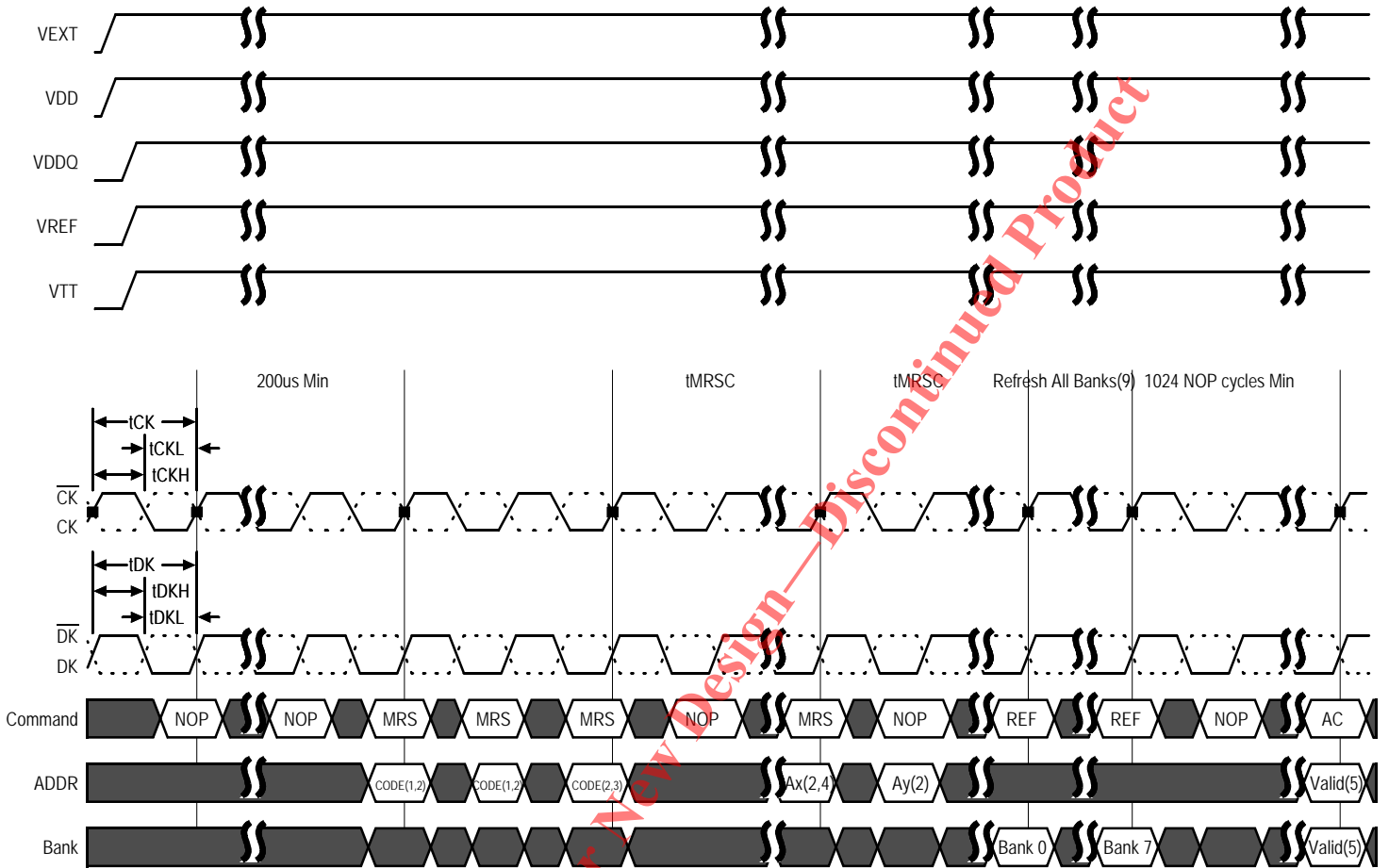
LLDRAM II defaults to “broadside” addressing at power up, meaning, it registers all address inputs on a single clock transition. However, for most configurations of the device, considerable efficiency can be gained by operating in Address Multiplexed mode, cutting the address pin count on the host device in half. In Multiplexed Address mode, the address is loaded in two consecutive clock transitions. Broadside Addressing only improves Continuous Burst mode data transfer efficiency of Burst Length 2 (BL = 2) configuration.

In Address Multiplex mode, bank addresses are loaded on the same clock transition as Command and the first half of the address, A_x . The 576Mb Address Mapping in Multiplexed Address Mode table and Cycle Time and Read/Write Latency Configuration in Multiplexed Mode table show the addresses needed for both the first and second clock transitions (A_x and A_y , respectively). The AREF command does not require an address on the second clock transition, as only the Bank Address are loaded for refresh commands. Therefore, AREF commands may be issued on consecutive clocks, even when in Address Multiplex mode.

Setting Mode Register Bit 5 (M5) to 1 in the Mode Register activates the Multiplexed Address mode. Once this bit is set subsequent MRS, READ, and WRITE operate as described in the Multiplexed Address Mode diagram.

Not Recommended for New Design—Discontinued Product

Power-Up Multiplexed Address Mode



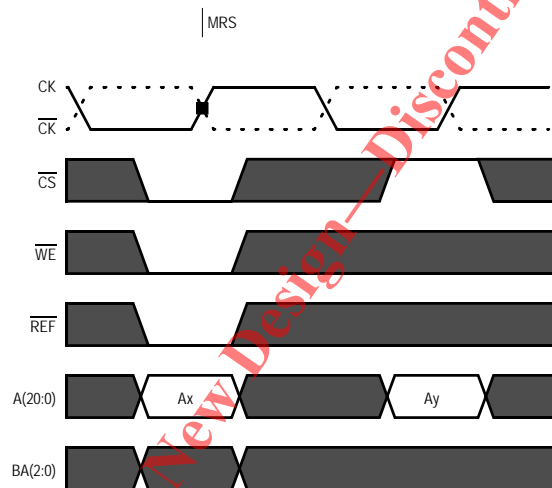
Not Recommended for New Design - Discontinued Product

MRS Command In Multiplexed Mode

The Mode Register Set command stores the data for controlling the RAM into the Mode Register. The register allows the user to modify Read and Write pipeline length, burst length, test mode, and I/O options. The Multiplexed MRS command requires two cycles to complete. The A_x address is sampled on the true crossing of clock with the MRS Command. The A_y address and a required NOP command are captured on the next next crossing of clock. After issuing a valid MRS command, t_{MRSC} must be met before any READ, WRITE, MRS, or AREF command can be issued to the LLDRAM II. This statement does not apply to the consecutive MRS commands needed for internal logic reset during the initialization routine. The MRS command can only be issued when all banks are idle and no bursts are in progress.

Note: The data written by the prior burst length is not guaranteed to be accurate when the burst length of the device is changed.

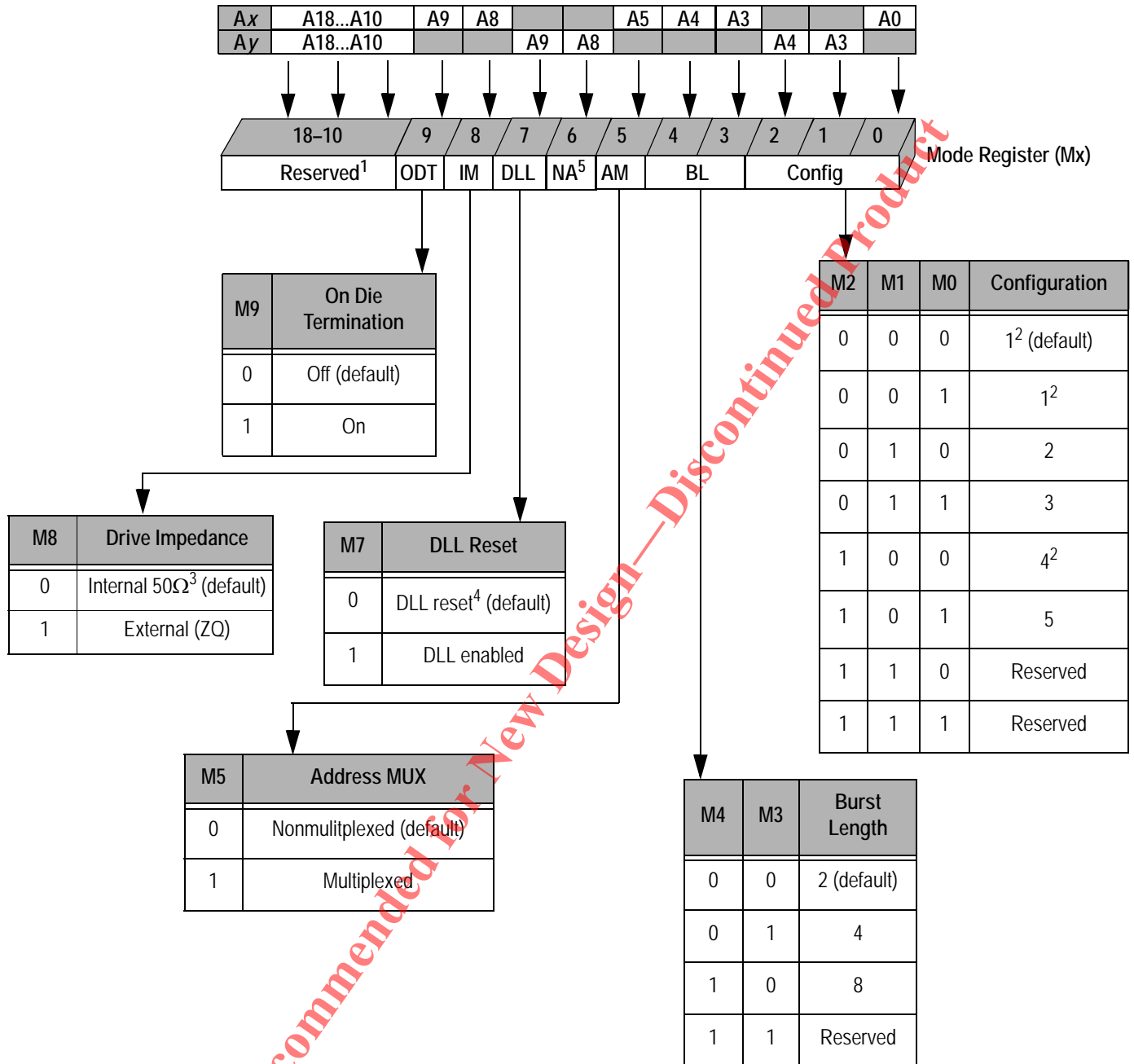
MRS Command in Multiplexed Mode



Notes:

1. Recommended that all address pins held Low during dummy MRS commands.
2. A10–A18 must be Low.
3. Set address A5 High. This enables the part to enter Multiplexed Address mode when in Non-Multiplexed mode operation. Multiplexed Address mode can also be entered at some later time by issuing an MRS command with A5 High. Once address Bit A5 is set High, t_{MRSC} must be satisfied before the two-cycle multiplexed mode MRS command is issued.
4. Address A5 must be set High. This and the following step set the desired mode register once the LLDRAM II is in Multiplexed Address mode.
5. Any command or address.
6. The above sequence must be followed in order to power up the LLDRAM II in the Multiplexed Address mode.
7. DLL must be reset if t_{CK} or V_{DD} are changed.
8. CK and \overline{CK} must be separated at all times to prevent bogus commands from being issued.
9. The sequence of the eight AUTO REFRESH commands (with respect to the 1024 NOP commands) does not matter. As is required for any operation, t_{RC} must be met between an AUTO REFRESH command and a subsequent VALID command to the same bank.

Mode Register Definition in Multiplexed Address Mode



Notes:

1. A10–A18 must be set to zero.
2. BL = 8 is not available.
3. +/-30% over rated temperature range.
4. DLL RESET turns the DLL off.
5. Ay8 not used in MRS.
6. BA0–BA2 are "Don't Care".
7. Addresses A0, A3, A4, A5, A8, and A9 must be set as shown in order to activate the Mode Register in the Multiplexed Address mode.

576Mb Address Mapping in Multiplexed Address Mode

| Data Width | Burst Length | Ball | Address | | | | | | | | | | |
|------------|--------------|------|---------|----|----|-----|----|----|-----|-----|-----|-----|-----|
| | | | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| x36 | 2 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | X | A1 | A2 | X | A6 | A7 | A19 | A11 | A12 | A16 | A15 |
| | 4 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | X | A1 | A2 | X | A6 | A7 | X | A11 | A12 | A16 | A15 |
| | 8 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | X |
| | | Ay | X | A1 | A2 | X | A6 | A7 | X | A11 | A12 | A16 | A15 |
| x18 | 2 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | A20 | A1 | A2 | X | A6 | A7 | A19 | A11 | A12 | A16 | A15 |
| | 4 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | X | A1 | A2 | X | A6 | A7 | A19 | A11 | A12 | A16 | A15 |
| | 8 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | X | A1 | A2 | X | A6 | A7 | X | A11 | A12 | A16 | A15 |
| x9 | 2 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | A20 | A1 | A2 | A21 | A6 | A7 | A19 | A11 | A12 | A16 | A15 |
| | 4 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | A20 | A1 | A2 | X | A6 | A7 | A19 | A11 | A12 | A16 | A15 |
| | 8 | Ax | A0 | A3 | A4 | A5 | A8 | A9 | A10 | A13 | A14 | A17 | A18 |
| | | Ay | X | A1 | A2 | X | A6 | A7 | A19 | A11 | A12 | A16 | A15 |

Notes:

X= Don't Care.

Configuration in Multiplexed Mode

In Multiplexed Address mode, the Read and Write latencies are increased by one clock cycle. However, the LLDRAM II cycle time remains the same as when in Nonmultiplexed Address mode.

Cycle Time and Read/Write Latency Configuration in Multiplexed Mode

| Parameter | Configuration | | | | | Units |
|-----------------------|----------------|---------|---------|------------------|---------|-------|
| | 1 ² | 2 | 3 | 4 ^{2,3} | 5 | |
| tRC | 4 | 6 | 8 | 3 | 5 | tCK |
| tRL | 5 | 7 | 9 | 4 | 6 | tCK |
| tWL | 6 | 8 | 10 | 5 | 7 | tCK |
| Valid Frequency Range | 266–175 | 400–175 | 533–175 | 200–175 | 333–175 | MHz |

Notes:

- tRC < 20 ns in any configuration is only available with –24 and –18 speed grades.
- Minimum operating frequency for –18 is 370 MHz.
- The minimum tRC is typically 3 cycles, except in the case of a Write followed by a Read to the same bank. In this instance the minimum tRC is 4 cycles.

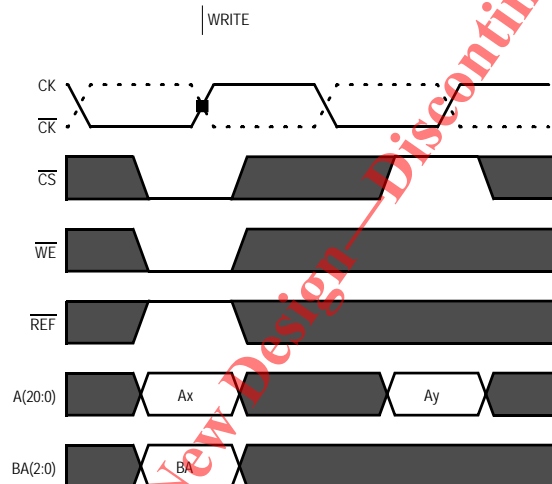
Write Command in Multiplexed Mode

Address Multiplexed Write data transfers are launched with a Write command, as shown below. A valid address must be provided during the Write command. The Ax address must be loaded on the same true clock crossing used to load the Write command and the Bank address. The Ay address and a NOP command must be provided at the next clock crossing.

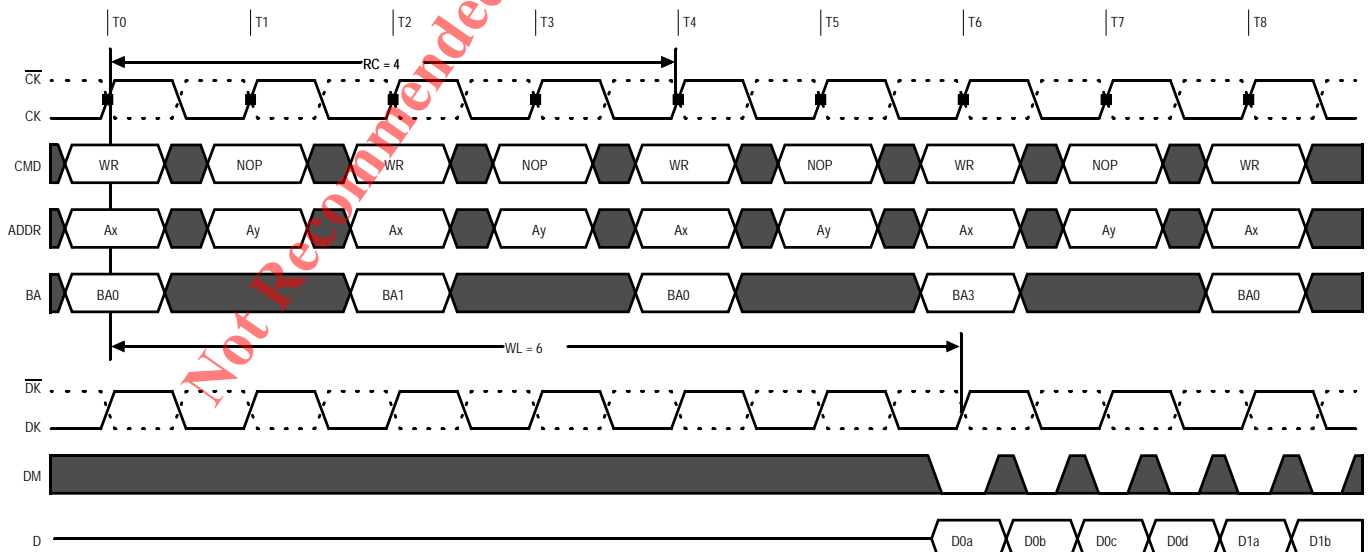
During Write data transfers, each beat of incoming data is registered on crossings of DK and \overline{DK} until the burst transfer is complete. Write Latency (WL) is always one cycle longer than the programmed Read Latency (RL).

A Write burst may be followed by a Read command (assuming tRC is met). At least one NOP command is required between Write and Read commands to avoid data bus contention. The Write-to-Read timing diagrams illustrate the timing requirements for a Write followed by a Read. Setup and hold times for incoming DQ relative to the DK edges are specified as tDS and tDH. Input data may be masked high on an associated DM pin. The setup and hold times for the DM signal are tDS and tDH.

Write Command in Multiplexed Mode



Write Burst Length 4, Configuration 1 in Multiplexed Mode



Read Command in Multiplexed Mode

Address Multiplexed Read data transfers are launched with a Read command, as shown below. A valid address must be provided during the READ command. The A_x address must be loaded on the same True clock crossing used to load the READ command and the Bank address. The A_y address and a NOP command must be provided at the next clock crossing.

Each beat of a Read data transfer is edge-aligned with the QK_x signals. After a programmable Read Latency, data is available at the outputs. One half clock cycle prior to valid data on the read bus, the data valid signal (QVLD) is driven High. QVLD is also edge-aligned with the QK_x signals. The QK clocks are free-running.

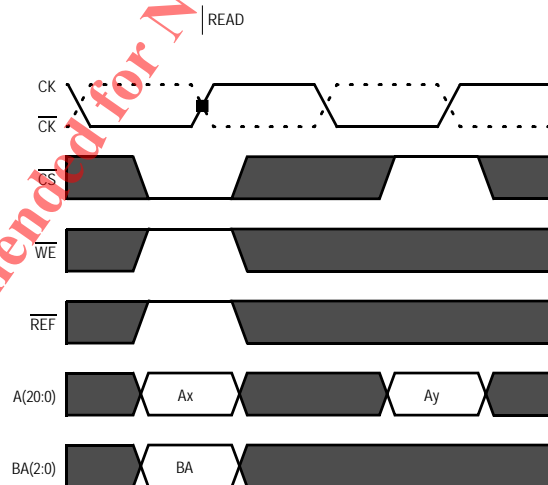
The skew between QK and the crossing point of CK is specified as t_{CKQK} . t_{QKQ0} is the skew between $QK0$ and the last valid data edge generated at the DQ signals associated with $QK0$ (t_{QKQ0} is referenced to $DQ0$ – $DQ17$ for the x36 configuration and $DQ0$ – $DQ8$ for the x18 configuration). t_{QKQ1} is the skew between $QK1$ and the last valid data edge generated at the DQ signals associated with $QK1$ (t_{QKQ1} is referenced to $DQ18$ – $DQ35$ for the x36 and $DQ9$ – $DQ17$ for the x18 configuration). t_{QKQ_x} is derived at each QK_x clock edge and is not cumulative over time. t_{QKQ} is defined as the skew between either QK differential pair and any output data edge.

At the end of a burst transfer, assuming no other commands have been initiated, output data (DQ) will go High-Z. The QVLD signal transitions Low on the beat of a Read burst. Note that if CK/\overline{CK} violates the $V_{ID(DC)}$ specification while a Read burst is occurring, QVLD remains High until a dummy Read command is issued. Back-to-back Read commands are possible, producing a continuous flow of output data.

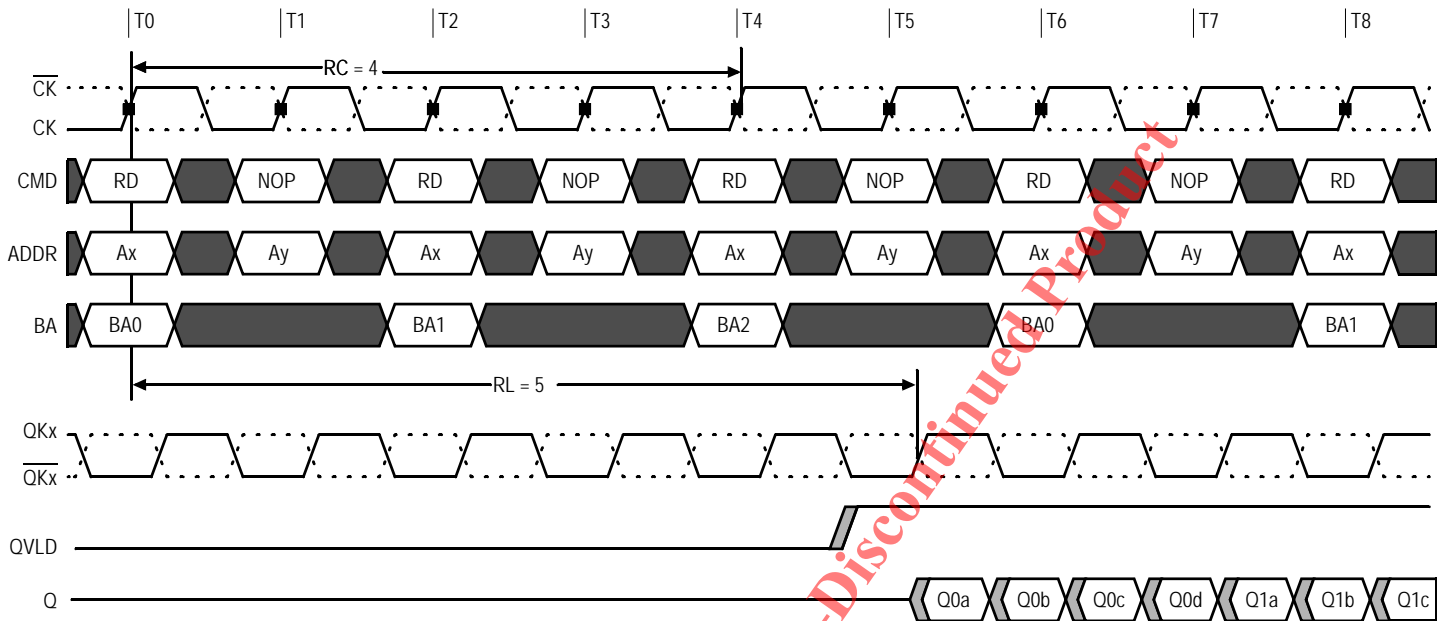
The data valid window specification is referenced to QK transitions and is defined as: $t_{QHP} - (t_{QKQ} [MAX] + |t_{QKQ} [MIN]|)$. See the Read Data Valid Window section.

Any Read transfer may be followed by a subsequent Write command. The Read-to-Write timing diagram illustrates the timing requirements for a Read followed by a Write. Some systems having long line lengths or severe skews may need additional NOP cycles inserted between Read and Write commands to prevent data bus contention.

Read Command in Multiplexed Mode



Read Burst Length 4, Configuration 1 in Multiplexed Mode



Not Recommended for New Design—Discontinued Product

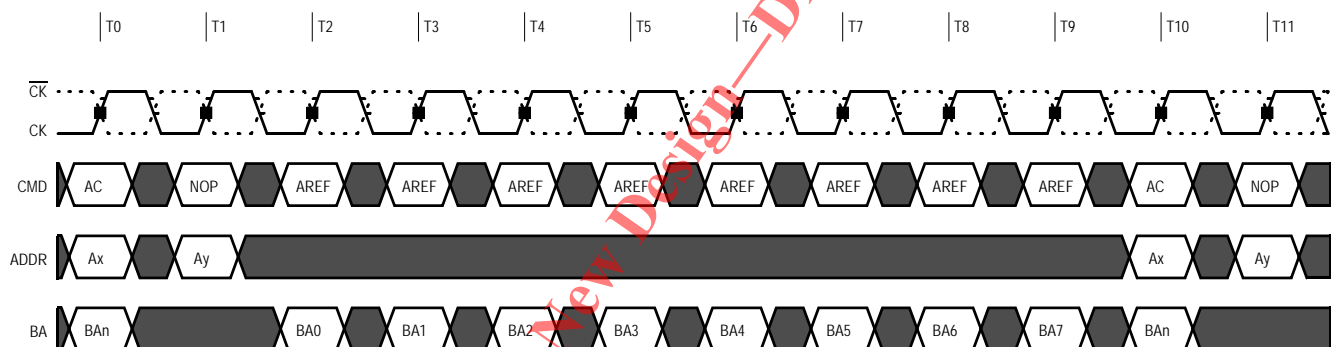
Refresh Commands in Multiplexed Address Mode

The AREF command launches a REFRESH cycle on one row in the bank addressed. Refresh row addresses are generated by an internal refresh counter, so address inputs are Don't Care, but Bank addresses (BA 2:0) must be provided during the AREF command. A refresh may be continuing in one bank while other commands, including other AREF commands, are launched in other banks. The delay between the AREF command and a READ, WRITE or AREF command to the same bank must be at least t_{RC} .

The entire memory must be refreshed every 32 ms (t_{REF}). This means that this 576Mb device requires 128K refresh cycles at an average periodic interval of 0.24 μ s MAX (actual periodic refresh interval is 32 ms/16K rows/8 = 0.244 μ s). To improve efficiency, eight AREF commands (one for each bank) can be launched at periodic intervals of 1.95 μ s (32 ms/16K rows = 1.95 μ s). The Auto Refresh Cycle diagram illustrates an example of a refresh sequence.

Unlike READ and WRITE commands in Address Multiplex mode, all the information needed to execute an AREF command (the AREF command and the Band Address (BA 2:0)) is loaded in a single clock crossing, another AREF command (to a different bank) may be loaded on the next clock crossing.

Consecutive Refresh Operations with Multiplexed Mode



Notes:

1. Any command.
2. Bank n is chosen so that t_{RC} is met.

Absolute Maximum Ratings

Absolute Maximum Voltage

(All voltages reference to V_{SS})

| Parameter | Min | Max | Unit |
|--|------|-----------------|------|
| I/O Voltage | -0.3 | $V_{DDQ} + 0.3$ | V |
| Voltage on V_{EXT} supply | -0.3 | +2.8 | V |
| Voltage on V_{DD} supply relative to V_{SS} | -0.3 | +2.1 | V |
| Voltage on V_{DDQ} supply relative to V_{SS} | -0.3 | +2.1 | V |

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Absolute Maximum Temperature

| Parameter | Temperature Range | Symbol | Min. | Max. | Unit | Notes |
|----------------------------------|-------------------|-----------|------|------|------|-------|
| Storage Temperature | — | T_{STG} | -55 | +150 | C° | 1 |
| Reliability junction temperature | Commercial | T_J | — | +110 | C° | 2 |
| | Industrial | | — | +110 | C° | 2 |

Notes:

1. Max storage case temperature; T_{STG} is measured in the center of the package.
2. Temperatures greater than 110 C° may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or above this is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect reliability of the part.

Not Recommended for New Design - Discontinued Product

Recommended Operating Temperature and Thermal Impedance

Like any other semiconductor device, the LLD RAM II must be operated within the temperature specifications shown in the Temperature Limits table for the device to meet datasheet specifications. The thermal impedance characteristics of the device are listed below. In applications where the ambient temperature or PCB temperature are too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Temperature Limits

| Parameter | Temperature Range | Symbol | Min. | Max. | Unit | Notes |
|--------------------------------|-------------------|--------|------|------|------|---------|
| Operating junction temperature | Commercial | T_J | 0 | +100 | C° | 1 |
| | Industrial | | -40 | +100 | C° | 1 |
| Operating case temperature | Commercial | T_C | 0 | +95 | C° | 2, 3 |
| | Industrial | | -40 | +95 | C° | 2, 3, 4 |

Notes:

1. Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.
2. Maximum operating case temperature, T_C , is measured in the center of the package.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Junction and case temperature specifications must be satisfied.

Thermal Impedance

| Package | Test PCB Substrate | θ_{JA} (C°/W) Airflow = 0 m/s | θ_{JA} (C°/W) Airflow = 1 m/s | θ_{JA} (C°/W) Airflow = 2 m/s | θ_{JB} (C°/W) | θ_{JC} (C°/W) |
|-----------|--------------------|---|---|---|----------------------|----------------------|
| μ BGA | 2-layer | TBD | TBD | TBD | TBD | TBD |
| | 4-layer | 22.4 | 19.0 | 16.2 | 5.3 | 1.7 |

Notes:

1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. The minimal metalization of a 2-layer board tends to minimize the utility of the junction-to-board heat path. The 4-layer test fixture PCB is intended to highlight the effect of connection to power planes typically found in the PCBs used in most applications. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Recommended DC Operating Conditions and Electrical Characteristics

| Description | Conditions | Symbol | Min. | Max. | Unit | Notes |
|-------------------------------|--------------------------------|--------------|-----------------------------|-----------------------------|---------|-----------|
| Supply Voltage | — | V_{EXT} | 2.38 | 2.63 | V | — |
| Supply Voltage | — | V_{DD} | 1.7 | 1.9 | V | 2 |
| Isolated Output Buffer Supply | — | V_{DDQ} | 1.4 | V_{DD} | V | 2, 3 |
| Reference Voltage | — | V_{REF} | $0.49 * V_{DDQ}$ | $0.51 * V_{DDQ}$ | V | 4, 5, 6 |
| Termination Voltage | — | V_{TT} | $0.95 * V_{REF}$ | $1.05 * V_{REF}$ | V | 7, 8 |
| Input High (logic 1) voltage | — | $V_{IH(DC)}$ | $V_{REF} + 0.1$ | $V_{DDQ} + 0.3$ | V | 2 |
| Input Low (logic 0) voltage | — | $V_{IL(DC)}$ | $V_{SS} - 0.3$ | $V_{REF} - 0.1$ | V | 2 |
| Output High Current | $V_{OUT} = V_{DDQ}/2$ | I_{OH} | $(V_{DDQ}/2)/(1.15 * RQ/5)$ | $(V_{DDQ}/2)/(0.85 * RQ/5)$ | A | 9, 10, 11 |
| Output Low Current | $V_{OUT} = V_{DDQ}/2$ | I_{OL} | $(V_{DDQ}/2)/(1.15 * RQ/5)$ | $(V_{DDQ}/2)/(0.85 * RQ/5)$ | A | 9, 10, 11 |
| Clock Input Leakage Current | $0 V \leq V_{IN} \leq V_{DD}$ | I_{LC} | -5 | 5 | μA | — |
| Input Leakage Current | $0 V \leq V_{IN} \leq V_{DD}$ | I_{LI} | -5 | 5 | μA | — |
| Output Leakage Current | $0 V \leq V_{IN} \leq V_{DDQ}$ | I_{LO} | -5 | 5 | μA | — |
| Reference Voltage Current | — | I_{REF} | -5 | 5 | μA | — |

Notes:

- All voltages referenced to V_{SS} (GND). This note applies to the entire table.
- Overshoot $V_{IH(AC)} \leq V_{DD} + 0.7 V$ for $t \leq t_{CK}/2$. Undershoot $V_{IL(AC)} \geq -0.5 V$ for $t \leq t_{CK}/2$. During normal operation V_{DDQ} must not exceed V_{DD} . Control input signals may not have pulse widths less than $t_{CK}/2$ or operate at frequencies exceeding t_{CK} (MAX).
- V_{DDQ} can be set to a nominal $1.5 V \pm 0.1 V$ or $1.8 V \pm 0.1 V$ supply.
- Typically the value of V_{REF} is expected to be $0.5 * V_{DDQ}$ of the transmitting device. V_{REF} is expected to track variations in V_{DDQ} .
- Peak-to-Peak AC noise on V_{REF} must not exceed $\pm 2\%$ of $V_{REF(DC)}$.
- V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed $\pm 2\%$ of the DC value. Thus, from $V_{DDQ}/2$, V_{REF} is allowed $\pm 2\% V_{DDQ}/2$ for DC error and an additional $\pm 2\% V_{DDQ}/2$ for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF} .
- On-die termination may be selected using Mode Register Bit 9 (M9). A resistance R_{TT} from each data input signal to the nearest V_{TT} can be enabled. $R_{TT} = 125\Omega - 185\Omega$ at $95^\circ C T_C$.
- I_{OH} and I_{OL} are defined as absolute values and are measured at $V_{DDQ}/2$. I_{OH} flows from the device, I_{OL} flows into the device.
- If Mode Register Bit 8 (M8) is 0, use $RQ = 250\Omega$ in the equation in lieu of presence of an external impedance matched resistor.
- For V_{OL} and V_{OH} , refer to the LLDRAM II IBIS models.

DC Differential Input Clock Logic Levels

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|---------------------|------|------------------------|------|-------|
| Clock input voltage level: CK and $\overline{\text{CK}}$ | $V_{\text{IN(DC)}}$ | -0.3 | $V_{\text{DDQ}} + 0.3$ | V | 1-4 |
| Clock input differential voltage: CK and $\overline{\text{CK}}$ | $V_{\text{ID(DC)}}$ | 0.2 | $V_{\text{DDQ}} + 0.6$ | V | 1-5 |

Notes:

1. $\overline{\text{DKx}}$ and $\overline{\text{DKx}}$ have the same requirements as CK and $\overline{\text{CK}}$.
2. All voltages referenced to V_{SS} (GND).
3. The CK and $\overline{\text{CK}}$ input reference level (for timing referenced to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The input reference level for signals other than CK/ $\overline{\text{CK}}$ is V_{REF} .
4. The CK and $\overline{\text{CK}}$ input slew rate must be ≥ 2 V/ns (≥ 4 V/ns if measured differentially).
5. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.

Recommended AC Operating Conditions and Electrical Characteristics

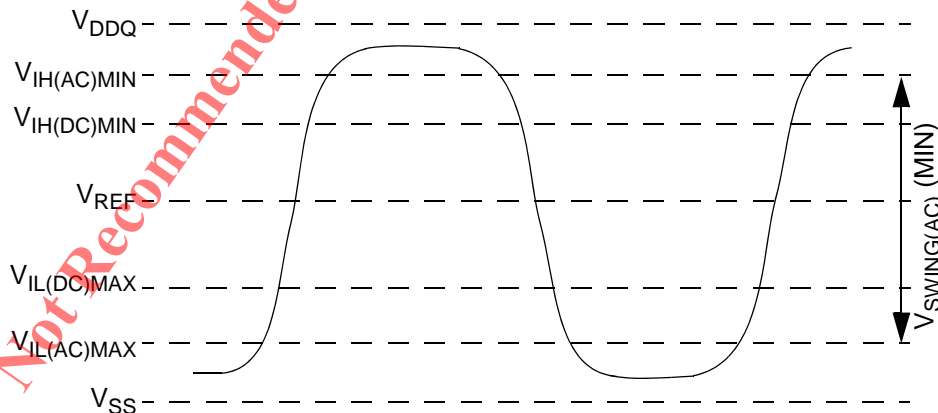
Input AC Logic Levels

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|------------------------------|-----------------|------------------------|------------------------|------|---------|
| Input High (logic 1) Voltage | V_{IH} | $V_{\text{REF}} + 0.2$ | — | V | 1, 2, 3 |
| Input Low (logic 0) Voltage | V_{IL} | — | $V_{\text{REF}} - 0.2$ | V | 1, 2, 3 |

Notes:

1. All voltages referenced to V_{SS} (GND).
2. The AC and the DC input level specifications are defined in the HSTL standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (see drawing below) the DC input Low (High) level).
3. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{\text{IL(AC)}}$ and $V_{\text{IH(AC)}}$.

Nominal t_{AS} / t_{CS} / t_{DS} and t_{AH} / t_{CH} / t_{DH} Slew Rate



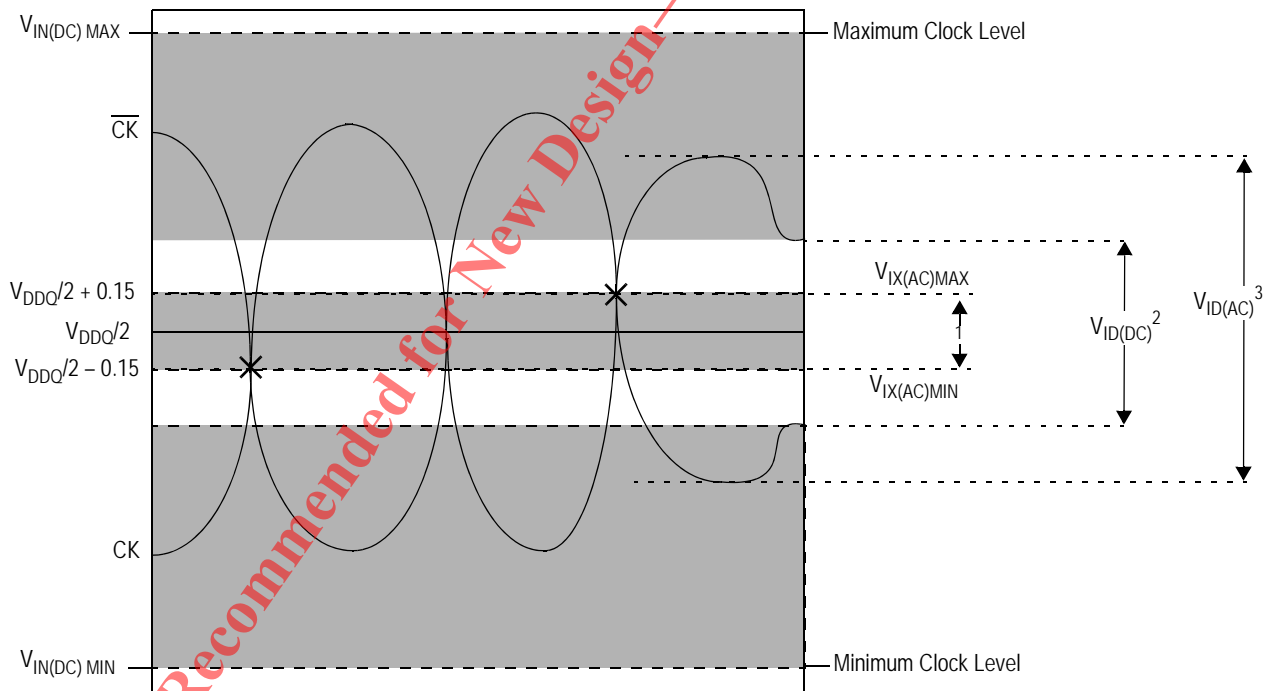
AC Differential Input Clock Levels

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|---------------------|---------------------------|---------------------------|------|--------|
| Clock input differential voltage: CK and $\overline{\text{CK}}$ | $V_{\text{ID(AC)}}$ | 0.4 | $V_{\text{DDQ}} + 0.6$ | V | 1-5 |
| Clock input crossing point voltage: CK and $\overline{\text{CK}}$ | $V_{\text{IX(AC)}}$ | $V_{\text{DDQ}}/2 - 0.15$ | $V_{\text{DDQ}}/2 + 0.15$ | V | 1-4, 6 |

Notes:

1. DKx and $\overline{\text{DKx}}$ have the same requirements as CK and $\overline{\text{CK}}$.
2. All voltages referenced to V_{SS} (GND).
3. The CK and $\overline{\text{CK}}$ input reference level (for timing referenced to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The input reference level for signals other than CK/ $\overline{\text{CK}}$ is V_{REF} .
4. The CK and $\overline{\text{CK}}$ input slew rate must be ≥ 2 V/ns (≥ 4 V/ns if measured differentially).
5. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.
6. The value of V_{IX} is expected to equal $V_{\text{DDQ}}/2$ of the transmitting device and must track variations in the DC level of the same.

Differential Clock Input Requirements



Notes:

1. CK and $\overline{\text{CK}}$ must cross within this region.
2. CK and $\overline{\text{CK}}$ must meet at least $V_{\text{ID(DC)MIN}}$ when static and centered around $V_{\text{DDQ}}/2$.
3. Minimum peak-to-peak swing.
4. It is a violation to tristate CK and $\overline{\text{CK}}$ after the part is initialized.

Input Slew Rate Derating

The Address and Command Setup and Hold Derating Values shown in the following table should be added to the default t_{AS}/t_{CS} , t_{DS} and $t_{AH}/t_{CH}/t_{DH}$ specifications when the slew rate of any of these input signals is less than the 2 V/ns.

To determine the setup and hold time needed for a given slew rate, add the t_{AS}/t_{CS} default specification to the “ $t_{AS}/t_{CS} V_{REF}$ to CK/\overline{CK} Crossing” and the t_{AH}/t_{CH} default specification to the “ $t_{AH}/t_{CH} CK/\overline{CK}$ Crossing to V_{REF} ” derated values in the Address and Command Setup and Hold Derating Values table. The derated data setup and hold values can be determined the same way using the “ $t_{DS} V_{REF}$ to CK/\overline{CK} Crossing” and “ t_{DH} to CK/\overline{CK} Crossing to V_{REF} ” values in the Data Setup and Hold Derating Values table. The derating values apply to all speed grades.

The setup times in the table relate to a rising signal. The time from the rising signal crossing $V_{IH(AC)MIN}$ to the CK/\overline{CK} cross point is static and must be maintained across all slew rates. The derated setup timing describes the point at which the rising signal crosses $V_{REF(DC)}$ to the CK/\overline{CK} cross point. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between $V_{IH(AC)MIN}$ and the CK/\overline{CK} cross point. All these same values are also valid for falling signals (with respect to $V_{IL(AC)MAX}$ and the CK/\overline{CK} cross point).

The hold times in the table relate to falling signals. The time from the CK/\overline{CK} cross point to when the signal crosses $V_{IH(DC)MIN}$ is static and must be maintained across all slew rates. The derated hold timing describes the delta between the CK/\overline{CK} cross point to when the falling signal crosses $V_{REF(DC)}$. This derated value is calculated by determining the time needed to maintain the given slew rate and the delta between the CK/\overline{CK} cross point and $V_{IH(DC)}$. The hold values are also valid for rising signals (with respect to $V_{IL(DC)MAX}$ and the CK/\overline{CK} cross point).

Note: The above descriptions also pertain to data setup and hold derating when CK/\overline{CK} are replaced with DK/\overline{DK} .

Not Recommended for New Design – Discontinued Product

Address and Command Setup and Hold Derating Values

| Command/Address Slew Rate (V/ns) | tAS/tCS V _{REF} to CK/ $\overline{\text{CK}}$ crossing | tAS/tCS V _{IH(AC)MIN} CK/ $\overline{\text{CK}}$ crossing | tAH/tCH CK/ $\overline{\text{CK}}$ crossing to V _{REF} | tAH/tCH CK/ $\overline{\text{CK}}$ crossing to V _{IH(DC)MIN} | Units |
|---|---|--|---|---|-------|
| CK/ $\overline{\text{CK}}$ Differential Slew Rate: 2.0 V/ns | | | | | |
| 2.0 | 0 | -100 | 0 | -50 | ps |
| 1.9 | 5 | -100 | 3 | -50 | ps |
| 1.8 | 11 | -100 | 6 | -50 | ps |
| 1.7 | 18 | -100 | 9 | -50 | ps |
| 1.6 | 25 | -100 | 13 | -50 | ps |
| 1.5 | 33 | -100 | 17 | -50 | ps |
| 1.4 | 43 | -100 | 22 | -50 | ps |
| 1.3 | 54 | -100 | 27 | -50 | ps |
| 1.2 | 67 | -100 | 34 | -50 | ps |
| 1.1 | 82 | -100 | 41 | -50 | ps |
| 1.0 | 100 | -100 | 50 | -50 | ps |
| CK/ $\overline{\text{CK}}$ Differential Slew Rate: 1.5 V/ns | | | | | |
| 2.0 | 30 | -70 | 30 | -20 | ps |
| 1.9 | 35 | -70 | 33 | -20 | ps |
| 1.8 | 41 | -70 | 36 | -20 | ps |
| 1.7 | 48 | -70 | 39 | -20 | ps |
| 1.6 | 55 | -70 | 43 | -20 | ps |
| 1.5 | 63 | -70 | 47 | -20 | ps |
| 1.4 | 73 | -70 | 52 | -20 | ps |
| 1.3 | 84 | -70 | 57 | -20 | ps |
| 1.2 | 97 | -70 | 64 | -20 | ps |
| 1.1 | 112 | -70 | 71 | -20 | ps |
| 1.0 | 130 | -70 | 80 | -20 | ps |
| CK/ $\overline{\text{CK}}$ Differential Slew Rate: 1.0 V/ns | | | | | |
| 2.0 | 60 | -40 | 60 | 10 | ps |
| 1.9 | 65 | -40 | 63 | 10 | ps |
| 1.8 | 71 | -40 | 66 | 10 | ps |
| 1.7 | 78 | -40 | 69 | 10 | ps |
| 1.6 | 85 | -40 | 73 | 10 | ps |
| 1.5 | 93 | -40 | 77 | 10 | ps |
| 1.4 | 103 | -40 | 82 | 10 | ps |
| 1.3 | 114 | -40 | 87 | 10 | ps |
| 1.2 | 127 | -40 | 94 | 10 | ps |
| 1.1 | 142 | -40 | 101 | 10 | ps |
| 1.0 | 160 | -40 | 110 | 10 | ps |

Data Setup and Hold Derating Values

| Data Slew Rate (V/ns) | tDS V _{REF} to CK/ $\overline{\text{CK}}$ crossing | tDS V _{IH(AC)MIN} CK/ $\overline{\text{CK}}$ crossing | tDS CK/ $\overline{\text{CK}}$ crossing to V _{REF} | tDS CK/ $\overline{\text{CK}}$ crossing to V _{IH(DC)MIN} | Units |
|---|---|--|---|---|-------|
| DK/ $\overline{\text{DK}}$ Differential Slew Rate: 2.0 V/ns | | | | | |
| 2.0 | 0 | -100 | 0 | -50 | ps |
| 1.9 | 5 | -100 | 3 | -50 | ps |
| 1.8 | 11 | -100 | 6 | -50 | ps |
| 1.7 | 18 | -100 | 9 | -50 | ps |
| 1.6 | 25 | -100 | 13 | -50 | ps |
| 1.5 | 33 | -100 | 17 | -50 | ps |
| 1.4 | 43 | -100 | 22 | -50 | ps |
| 1.3 | 54 | -100 | 27 | -50 | ps |
| 1.2 | 67 | -100 | 34 | -50 | ps |
| 1.1 | 82 | -100 | 41 | -50 | ps |
| 1.0 | 100 | -100 | 50 | -50 | ps |
| DK/ $\overline{\text{DK}}$ Differential Slew Rate: 1.5 V/ns | | | | | |
| 2.0 | 30 | -70 | 30 | -20 | ps |
| 1.9 | 35 | -70 | 33 | -20 | ps |
| 1.8 | 41 | -70 | 36 | -20 | ps |
| 1.7 | 48 | -70 | 39 | -20 | ps |
| 1.6 | 55 | -70 | 43 | -20 | ps |
| 1.5 | 63 | -70 | 47 | -20 | ps |
| 1.4 | 73 | -70 | 52 | -20 | ps |
| 1.3 | 84 | -70 | 57 | -20 | ps |
| 1.2 | 97 | -70 | 64 | -20 | ps |
| 1.1 | 112 | -70 | 71 | -20 | ps |
| 1.0 | 130 | -70 | 80 | -20 | ps |
| DK/ $\overline{\text{DK}}$ Differential Slew Rate: 1.0 V/ns | | | | | |
| 2.0 | 60 | -40 | 60 | 10 | ps |
| 1.9 | 65 | -40 | 63 | 10 | ps |
| 1.8 | 71 | -40 | 66 | 10 | ps |
| 1.7 | 78 | -40 | 69 | 10 | ps |
| 1.6 | 85 | -40 | 73 | 10 | ps |
| 1.5 | 93 | -40 | 77 | 10 | ps |
| 1.4 | 103 | -40 | 82 | 10 | ps |
| 1.3 | 114 | -40 | 87 | 10 | ps |
| 1.2 | 127 | -40 | 94 | 10 | ps |
| 1.1 | 142 | -40 | 101 | 10 | ps |
| 1.0 | 160 | -40 | 110 | 10 | ps |

Capacitance

| Description | Symbol | Conditions | Min. | Max. | Unit |
|--|------------|---|------|------|------|
| Address/control input capacitance | C_I | $T_A = 25^\circ\text{C}; f = 100\text{ MHz}$ $V_{DD} = V_{DDQ} = 1.8\text{ V}$ | 1.0 | 2.0 | pF |
| Input/Output capacitance (DQ, DM, and QK, \overline{QK}) | C_O | | 3.0 | 4.5 | pF |
| Clock capacitance (CK/ \overline{CK} and DK/ \overline{DK}) | C_{CK} | | 1.5 | 2.5 | pF |
| JTAG pins | C_{JTAG} | | 1.5 | 4.5 | pF |

Notes:

- Capacitance is not tested on the ZQ pin.
- JTAG Pins are tested at 50 MHz.

IDD Operating Conditions

| Description | Condition | Symbol | -18 | -24 | -25 | -33 | Units |
|------------------------|---|---------------------------------|-----|-----|-----|-----|-------|
| Standby Current | tCK = idle, All banks idle; No inputs toggling. | $I_{SB1}(V_{DD}) \times 9/x18$ | 55 | 55 | 55 | 55 | mA |
| | | $I_{SB1}(V_{DD}) \times 36$ | 55 | 55 | 55 | 55 | |
| | | $I_{SB1}(V_{EXT})$ | 5 | 5 | 5 | 5 | |
| Active Standby Current | $\overline{CS} = 1$, No commands; Bank address incremented and half address/data change once every four clock cycles. | $I_{SB2}(V_{DD}) \times 9/x18$ | 385 | 360 | 360 | 340 | mA |
| | | $I_{SB2}(V_{DD}) \times 36$ | 385 | 360 | 360 | 340 | |
| | | $I_{SB2}(V_{EXT})$ | 5 | 5 | 5 | 5 | |
| Operational Current | BL = 2, Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by Write sequence; Continuous data during Write Commands. | $I_{DD1}(V_{DD}) \times 9/x18$ | 495 | 470 | 445 | 425 | mA |
| | | $I_{DD1}(V_{DD}) \times 36$ | 510 | 485 | 455 | 435 | |
| | | $I_{DD1}(V_{EXT})$ | 15 | 15 | 15 | 10 | |
| Operational Current | BL = 4, Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC; Read followed by Write sequence; Continuous data during Write Commands. | $I_{DD2}(V_{DD}) \times 9/x18$ | 495 | 480 | 450 | 435 | mA |
| | | $I_{DD2}(V_{DD}) \times 36$ | 540 | 525 | 485 | 470 | |
| | | $I_{DD2}(V_{EXT})$ | 25 | 25 | 25 | 20 | |
| Operational Current | BL = 8, Sequential bank access; Bank transitions once every tRC; Half address transitions once every tRC. Read followed by Write sequence; Continuous data during Write Commands. | $I_{DD3}(V_{DD}) \times 9/x18$ | 580 | 555 | 500 | 480 | mA |
| | | $I_{DD3}(V_{DD}) \times 36$ | 665 | 640 | 570 | 550 | |
| | | $I_{DD3}(V_{EXT})$ | 40 | 40 | 40 | 30 | |
| Burst Refresh Current | Eight bank cyclic refresh; Continuous address/data; Command bus remains in refresh for all eight banks. | $I_{REF1}(V_{DD}) \times 9/x18$ | 720 | 625 | 615 | 540 | mA |
| | | $I_{REF1}(V_{DD}) \times 36$ | 720 | 625 | 615 | 540 | |
| | | $I_{REF1}(V_{EXT})$ | 60 | 60 | 60 | 45 | |

IDD Operating Conditions (Continued)

| Description | Condition | Symbol | -18 | -24 | -25 | -33 | Units |
|---------------------------------------|--|---------------------------------|-----|-----|-----|-----|-------|
| Distributed Refresh Current | Single bank refresh; Sequential bank access; Half address transitions once every tRC; Continuous data. | $I_{REF2}(V_{DD}) \times 9/x18$ | 425 | 400 | 390 | 370 | mA |
| | | $I_{REF2}(V_{DD}) \times 36$ | 425 | 400 | 390 | 370 | |
| | | $I_{REF2}(V_{EXT})$ | 15 | 15 | 15 | 10 | |
| Operating Burst Write Current Example | BL= 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous Write. | $I_{DD2W}(V_{DD}) \times 9/x18$ | 960 | 820 | 810 | 695 | mA |
| | | $I_{DD2W}(V_{DD}) \times 36$ | 995 | 855 | 850 | 735 | |
| | | $I_{DD2W}(V_{EXT})$ | 60 | 60 | 60 | 45 | |
| Operating Burst Write Current Example | BL= 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous Write. | $I_{DD4W}(V_{DD}) \times 9/x18$ | 755 | 655 | 655 | 575 | mA |
| | | $I_{DD4W}(V_{DD}) \times 36$ | 895 | 765 | 765 | 660 | |
| | | $I_{DD4W}(V_{EXT})$ | 55 | 55 | 55 | 40 | |
| Operating Burst Write Current Example | BL= 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous Write. | $I_{DD8W}(V_{DD}) \times 9/x18$ | 720 | 620 | 620 | 540 | mA |
| | | $I_{DD8W}(V_{DD}) \times 36$ | 855 | 730 | 730 | 630 | |
| | | $I_{DD8W}(V_{EXT})$ | 55 | 55 | 55 | 40 | |
| Operating Burst Read Current Example | BL= 2; Cyclic bank access; Half of address bits change every clock cycle; Continuous data; Measurement is taken during continuous Read. | $I_{DD2R}(V_{DD}) \times 9/x18$ | 850 | 725 | 720 | 620 | mA |
| | | $I_{DD2R}(V_{DD}) \times 36$ | 865 | 740 | 730 | 630 | |
| | | $I_{DD2R}(V_{EXT})$ | 60 | 60 | 60 | 45 | |
| Operating Burst Read Current Example | BL= 4; Cyclic bank access; Half of address bits change every two clock cycles; Continuous data; Measurement is taken during continuous Read. | $I_{DD4R}(V_{DD}) \times 9/x18$ | 675 | 580 | 580 | 505 | mA |
| | | $I_{DD4R}(V_{DD}) \times 36$ | 785 | 665 | 665 | 570 | |
| | | $I_{DD4R}(V_{EXT})$ | 55 | 55 | 55 | 40 | |
| Operating Burst Read Current Example | BL= 8; Cyclic bank access; Half of address bits change every four clock cycles; Continuous data; Measurement is taken during continuous Read. | $I_{DD8R}(V_{DD}) \times 9/x18$ | 645 | 555 | 555 | 485 | mA |
| | | $I_{DD8R}(V_{DD}) \times 36$ | 760 | 645 | 645 | 550 | |
| | | $I_{DD8R}(V_{EXT})$ | 55 | 55 | 55 | 40 | |

Notes:

- I_{DD} specifications are tested after the device is properly initialized and is operating at worst-case rated temperature and voltage specifications.
- Definitions of IDD Conditions:
 - Low is defined as $V_{IN} \leq V_{IL(AC) MAX}$.
 - High is defined as $V_{IN} \geq V_{IH(AC) MIN}$.
 - Stable is defined as inputs remaining at a High or Low level.
 - Floating is defined as inputs at $V_{REF} = V_{DD}/2$.
 - Continuous data is defined as half the DQ signals changing between High and Low every half clock cycle (twice per clock).
 - Continuous address is defined as half the address signals changing between High and Low every clock cycles (once per clock).
 - Sequential bank access is defined as the bank address incrementing by one every tRC.
 - Cyclic bank access is defined as the bank address incrementing by one for each command access. For BL = 2 this is every clock, for BL = 4 this is every other clock, and for BL = 8 this is every fourth clock.
- \overline{CS} is High unless a Read, Write, AREF, or MRS command is registered. \overline{CS} never transitions more than once per clock cycle.
- I_{DD} parameters are specified with ODT disabled.
- Tests for AC timing, I_{DD} , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
- I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/\overline{CK}), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

AC Electrical Characteristics

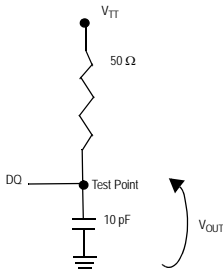
| Parameter | Symbol | -18 | | -24 | | -25 | | -33 | | Units | Notes |
|---|--|---|------|---|------|---|------|---|------|------------------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Clock | | | | | | | | | | | |
| Input Clock Cycle Time | t _{CK} | 1.875 | 5.7 | 2.5 | 5.7 | 2.5 | 5.7 | 3.3 | 5.7 | ns | — |
| Input data clock cycle time | t _{DK} | t _{CK} | | t _{CK} | | t _{CK} | | t _{CK} | | ns | — |
| Clock jitter: period | t _{JIT_{PER}} | -100 | 100 | -150 | 150 | -150 | 150 | -200 | 200 | ps | 5, 6 |
| Clock jitter: cycle-to-cycle | t _{JIT_{CC}} | — | 200 | — | 300 | — | 300 | — | 400 | ps | — |
| Clock High Time | t _{CKH} t _{DKH} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} | — |
| Clock Low Time | t _{CKL} t _{DKL} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} | — |
| Clock to input data clock | t _{CKDK} | -0.3 | 0.3 | -0.45 | 0.5 | -0.45 | 0.5 | -0.45 | 1.2 | ns | — |
| Mode register set cycle time to any command | t _{MRSC} | 6 | — | 6 | — | 6 | — | 6 | — | t _{CK} | — |
| Setup Times | | | | | | | | | | | |
| Address/command and input setup time | t _{AS/ICS} | 0.3 | — | 0.4 | — | 0.4 | — | 0.5 | — | ns | — |
| Data-in and data mask to DK set up time | t _{DS} | 0.17 | — | 0.25 | — | 0.25 | — | 0.3 | — | ns | — |
| Hold Times | | | | | | | | | | | |
| Address/command and input hold time | t _{AH/ICS} | 0.3 | — | 0.4 | — | 0.4 | — | 0.5 | — | ns | — |
| Data-in and data mask to DK setup time | t _{DH} | 0.17 | — | 0.25 | — | 0.25 | — | 0.3 | — | ns | — |
| Data and Data Strobe | | | | | | | | | | | |
| Output data clock High time | t _{QKH} | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t _{CKH} | — |
| Output data clock Low time | t _{QKL} | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t _{CKL} | — |
| Half-clock period | t _{QHP} | MIN (t _{QKH} , t _{QKL}) | — | MIN (t _{QKH} , t _{QKL}) | — | MIN (t _{QKH} , t _{QKL}) | — | MIN (t _{QKH} , t _{QKL}) | — | — | — |
| QK edge to clock edge skew | t _{CKQK} | -0.2 | 0.2 | -0.25 | 0.25 | -0.25 | 0.25 | -0.3 | 0.3 | ns | — |
| QK edge to output data edge | t _{QKQ0} , t _{QKQ1} | -0.12 | 0.12 | -0.2 | 0.2 | -0.2 | 0.2 | -0.25 | 0.25 | ns | 7 |
| QK edge to any output data edge | t _{QKQ} | -0.22 | 0.22 | -0.3 | 0.3 | -0.3 | 0.3 | -0.35 | 0.35 | ns | 8 |
| QK edge to QVLD | t _{QKVLD} | -0.22 | 0.22 | -0.3 | 0.3 | -0.3 | 0.3 | -0.35 | 0.35 | ns | — |
| Data Valid Window | t _{DVW} | t _{DVW} (MIN) | — | t _{DVW} (MIN) | — | t _{DVW} (MIN) | — | t _{DVW} (MIN) | — | — | 9 |

AC Electrical Characteristics (Continued)

| Parameter | Symbol | -18 | | -24 | | -25 | | -33 | | Units | Notes |
|-----------------------------------|--------|-----|------|-----|------|-----|------|-----|------|-------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Refresh | | | | | | | | | | | |
| Average Periodic Refresh Interval | tREFI | — | 0.24 | — | 0.24 | — | 0.24 | — | 0.24 | μ | 10 |

Notes:

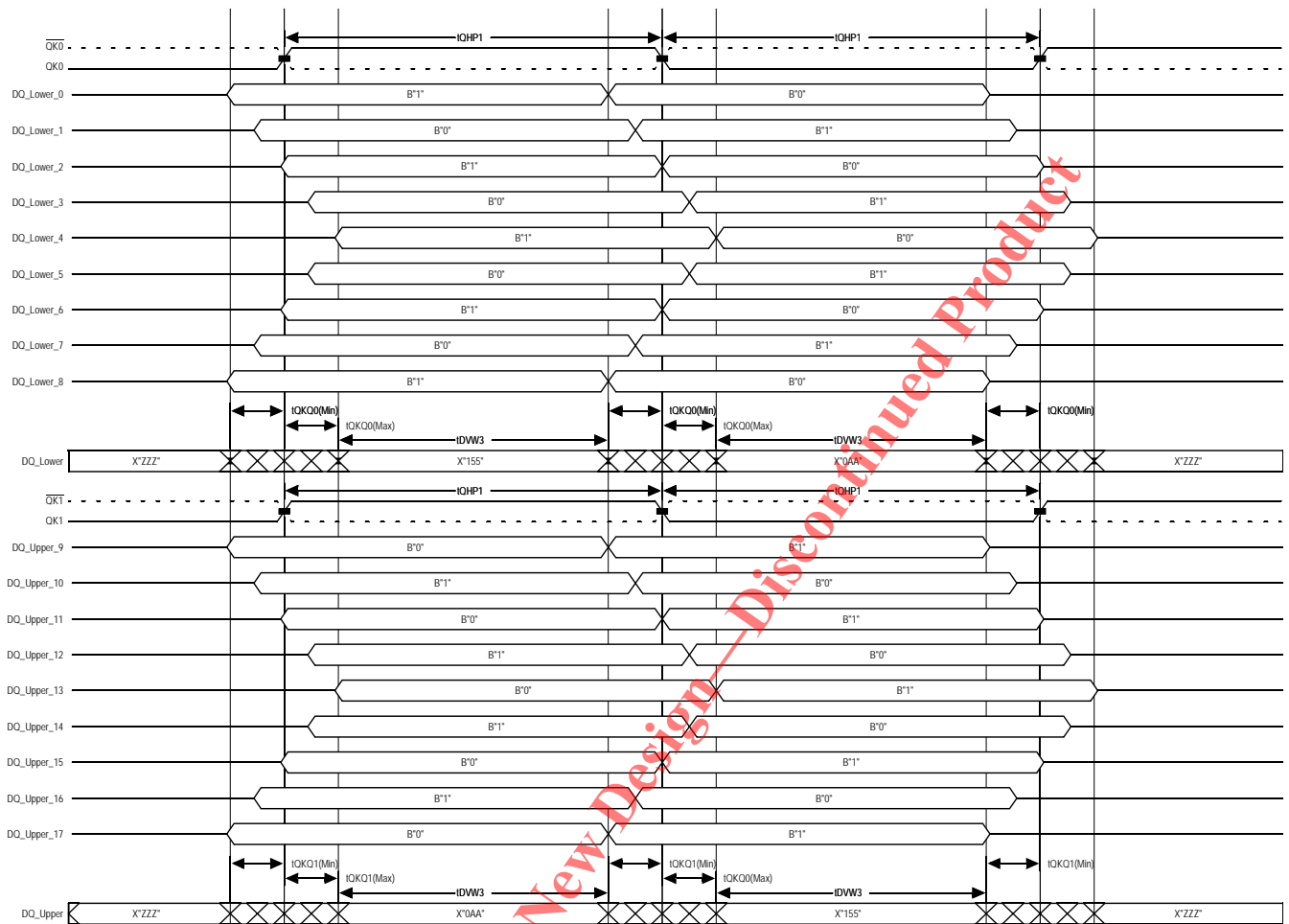
- All timing parameters are measured relative to the crossing point of $\overline{CK}/\overline{CK}$, $\overline{DK}/\overline{DK}$ and to the crossing point with V_{REF} of the command, address, and data signals.
- Outputs measured with equivalent load:



- Tests for AC timing I_{DD} , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
- AC timing may use a V_{IL} to $-V_{IH}$ swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for $\overline{CK}/\overline{CK}$), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
- Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
- Frequency drift is not allowed.
- tQKQ0 is referenced to DQ0–DQ17 for the x36 xconfiguration and DQ0–DQ8 for the x18 configuration. tQKQ1 is referenced to DQ18–DQ35 for the x36 configuration and the DQ9–DQ17 for the x18 configuration.
- tQKQ takes in to account the skew between any QKx and any Q.
- $tDVW (MIN) \leq tQHP - (tQKQx [MAX] + |tQKQx [MIN]|)$
- To improve efficiency, eight AREF commands (one for each bank) can be posted to the LLDRAM II on consecutive cycles at periodic intervals of 1.95 μs.

Not Recommended for New Design - Discontinued Product

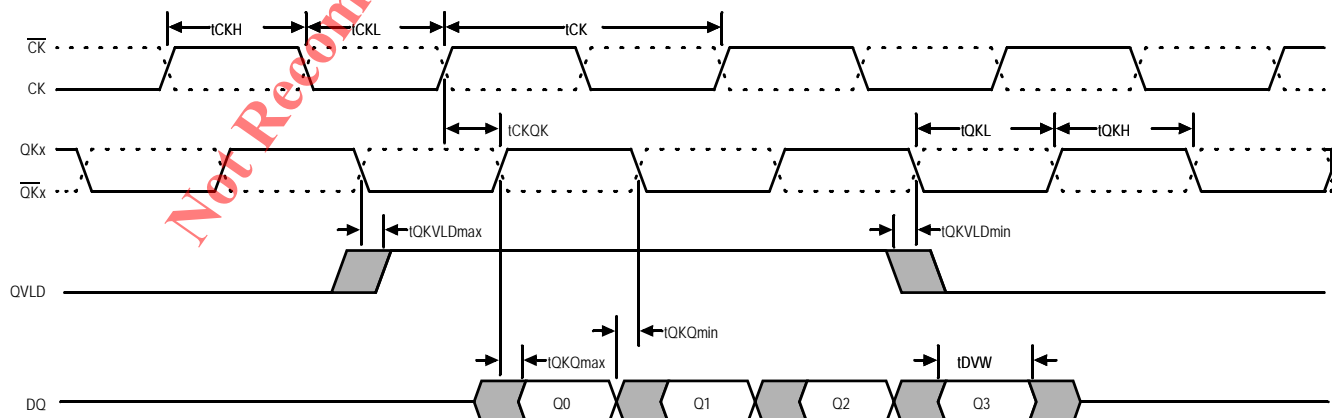
Read Data Valid Window for x18 Device



Notes:

1. $tQHP$ is defined as the lesser of $tQKH$ or $tQKL$.
2. $tQKQ0$ is referenced to $DQ0-DQ8$.
3. Minimum data valid window ($tDVW$) can be expressed as $tQHP - (tQKQx [MAX] + |tQKQx [MIN]|)$.
4. $tQKQ1$ is referenced to $DQ9-DQ17$.
5. $tQKQ$ takes into account the skew between any QKx and any DQ .

Read Burst Timing



IEEE 1149.1 Serial Boundary Scan (JTAG)

LLDRAM II includes an IEEE 1149.1 (JTAG) serial boundary scan Test Access Port (TAP). JTAG ports are generally used to verify the connectivity of the device once it has been mounted on a Printed Circuit Board (PCB). The port operates in accordance with IEEE Standard 1149.1-2001 (JTAG). Because the ZQ pin is actually an analog output, to ensure proper boundary-scan testing of the ZQ pin, Mode Register Bit 8 (M8) needs to be set to 0 until the JTAG testing of the pin is complete. Note that upon power up, the default state of Mode Register Bit 8 (M8) is Low.

Whenever the JTAG port is used prior to the initialization of the LLDRAM II device, such as when initial connectivity testing is conducted, it is critical that the CK and $\overline{\text{CK}}$ pins meet $V_{\text{ID}(\text{DC})}$ or that $\overline{\text{CS}}$ be held High from power-up until testing begins. Failure to do so can result in inadvertent MRS commands being loaded and causing unexpected test results. Alternately a partial initialization can be conducted that consists of simply loading a single MRS command with desired MRS Register settings. JTAG testing may then begin as soon as tMRSC is satisfied. JTAG testing can be conducted after full initialization as well.

The input signals of the test access port (TDI, TMS, and TCK) are referenced to the V_{DD} as a supply, while the output driver of the TAP (TDO) is powered by V_{DDQ} .

The JTAG test access port incorporates a standard TAP controller from which the Instruction Register, Boundary Scan Register, Bypass Register, and ID Code Register can be selected. Each of these functions of the TAP controller are described below.

Disabling the JTAG Feature

Use of the JTAG port is never required for RAM operation. To disable the TAP controller, TCK must be tied Low (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected or they can be connected to V_{DD} directly or through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK.

All of the states in the TAP Controller State Diagram are entered through the serial input of the TMS pin. A “0” in the diagram represents a Low on the TMS pin during the rising edge of TCK while a “1” represents a High on TMS.

Test Data-In (TDI)

The TDI ball is used to serially input test instructions and data into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is connected to the Most Significant Bit (MSB) of any register (see the TAP Controller Block Diagram).

Test Data-Out (TDO)

The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register (see the TAP Controller Block Diagram).

TAP Controller

The TAP controller is a finite state machine that uses the state of the TMS pin at the rising edge of TCK to navigate through its various modes of operation. See the TAP Controller State Diagram. Each state is described in detail below.

Test-Logic-Reset

The test-logic-reset controller state is entered when TMS is held High for at least five consecutive rising edges of TCK. As long as TMS remains High, the TAP controller will remain in the test-logic-reset state. The test logic is inactive during this state.

Run-Test/Idle

The run-test/idle is a controller state in between scan operations. This state can be maintained by holding TMS Low. From here either the data register scan, or subsequently, the instruction register scan can be selected.

Select-DR-Scan

Select-DR-scan is a temporary controller state. All test data registers retain their previous state while here.

Capture-DR

The Capture-DR state is where the data is parallel-loaded into the test data registers. If the Boundary Scan Register is the currently selected register, then the data currently on the pins is latched into the test data registers.

Shift-DR

Data is shifted serially through the data register while in this state. As new data is input through the TDI pin, data is shifted out of the TDO pin.

Exit1-DR, Pause-DR, and Exit2-DR

The purpose of Exit1-DR is used to provide a path to return back to the run-test/idle state (through the Update-DR state). The Pause-DR state is entered when the shifting of data through the test registers needs to be suspended. When shifting is to reconvene, the controller enters the Exit2-DR state and then can re-enter the Shift-DR state.

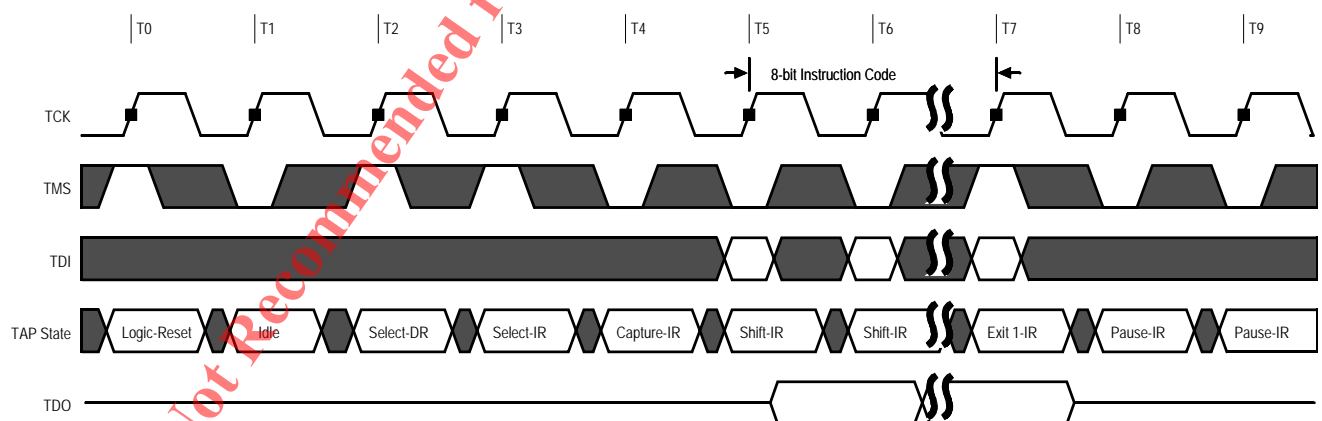
Update-DR

When the EXTEST instruction is selected, there are latched parallel outputs of the boundary scan shift register that only change state during the Update-DR controller state.

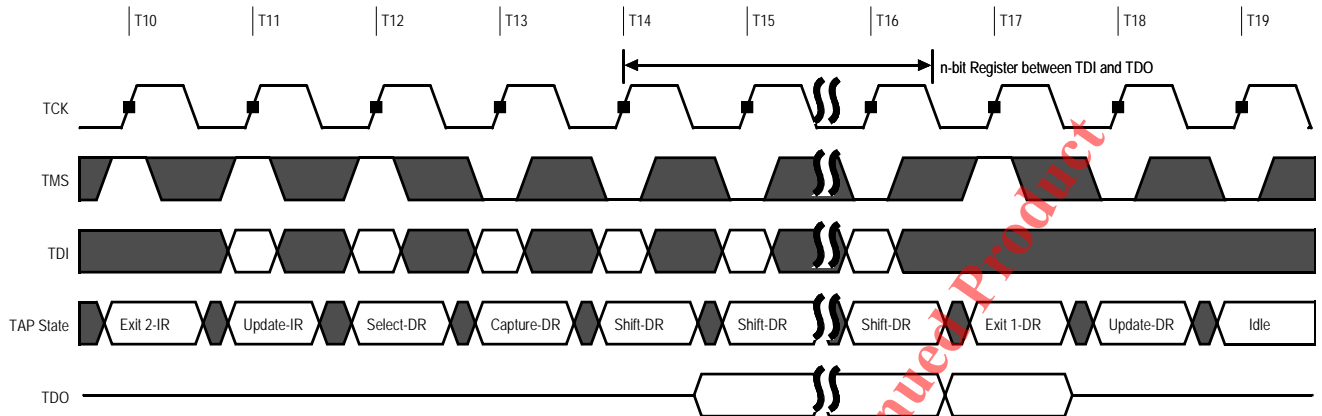
Instruction Register States

The instruction register states of the TAP controller are similar to the data register states. The desired instruction is serially shifted into the instruction register during the Shift-IR state and is loaded during the Update-IR state.

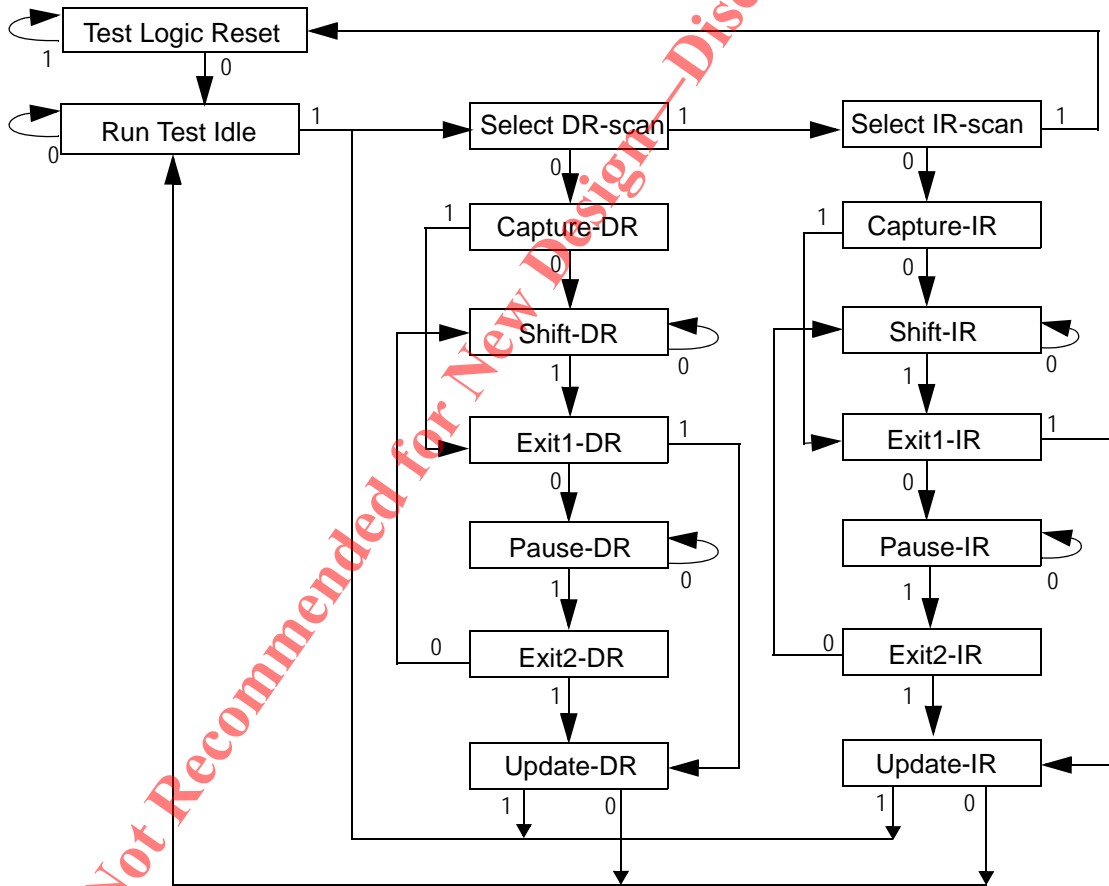
Loading Instruction Code and Shifting Out Data

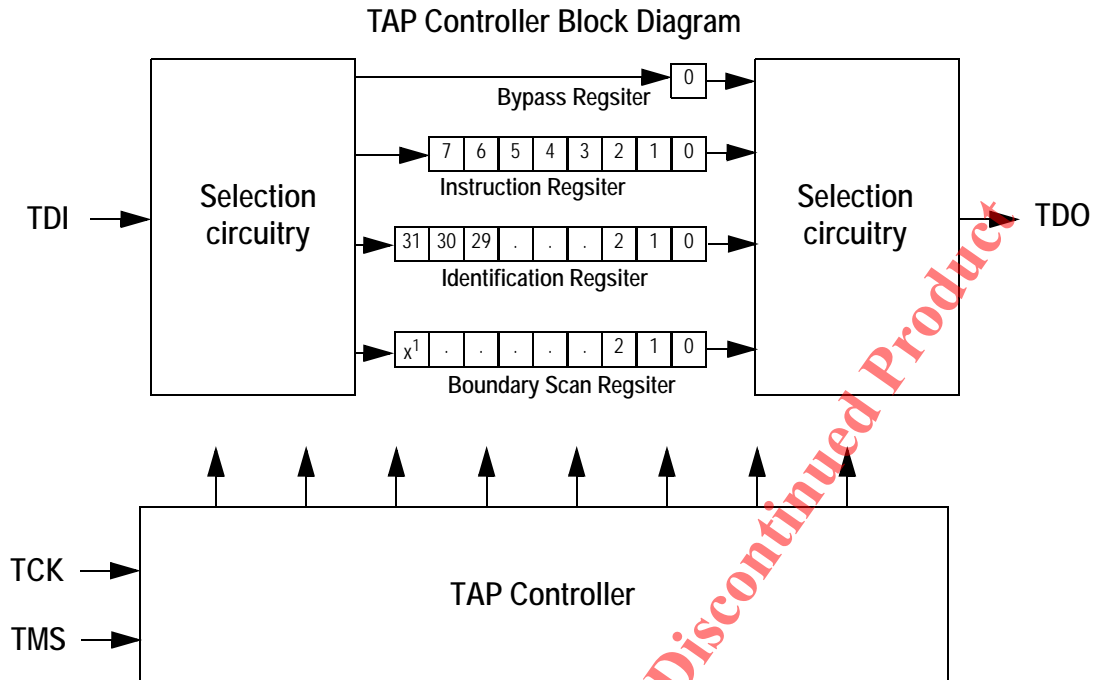


Loading Instruction Code and Shifting Out Data (Continued)



JTAG Tap Controller State Diagram





Note:

x= 112 for all configurations

Performing a TAP RESET

A reset is performed by forcing TMS High (V_{DDQ}) for five rising edges of TCK. This RESET does not affect the operation of the LLD RAM II and may be performed while the LLD RAM II is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the LLD RAM II test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded during the Update-IR state of the TAP controller. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the LLD RAM II with minimal delay. The bypass register is set Low (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The Boundary Scan Register is connected to all the input and bidirectional balls on the LLD RAM II. Several bits are also included in the scan register for reserved balls. The LLD RAM II has a 113-bit register.

The Boundary Scan Register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state.

The Boundary Scan Register table shows the order in which the bits are connected. Each bit corresponds to one of the balls on the LLD RAM II package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the LLD RAM II and can be shifted out when the TAP controller is in the shift-DR state. The ID register has a vendor code and other information described in the table below.

Identification Register Definitions

| Instruction Field | Bit Size | Bit Size |
|------------------------------------|------------------|--|
| Revision number (31:28) | abcd | ab = die revision cd = 00 for x9, 01 for x18, 10 for x36 |
| Device ID (27:12) | 00jkidef10100111 | def = 000 for 288Mb, 001 for 576Mb i = 0 for common I/O, 1 for separate I/O jk = 01 for LLD RAM II |
| GSI JEDEC ID code (11:1) | 01011011001 | Allows unique identification of LLD RAM II vendor |
| ID register presence indicator (0) | 1 | Indicates the presence of an ID register |

TAP Instruction Set

Overview

Many different instructions (256) are possible with the 8-bit instruction register. All combinations used are listed in the Instruction Codes table. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this LLD RAM II is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary Scan Register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the Boundary Scan Register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-Z instruction places all LLD RAM II outputs into a High-Z state, and causes the bypass register to be connected between TDI and TDO when the TAP Controller is in the Shift DR state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output balls are determined from the values held in the Boundary Scan Register. Additionally, it causes the bypass register to be connected between TDI and TDO when the TAP Controller is in the Shift DR state.

SAMPLE/PRELOAD

When the SAMPLe/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the Boundary Scan Register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the LLD RAM II clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the Boundary Scan Register will capture the correct value of a signal, the LLD RAM II signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time ($t_{CS} + t_{CH}$). The LLD RAM II clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLe/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and \overline{CK} captured in the Boundary Scan Register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the Boundary Scan Register between the TDI and TDO balls.

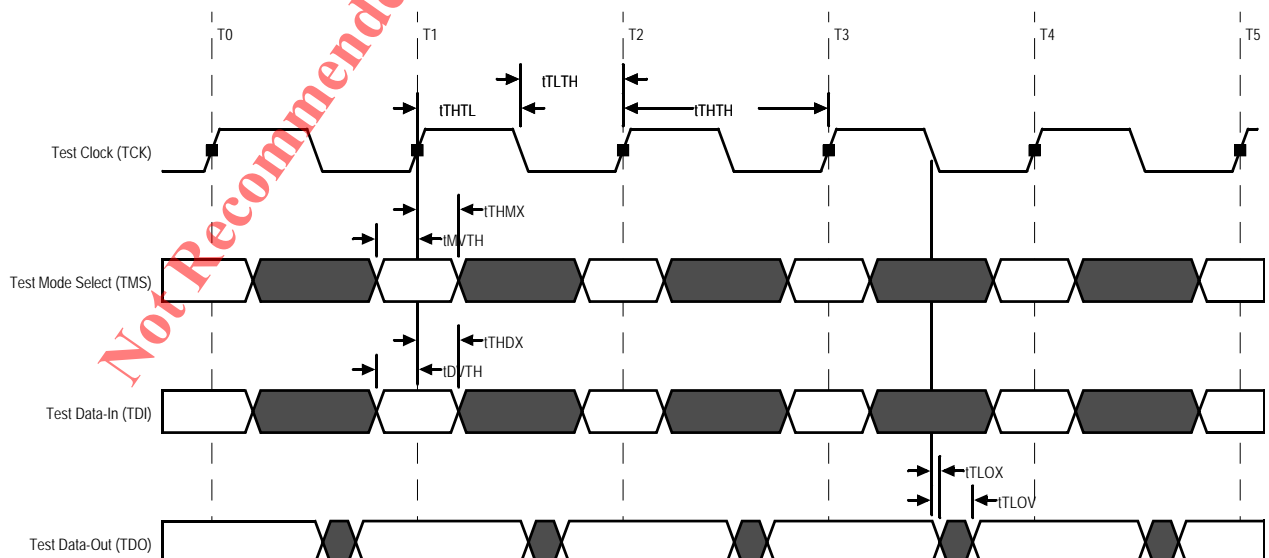
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved for Future Use

The remaining instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP Input AC Logic Levels

| Description | Symbol | Min | Max | Units |
|------------------------------|----------|-----------------|-----------------|-------|
| Input High (logic 1) Voltage | V_{IH} | $V_{REF} + 0.3$ | — | V |
| Input Low (logic 0) Voltage | V_{IL} | — | $V_{REF} - 0.3$ | V |

TAP AC Electrical Characteristics

| Description | Symbol | Min | Max | Units |
|-------------------------|-------------------|-----|-----|-------|
| Clock | | | | |
| Clock Cycle Time | t _{THTH} | 20 | — | ns |
| Clock Frequency | t _{TF} | — | 50 | MHz |
| Clock High Time | t _{THTL} | 10 | — | ns |
| Clock Low Time | t _{TLTH} | 10 | — | ns |
| TDI/TDO Times | | | | |
| TCK Low to TDO Unknown | t _{TLOX} | 0 | — | ns |
| TCK Low to TDO Valid | t _{TLOV} | — | 10 | ns |
| TDI Valid to TCK High | t _{DVTH} | 5 | — | ns |
| TCK High to TDI Invalid | t _{THDX} | 5 | — | ns |
| Setup Times | | | | |
| TMS Setup | t _{MVTH} | 5 | — | ns |
| Capture Setup | t _{CS} | 5 | — | ns |
| Hold Times | | | | |
| TMS Setup | t _{THMX} | 5 | — | ns |
| Capture Setup | t _{CH} | 5 | — | ns |

Note:

t_{CS} and t_{CH} refer to the set up and hold time requirements of latching data from the Boundary Scan Register.

TAP DC Electrical Characteristics and Operating Conditions

| Description | Condition | Symbol | Min | Max | Units | Notes |
|------------------------------|--|-----------|------------------|------------------|---------|-------|
| Input High (logic 1) Voltage | — | V_{IH} | $V_{REF} + 0.15$ | $V_{DD} + 0.3$ | V | 1, 2 |
| Input High (logic 0) Voltage | — | V_{IL} | $V_{SS} - 0.3$ | $V_{REF} - 0.15$ | V | 1, 2 |
| Input Leakage Current | Output disabled, $0 V \leq V_{IN} \leq V_{DDQ}$ | I_{LI} | -5.0 | 5.0 | μA | — |
| Output Leakage Current | $0 V \leq V_{IN} \leq V_{DD}$ | I_{LO} | -5.0 | 5.0 | μA | — |
| Output Low Voltage | $I_{OLC} = 100 \mu A$ | V_{OL1} | — | 0.2 | V | 1 |
| Output Low Voltage | $I_{OLT} = 2mA$ | V_{OL2} | — | 0.4 | V | 1 |
| Output High Voltage | $ I_{OHC} = 100 \mu A$ | V_{OH1} | $V_{DDQ} - 0.2$ | — | V | 1 |
| Output High Voltage | $ I_{OHT} = 2mA$ | V_{OH2} | $V_{DDQ} - 0.4$ | — | V | 1 |

Notes:

- All voltages referenced to V_{SS} (GND).
- Overshoot = $V_{IH(AC)} \leq V_{DD} + 0.7 V$ for $t \leq t_{THH}/2$; undershoot = $V_{IL(AC)} \geq -0.5 V$ for $t \leq t_{THH}/2$; during normal operation, V_{DDQ} must not exceed V_{DD} .

Scan Register Sizes

| Register Name | Bit Size |
|---------------|----------|
| Instruction | 8 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 113 |

JTAG TAP Instruction Codes

| Instruction | Code | Description |
|----------------|-----------|---|
| EXTEST | 0000 0000 | Captures I/O ring contents; Places the Boundary Scan Register between TDI and TDO. Data driven by output balls are determined from values held in the Boundary Scan Register. |
| IDCODE | 0010 0001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect LLDRAM II operations. |
| SAMPLE/PRELOAD | 0000 0101 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. This operation does not affect LLDRAM II operations. |
| CLAMP | 0000 0111 | Selects the bypass register to be connected between TDI and TDO. Data driven by output balls are determined from values held in the Boundary Scan Register. |
| HIGH-Z | 0000 0011 | Selects the bypass register to be connected between TDI and TDO. All outputs are forced into High-Z. |
| BYPASS | 1111 1111 | Places Bypass Register between TDI and TDO. This operation does not affect LLDRAM II operations. |

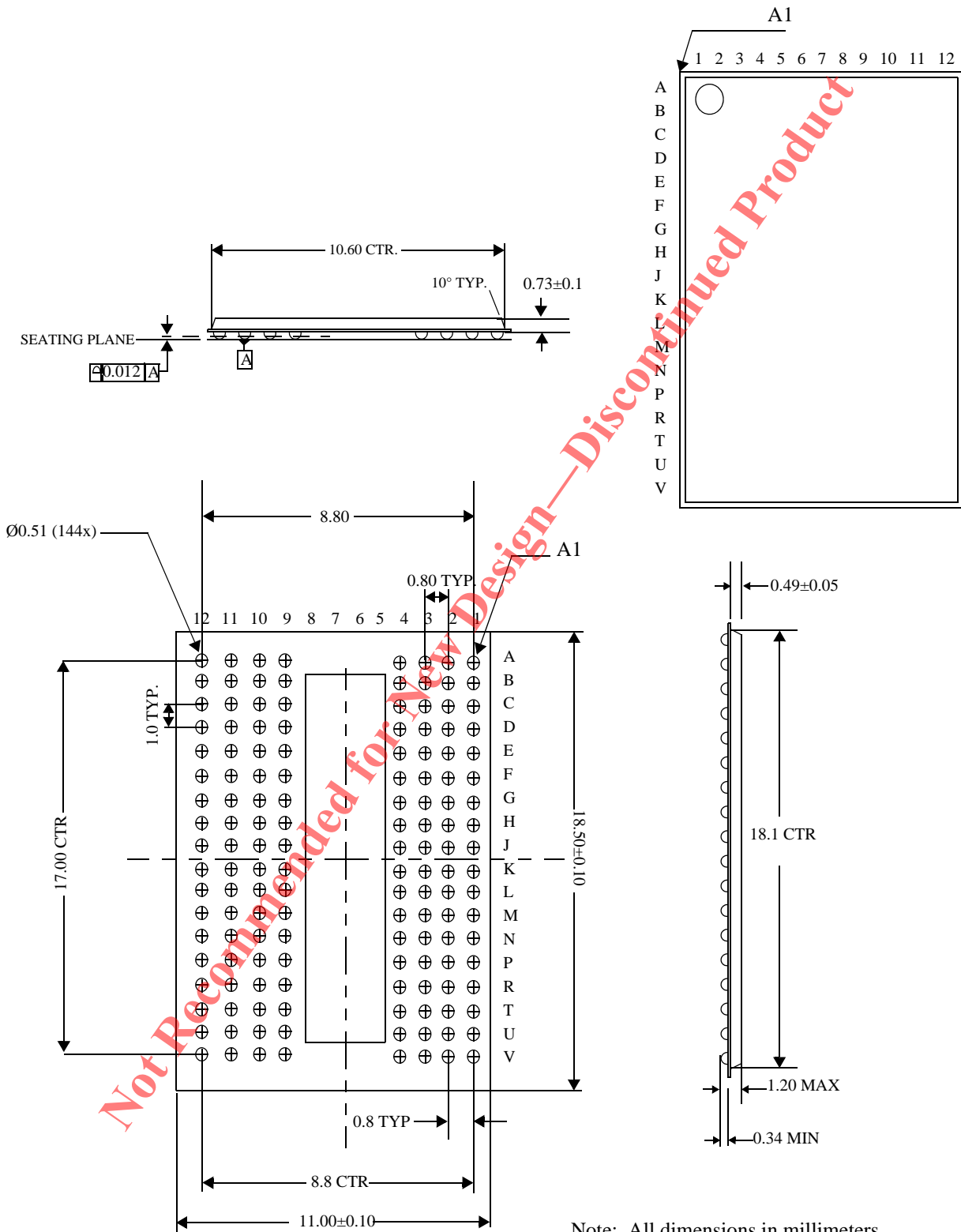
Boundary Scan Exit Order

| Bit # | Ball | Bit # | Ball | Bit # | Ball |
|-------|------|-------|------|-------|------|
| 1 | K1 | 39 | R11 | 77 | C11 |
| 2 | K2 | 40 | R11 | 78 | C11 |
| 3 | L2 | 41 | P11 | 79 | C10 |
| 4 | L1 | 42 | P11 | 80 | C10 |
| 5 | M1 | 43 | P10 | 81 | B11 |
| 6 | M3 | 44 | P10 | 82 | B11 |
| 7 | M2 | 45 | N11 | 83 | B10 |
| 8 | N1 | 46 | N11 | 84 | B10 |
| 9 | P1 | 47 | N10 | 85 | B3 |
| 10 | N3 | 48 | N10 | 86 | B3 |
| 11 | N3 | 49 | P12 | 87 | B2 |
| 12 | N2 | 50 | N12 | 88 | B2 |
| 13 | N2 | 51 | M11 | 89 | C3 |
| 14 | P3 | 52 | M10 | 90 | C3 |
| 15 | P3 | 53 | M12 | 91 | C2 |
| 16 | P2 | 54 | L12 | 92 | C2 |
| 17 | P2 | 55 | L11 | 93 | D3 |
| 18 | R2 | 56 | K11 | 94 | D3 |
| 19 | R3 | 57 | K12 | 95 | D2 |
| 20 | T2 | 58 | J12 | 96 | D2 |
| 21 | T2 | 59 | J11 | 97 | E2 |
| 22 | T3 | 60 | H11 | 98 | E2 |
| 23 | T3 | 61 | H12 | 99 | E3 |
| 24 | U2 | 62 | G12 | 100 | E3 |
| 25 | U2 | 63 | G10 | 101 | F2 |
| 26 | U3 | 64 | G11 | 102 | F2 |
| 27 | U3 | 65 | E12 | 103 | F3 |
| 28 | V2 | 66 | F12 | 104 | F3 |
| 29 | U10 | 67 | F10 | 105 | E1 |
| 30 | U10 | 68 | F10 | 106 | F1 |
| 31 | U11 | 69 | F11 | 107 | G2 |
| 32 | U11 | 70 | F11 | 108 | G3 |
| 33 | T10 | 71 | E10 | 109 | G1 |
| 34 | T10 | 72 | E10 | 110 | H1 |
| 35 | T11 | 73 | E11 | 111 | H2 |
| 36 | T11 | 74 | E11 | 112 | J2 |
| 37 | R10 | 75 | D11 | 113 | J1 |
| 38 | R10 | 76 | D10 | — | — |

Boundary Scan (BSDL Files)

For information regarding the Boundary Scan Chain, or to obtain BSDL files for this part, please contact our Applications Engineering Department at: apps@gsitechnology.com.

Package Dimensions—144-Bump μ BGA (Package L)



Note: All dimensions in millimeters.

Ordering Information for GSI LLD RAM IIs

| Org | Part Number ¹ | Type | Package | Speed (tCK/tRC) | T ² |
|----------|--------------------------|----------------|------------------------------|-----------------|----------------|
| 64M x 9 | GS4576C09L-18 | CIO LLD RAM II | 144-ball μBGA | 533/15 | C |
| 64M x 9 | GS4576C09L-24 | CIO LLD RAM II | 144-ball μBGA | 400/15 | C |
| 64M x 9 | GS4576C09L-25 | CIO LLD RAM II | 144-ball μBGA | 400/20 | C |
| 64M x 9 | GS4576C09L-33 | CIO LLD RAM II | 144-ball μBGA | 300/20 | C |
| 32M x 18 | GS4576C18L-18 | CIO LLD RAM II | 144-ball μBGA | 533/15 | C |
| 32M x 18 | GS4576C18L-24 | CIO LLD RAM II | 144-ball μBGA | 400/15 | C |
| 32M x 18 | GS4576C18L-25 | CIO LLD RAM II | 144-ball μBGA | 400/20 | C |
| 32M x 18 | GS4576C18L-33 | CIO LLD RAM II | 144-ball μBGA | 300/20 | C |
| 16M x 36 | GS4576C36L-18 | CIO LLD RAM II | 144-ball μBGA | 533/15 | C |
| 16M x 36 | GS4576C36L-24 | CIO LLD RAM II | 144-ball μBGA | 400/15 | C |
| 16M x 36 | GS4576C36L-25 | CIO LLD RAM II | 144-ball μBGA | 400/20 | C |
| 16M x 36 | GS4576C36L-33 | CIO LLD RAM II | 144-ball μBGA | 300/20 | C |
| 64M x 9 | GS4576C09GL-18 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 533/15 | C |
| 64M x 9 | GS4576C09GL-24 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 400/15 | C |
| 64M x 9 | GS4576C09GL-25 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 400/20 | C |
| 64M x 9 | GS4576C09GL-33 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 300/20 | C |
| 32M x 18 | GS4576C18GL-18 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 533/15 | C |
| 32M x 18 | GS4576C18GL-24 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 400/15 | C |
| 32M x 18 | GS4576C18GL-25 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 400/20 | C |
| 32M x 18 | GS4576C18GL-33 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 300/20 | C |
| 16M x 36 | GS4576C36GL-18 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 533/15 | C |
| 16M x 36 | GS4576C36GL-24 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 400/15 | C |
| 16M x 36 | GS4576C36GL-25 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 400/20 | C |
| 16M x 36 | GS4576C36GL-33 | CIO LLD RAM II | RoHS-compliant 144-ball μBGA | 300/20 | C |
| 64M x 9 | GS4576C09L-18I | CIO LLD RAM II | 144-ball μBGA | 533/15 | I |
| 64M x 9 | GS4576C09L-24I | CIO LLD RAM II | 144-ball μBGA | 400/15 | I |
| 64M x 9 | GS4576C09L-25I | CIO LLD RAM II | 144-ball μBGA | 400/20 | I |

Note:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS4576C09-533T.
- C = Commercial Temperature Range. I = Industrial Temperature Range.

Ordering Information for GSI LLD RAM IIs (Continued)

| Org | Part Number ¹ | Type | Package | Speed (tCK/tRC) | T ² |
|----------|--------------------------|----------------|-----------------------------------|-----------------|----------------|
| 64M x 9 | GS4576C09L-33I | CIO LLD RAM II | 144-ball μ BGA | 300/20 | I |
| 32M x 18 | GS4576C18L-18I | CIO LLD RAM II | 144-ball μ BGA | 533/15 | I |
| 32M x 18 | GS4576C18L-24I | CIO LLD RAM II | 144-ball μ BGA | 400/15 | I |
| 32M x 18 | GS4576C18L-25I | CIO LLD RAM II | 144-ball μ BGA | 400/20 | I |
| 32M x 18 | GS4576C18L-33I | CIO LLD RAM II | 144-ball μ BGA | 300/20 | I |
| 16M x 36 | GS4576C36L-18I | CIO LLD RAM II | 144-ball μ BGA | 533/15 | I |
| 16M x 36 | GS4576C36L-24I | CIO LLD RAM II | 144-ball μ BGA | 400/15 | I |
| 16M x 36 | GS4576C36L-25I | CIO LLD RAM II | 144-ball μ BGA | 400/20 | I |
| 16M x 36 | GS4576C36L-33I | CIO LLD RAM II | 144-ball μ BGA | 300/20 | I |
| 64M x 9 | GS4576C09GL-18I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 533/15 | I |
| 64M x 9 | GS4576C09GL-24I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 400/15 | I |
| 64M x 9 | GS4576C09GL-25I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 400/20 | I |
| 64M x 9 | GS4576C09GL-33I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 300/20 | I |
| 32M x 18 | GS4576C18GL-18I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 533/15 | I |
| 32M x 18 | GS4576C18GL-24I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 400/15 | I |
| 32M x 18 | GS4576C18GL-25I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 400/20 | I |
| 32M x 18 | GS4576C18GL-33I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 300/20 | I |
| 16M x 36 | GS4576C36GL-18I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 533/15 | I |
| 16M x 36 | GS4576C36GL-24I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 400/15 | I |
| 16M x 36 | GS4576C36GL-25I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 400/20 | I |
| 16M x 36 | GS4576C36GL-33I | CIO LLD RAM II | RoHS-compliant 144-ball μ BGA | 300/20 | I |

Note:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS4576C09-533T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

576Mb LLDRAM II Datasheet Revision History

| DS/DateRev. Code: Old; New | Types of Changes Format or Content | Page;Revisions;Reason |
|-------------------------------|---------------------------------------|---|
| 4576Cxx_r1 | | • Creation of new datasheet |
| 4576Cxx_r1.00a | | <ul style="list-style-type: none"> • Revised Timing Diagrams • Modified Cycle Time and Read/Write Latency tables (pg. 19, 31.) • Updated Operating Conditions (pg. 46), AC Electrical Characteristics (pg. 48) |
| 4576Cxx_r1.00b | | • Changed FBGA references to μ BGA (including diagrams) |
| 4576Cxx_r1.01 | | • Various changes to prepare for public release |
| 4576Cxx_r1.02 | | <ul style="list-style-type: none"> • Added IDD Op Conditions • (Rev1.02b: corrected mechanical drawing) • (Rev1.02c: Editorial updates) • (Rev1.02d: Updated NOP commands from 3000 to 2048) • (Rev1.02e: Added Thermal Impedance numbers for 4-layer substrate) • (Rev1.02f: Changed all V_{SSQ} references to V_{SS}) |
| 4576Cxx_r1.03 | | <ul style="list-style-type: none"> • Changed DLL Reset to 1024 cycles (page 10) • Corrected typos/wording errors in TAP section • (Rev1.03a: Changed NOP time from 2048 to 1024) |
| 4576Cxx_r1.04 | | • Updated to reflect MP status |

Not Recommended for New Design - Discontinued Product

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А