

512K x 8 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM

AUGUST 2009

FEATURES

HIGH SPEED: (IS61/64WV5128ALL/BLL)

- High-speed access time: 8, 10, 20 ns
- Low Active Power: 85 mW (typical)
- Low stand-by power: 7 mW (typical)
CMOS standby

LOW POWER: (IS61/64WV5128ALS/BLS)

- High-speed access time: 25, 35 ns
- Low Active Power: 35 mW (typical)
- Low stand-by power: 0.6 mW (typical)
CMOS standby
- Single power supply
 - V_{DD} 1.65V to 2.2V (IS61WV5128Axx)
 - V_{DD} 2.4V to 3.6V (IS61/64WV5128Bxx)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

The *ISSI* IS61WV5128Axx and IS61/64WV5128Bxx are very high-speed, low power, 524,288-word by 8-bit CMOS static RAMs. The IS61WV5128Axx and IS61/64WV5128Bxx are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

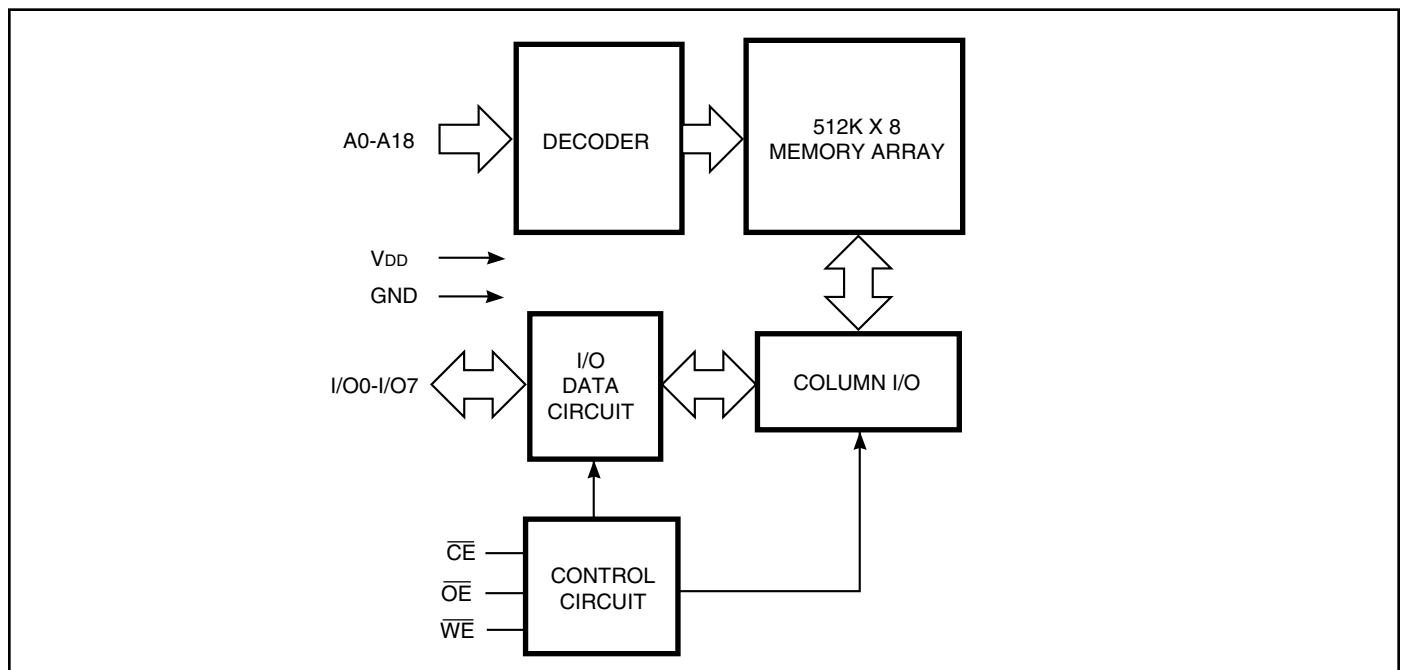
When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61WV5128Axx and IS61/64WV5128Bxx operate from a single power supply.

The IS61WV5128ALL and IS61/64WV5128BLL are available in 36-pin 400-mil SOJ, 36-pin mini BGA, and 44-pin TSOP (Type II) packages.

The IS61WV5128ALS and IS61/64WV5128BLS are available in 32-pin TSOP (Type I), 32-pin sTSOP (Type I), 32-pin SOP and 32-pin TSOP (Type II) packages.

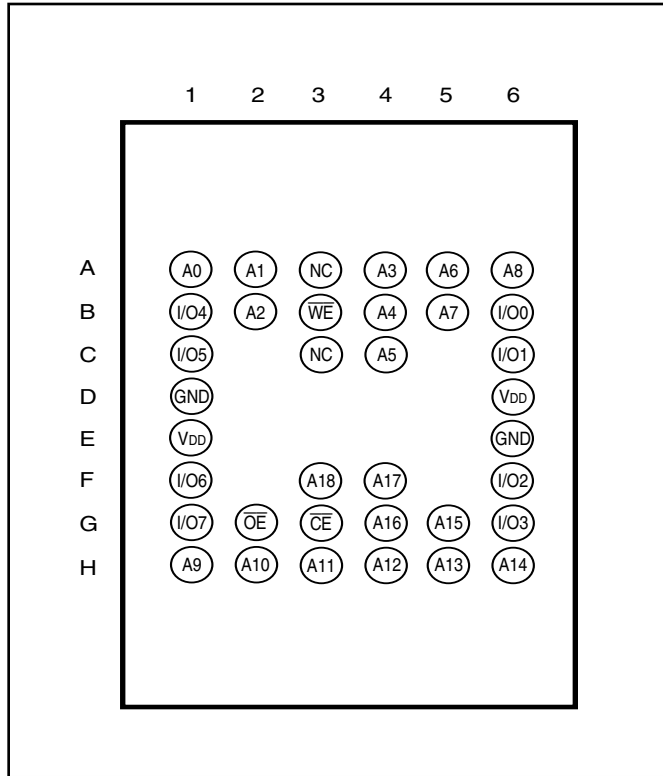
FUNCTIONAL BLOCK DIAGRAM



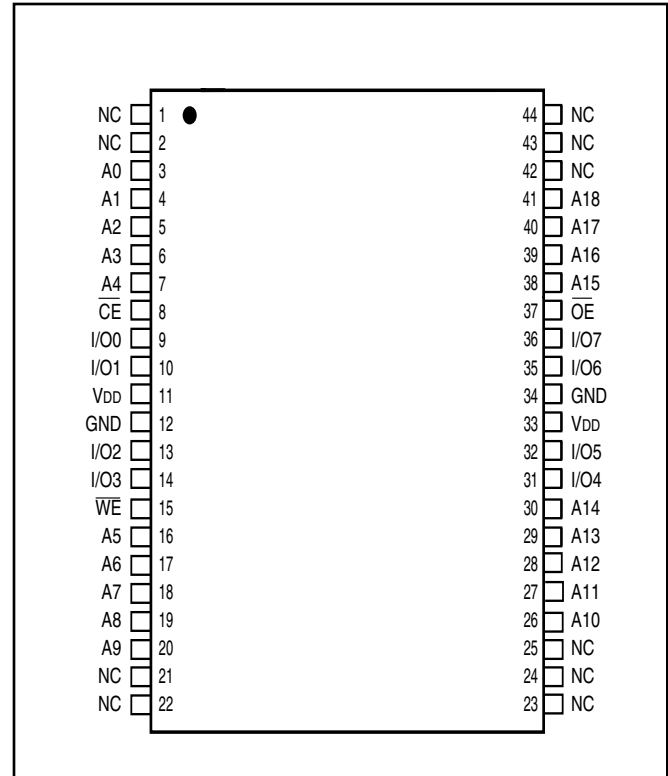
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PIN CONFIGURATION (HIGH SPEED) (61/64WV5128ALL/BLL)

36 mini BGA



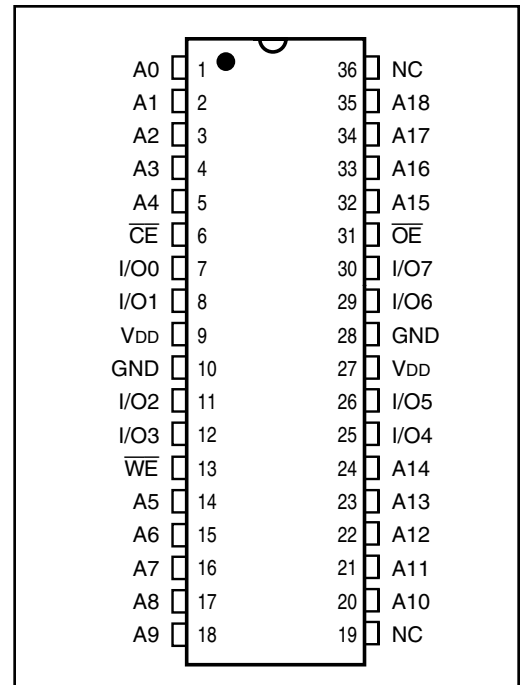
44-Pin TSOP (Type II)



PIN DESCRIPTIONS

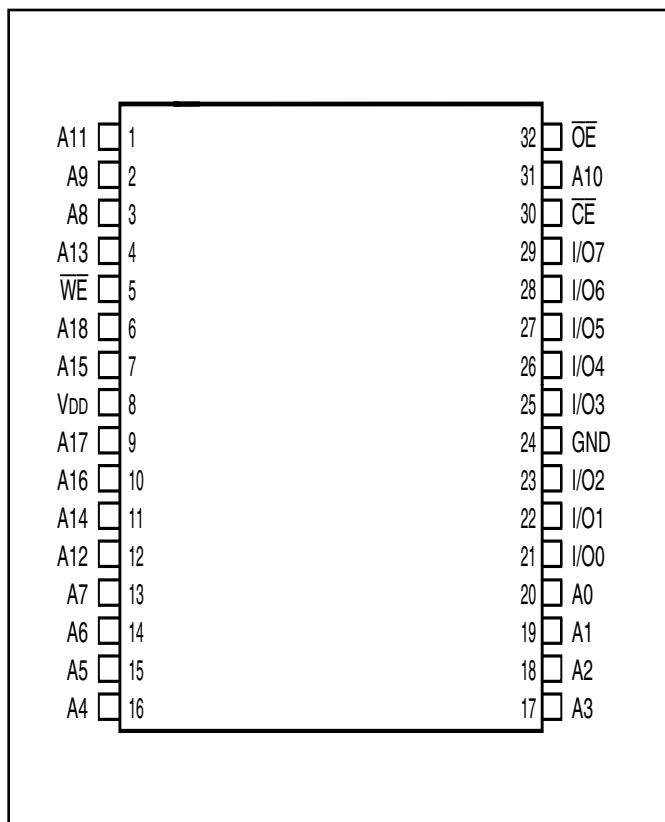
| | |
|-----------------|---------------------|
| A0-A18 | Address Inputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Bidirectional Ports |
| V _{DD} | Power |
| GND | Ground |
| NC | No Connection |

36-Pin SOJ

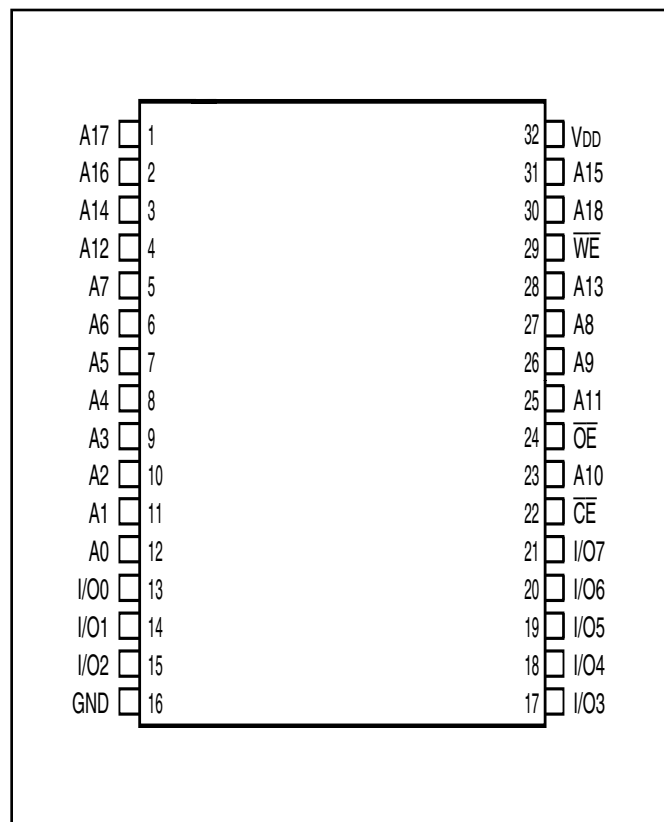


PIN CONFIGURATION (LOW POWER) (61/64WV5128ALS/BLS)

32-pin TSOP (TYPE I), (Package Code T)
32-pin sTSOP (TYPE I) (Package Code H)



32-pin SOP
32-pin TSOP (TYPE II)
(Package Code T2)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------|
| A0-A18 | Address Inputs |
| \overline{CE} | Chip Enable 1 Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| VDD | Power |
| GND | Ground |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -4.0 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 8.0 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width <10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1.0 mA | 1.8 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 1.0 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width <10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|--------------------------------|---------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min, I _{OH} = -0.1 mA | 1.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min, I _{OL} = 0.1 mA | — | 0.2 | V |
| V _{IH} | Input HIGH Voltage | | 1.4 | V _{DD} + 0.2 | V |
| V _{IL} ⁽¹⁾ | Input LOW Voltage | | -0.2 | 0.4 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width <10 ns). Not 100% tested.

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | I/O Operation | V _{DD} Current |
|------------------------------|-----------------|-----------------|-----------------|------------------|-------------------------|
| Not Selected (Power-down) | X | H | X | High-Z | ISB1, ISB2 |
| Output Disabled | H | L | H | High-Z | I _{CC} |
| Read | H | L | L | D _{OUT} | I _{CC} |
| Write | L | L | X | D _{IN} | I _{CC} |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | V _{DD} Relates to GND | -0.3 to 4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

HIGH SPEED (IS61WV5128ALL/BLL)

OPERATING RANGE (V_{DD}) (IS61WV5128ALL)

| Range | Ambient Temperature | V _{DD} | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C | 1.65V-2.2V | 20ns |
| Industrial | -40°C to +85°C | 1.65V-2.2V | 20ns |
| Automotive | -40°C to +125°C | 1.65V-2.2V | 20ns |

OPERATING RANGE (V_{DD}) (IS61WV5128BLL)⁽¹⁾

| Range | Ambient Temperature | V _{DD} (8 ns) ¹ | V _{DD} (10 ns) ¹ |
|------------|---------------------|-------------------------------------|--------------------------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 2.4V-3.6V |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 2.4V-3.6V |

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV5128BLL)

| Range | Ambient Temperature | V _{DD} (10 ns) |
|------------|---------------------|-------------------------|
| Automotive | -40°C to +125°C | 2.4V-3.6V |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 | | -10 | | -20 | | Unit |
|------------------|--|--|---------------------|------|------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 50 | — | 40 | — | 40 | mA |
| | | | Ind. | — | 55 | — | 45 | — | 45 | |
| | | | Auto. | — | — | — | 65 | — | 65 | |
| | | | typ. ⁽²⁾ | — | — | 25 | — | — | | |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = 0 | Com. | — | 35 | — | 35 | — | 30 | mA |
| | | | Ind. | — | 40 | — | 40 | — | 40 | |
| | | | Auto. | — | — | — | 60 | — | 60 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0 | Com. | — | 10 | — | 10 | — | 10 | mA |
| | | | Ind. | — | 15 | — | 15 | — | 15 | |
| | | | Auto. | — | — | — | 30 | — | 30 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 7 | — | 7 | — | 7 | mA |
| | | | Ind. | — | 10 | — | 10 | — | 10 | |
| | | | Auto. | — | — | — | 20 | — | 20 | |
| | | | typ. ⁽²⁾ | — | — | 2 | — | — | | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

LOW POWER (IS61WV5128ALS/BLS)

OPERATING RANGE (V_{DD}) (IS61WV5128ALS)

| Range | Ambient Temperature | V _{DD} | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C | 1.65V-2.2V | 35ns |
| Industrial | -40°C to +85°C | 1.65V-2.2V | 35ns |
| Automotive | -40°C to +125°C | 1.65V-2.2V | 35ns |

OPERATING RANGE (V_{DD}) (IS61WV5128BLS)⁽¹⁾

| Range | Ambient Temperature | V _{DD} | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C | 2.4V-3.6V | 25 ns |
| Industrial | -40°C to +85°C | 2.4V-3.6V | 25 ns |

OPERATING RANGE (V_{DD}) (IS64WV5128BLS)

| Range | Ambient Temperature | V _{DD} | Speed |
|------------|---------------------|-----------------|-------|
| Automotive | -40°C to +125°C | 2.4V-3.6V | 35 ns |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -25 | | -35 | | Unit |
|------------------|--|--|---------------------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 20 | — | 20 | mA |
| | | | Ind. | — | 25 | — | 25 | |
| | | | Auto. | — | 50 | — | 50 | |
| | | | typ. ⁽²⁾ | 11 | | | | |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = 0 | Com. | — | 10 | — | 10 | mA |
| | | | Ind. | — | 12 | — | 12 | |
| | | | Auto. | — | 20 | — | 20 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} CE ≥ V _{IH} , f = 0 | Com. | — | 5 | — | 5 | mA |
| | | | Ind. | — | 7 | — | 7 | |
| | | | Auto. | — | 10 | — | 10 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., CE ≥ V _{DD} - 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 1 | — | 1 | mA |
| | | | Ind. | — | 2 | — | 2 | |
| | | | Auto. | — | 10 | — | 10 | |
| | | | typ. ⁽²⁾ | 0.2 | | | | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

AC TEST CONDITIONS

| Parameter | Unit (2.4V-3.6V) | Unit (3.3V ± 10%) | Unit (1.65V-2.2V) |
|--|---------------------|----------------------|----------------------|
| Input Pulse Level | 0V to 3V | 0V to 3V | 0V to 1.8V |
| Input Rise and Fall Times | 1V/ ns | 1V/ ns | 1V/ ns |
| Input and Output Timing and Reference Level (V _{Ref}) | 1.5V | 1.5V | 0.9V |
| Output Load | See Figures 1 and 2 | See Figures 1 and 2 | See Figures 1 and 2 |

AC TEST LOADS

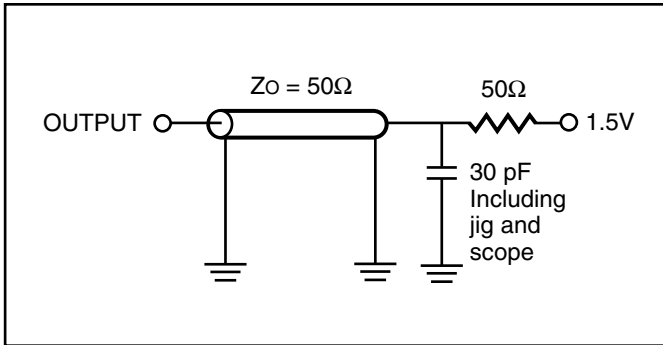


Figure 1.

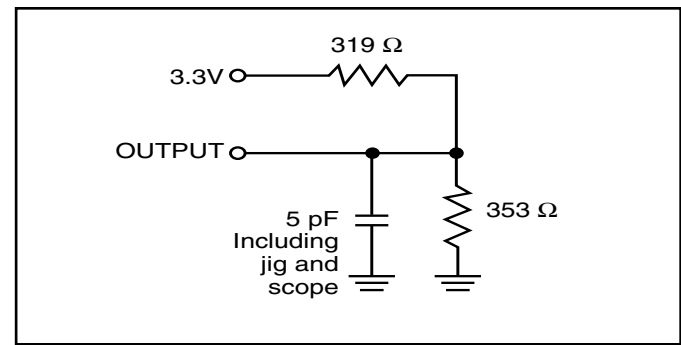


Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|---------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | ns |
| t _{OHA} | Output Hold Time | 2.0 | — | 2.0 | — | ns |
| t _{ACE} | CE Access Time | — | 8 | — | 10 | ns |
| t _{DOE} | OE Access Time | — | 4.5 | — | 4.5 | ns |
| t _{HZOE⁽²⁾} | OE to High-Z Output | — | 3 | — | 4 | ns |
| t _{LZOE⁽²⁾} | OE to Low-Z Output | 0 | — | 0 | — | ns |
| t _{HZCE⁽²⁾} | CE to High-Z Output | 0 | 3 | 0 | 4 | ns |
| t _{LZCE⁽²⁾} | CE to Low-Z Output | 3 | — | 3 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 8 | — | 10 | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

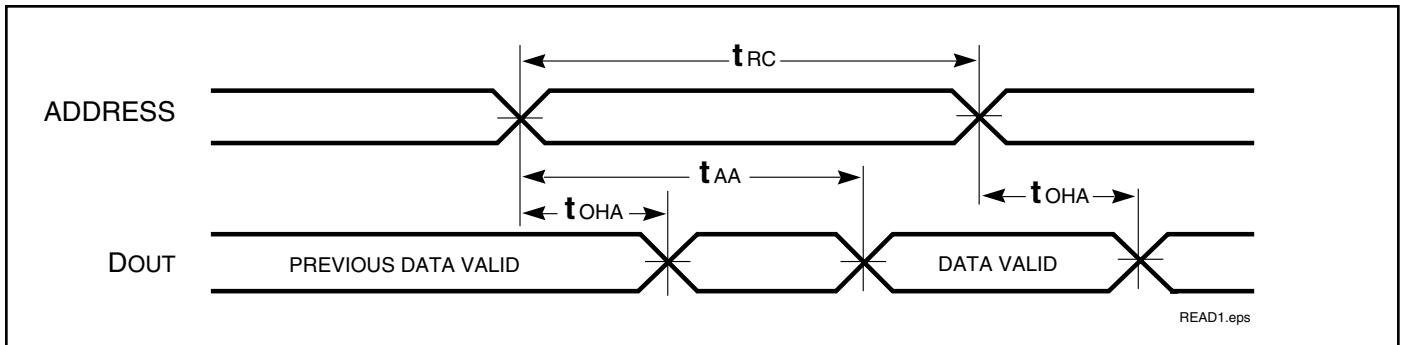
| Symbol | Parameter | -20 ns | | -25 ns | | -35 ns | | Unit |
|----------------------------------|---|--------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| t _{AA} | Address Access Time | — | 20 | — | 25 | — | 35 | ns |
| t _{OHA} | Output Hold Time | 2.5 | — | 4 | — | 4 | — | ns |
| t _{ACE} | $\overline{\text{CE}}$ Access Time | — | 20 | — | 25 | — | 35 | ns |
| t _{DOE} | $\overline{\text{OE}}$ Access Time | — | 8 | — | 12 | — | 15 | ns |
| t _{HZOE} ⁽²⁾ | $\overline{\text{OE}}$ to High-Z Output | 0 | 8 | 0 | 8 | 0 | 10 | ns |
| t _{LZOE} ⁽²⁾ | $\overline{\text{OE}}$ to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |
| t _{HZCE} ⁽²⁾ | $\overline{\text{CE}}$ to High-Z Output | 0 | 8 | 0 | 8 | 0 | 10 | ns |
| t _{LZCE} ⁽²⁾ | $\overline{\text{CE}}$ to Low-Z Output | 3 | — | 10 | — | 10 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 20 | — | 25 | — | 35 | ns |

Notes:

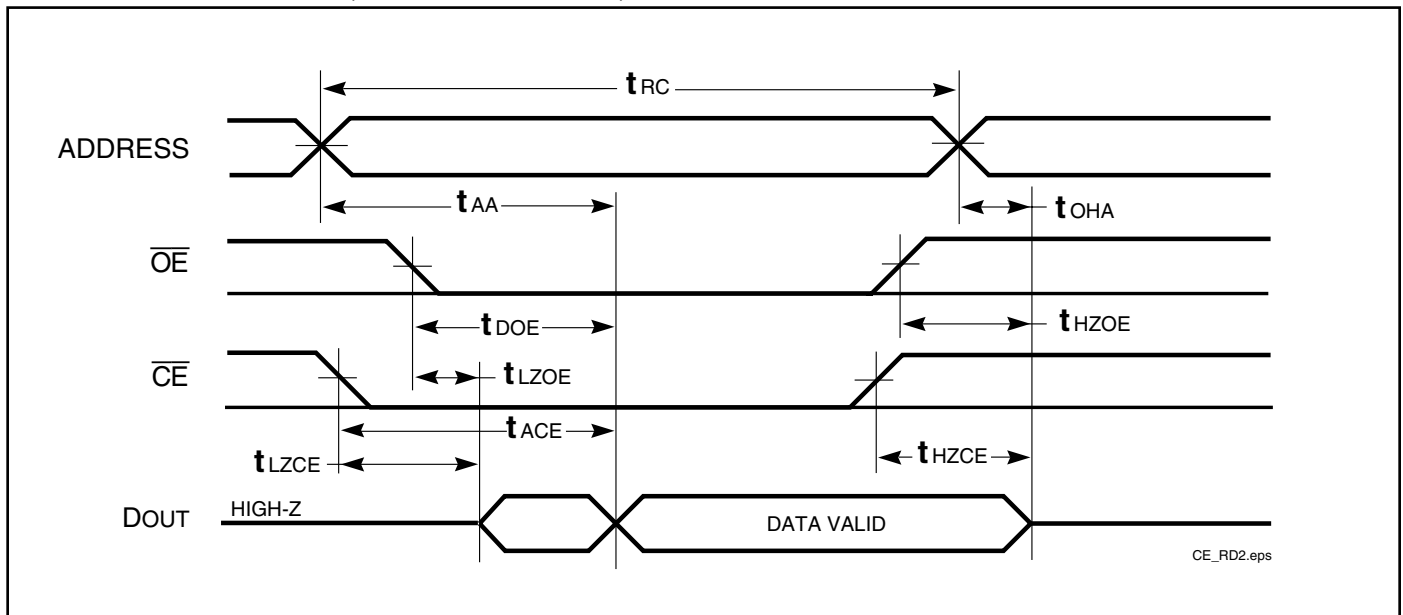
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) (\overline{CE} and \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|---|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 6.5 | — | 8 | — | ns |
| t _{AW} | Address Setup Time to Write End | 6.5 | — | 8 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 6.5 | — | 8 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 8.0 | — | 10 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 3.5 | — | 5 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 2 | — | 2 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

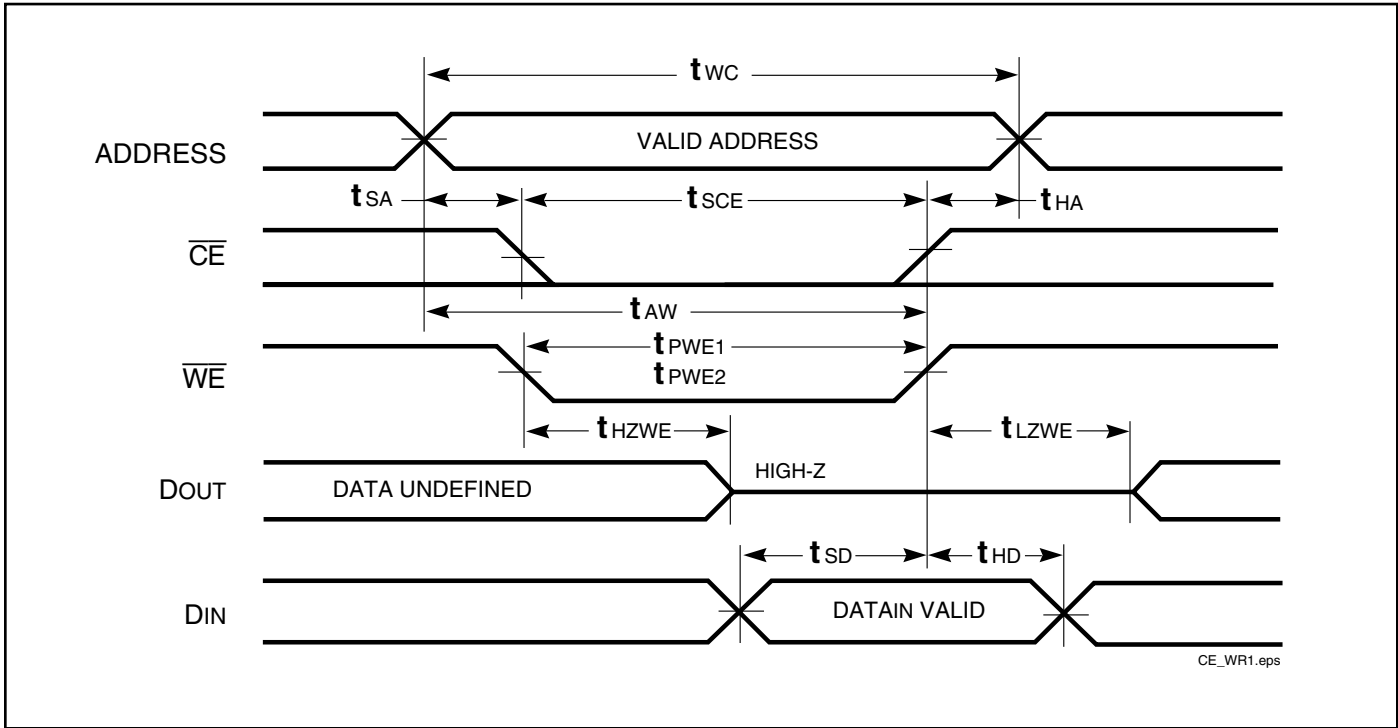
| Symbol | Parameter | -20 ns | | -25 ns | | -35 ns | | Unit |
|---------------------------------|---------------------------------|--------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| t _{SCE} | CE to Write End | 12 | — | 18 | — | 25 | — | ns |
| t _{AW} | Address Setup Time to Write End | 12 | — | 15 | — | 25 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PWE1} | WE Pulse Width (OE = HIGH) | 12 | — | 18 | — | 30 | — | ns |
| t _{PWE2} | WE Pulse Width (OE = LOW) | 17 | — | 20 | — | 30 | — | ns |
| t _{SD} | Data Setup to Write End | 9 | — | 12 | — | 15 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{HZWE⁽³⁾} | WE LOW to High-Z Output | — | 9 | — | 12 | — | 20 | ns |
| t _{LZWE⁽³⁾} | WE HIGH to Low-Z Output | 3 | — | 5 | — | 5 | — | ns |

Notes:

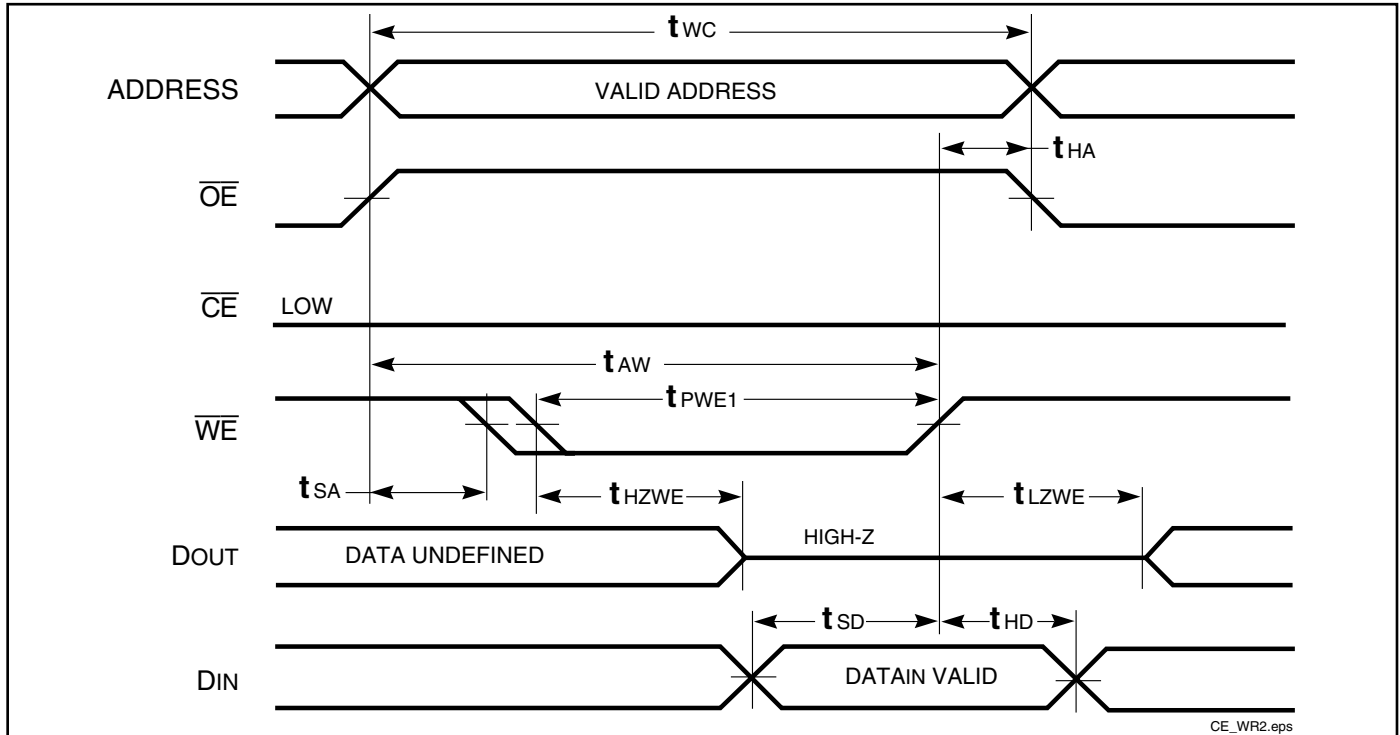
1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)



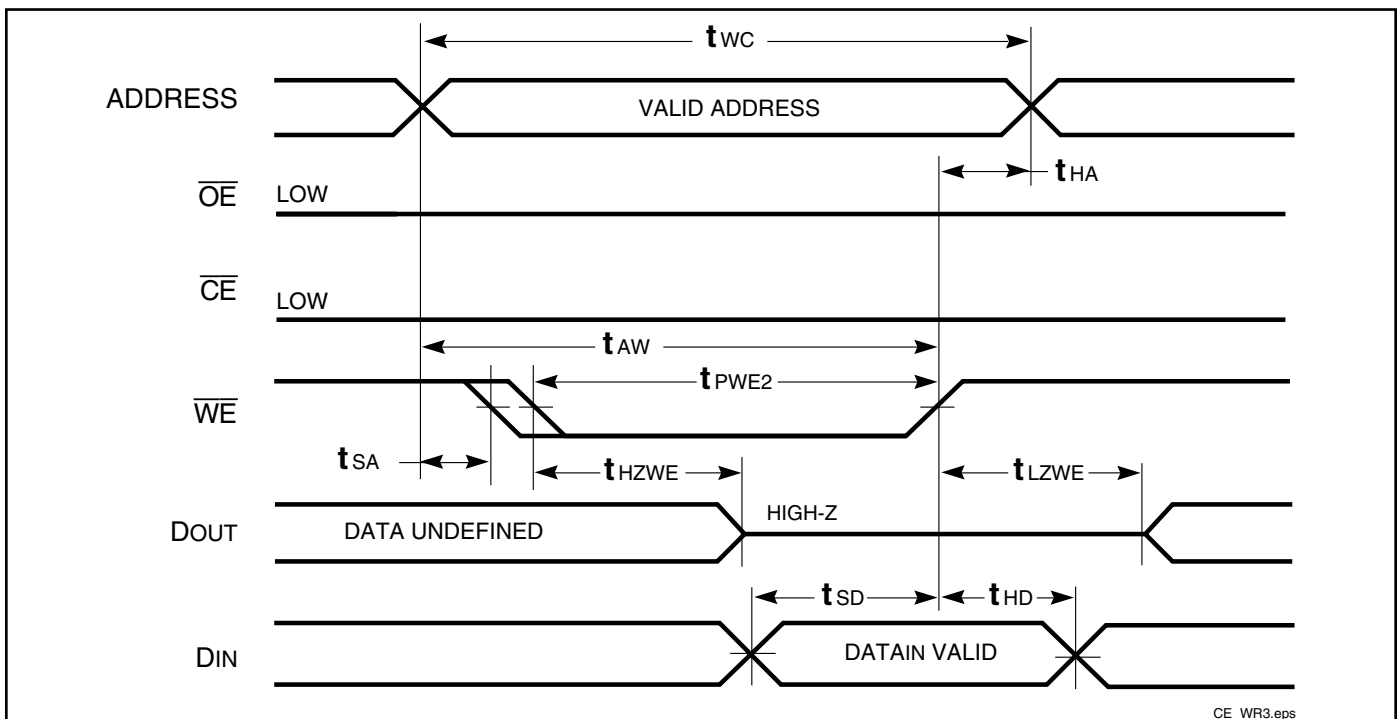
WRITE CYCLE NO. 2^(1,2) (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)



HIGH SPEED (IS61WV5128ALL/BLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|--|-----------------------|-----------------|---------------------|--------------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. Ind. Auto. | — | 2 | 6 8 15 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | — | — | ns |

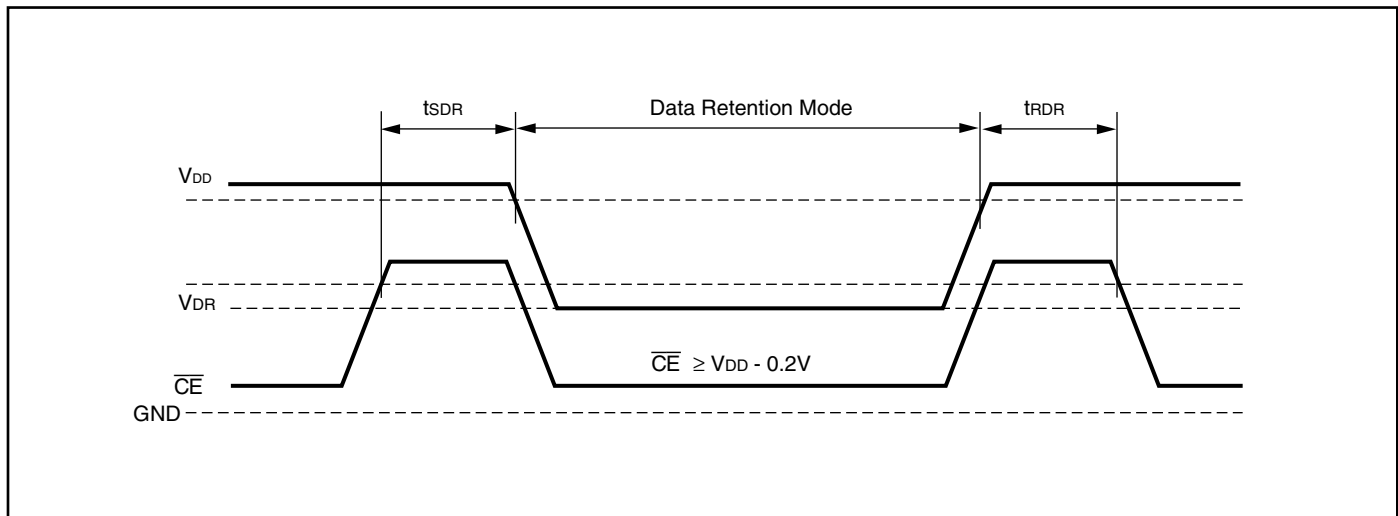
Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|--|--------------|-----------------|---------------------|--------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | | 1.2 | — | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. Ind. | — | 2 | 6 8 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | — | — | ns |

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



LOW POWER (IS61WV5128ALS/BLS)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|---|-----------------------|-----------------|---------------------|--------------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 2.0V, CE ≥ V _{DD} - 0.2V | Com. Ind. Auto. | — | 0.2 | 1 2 10 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | — | — | ns |

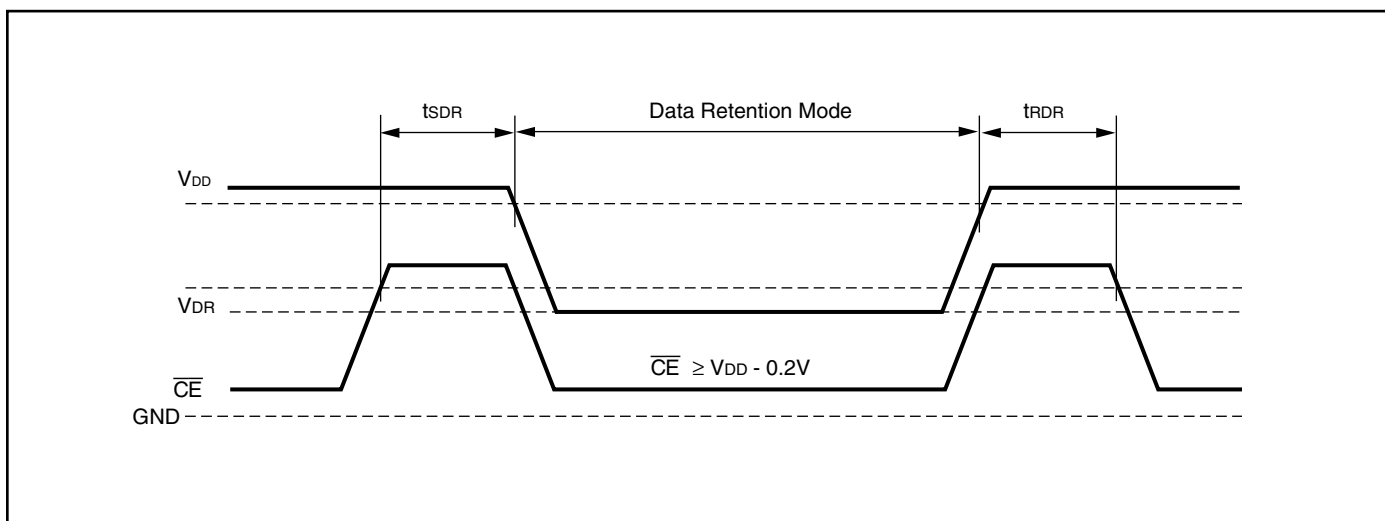
Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|---|--------------|-----------------|---------------------|--------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | | 1.2 | — | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 1.2V, CE ≥ V _{DD} - 0.2V | Com. Ind. | — | 0.2 | 1 2 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | — | — | ns |

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION (HIGH SPEED)

Commercial Range: 0°C to +70°C

Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|----------------------|--------------------|---------------------------|
| 10 (8 ¹) | IS61WV5128BLL-10TL | TSOP (Type II), Lead-free |

Note:

1. Speed = 8ns for V_{DD} = 3.3V ± 5%. Speed = 10ns for V_{DD} = 2.4V to 3.6V.

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|----------------------|---------------------|---|
| 10 (8 ¹) | IS61WV5128BLL-10BI | 36-ball mini BGA (6mm x 8mm) |
| | IS61WV5128BLL-10BLI | 36-ball mini BGA (6mm x 8mm), Lead-free |
| | IS61WV5128BLL-10TI | TSOP (Type II) |
| | IS61WV5128BLL-10TLI | TSOP (Type II), Lead-free |
| | IS61WV5128BLL-10KLI | 400-mil Plastic SOJ, Lead-free |

Note:

1. Speed = 8ns for V_{DD} = 3.3V ± 5%. Speed = 10ns for V_{DD} = 2.4V to 3.6V.

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|------------|--------------------|------------------------------|
| 20 | IS61WV5128ALL-20BI | 36-ball mini BGA (6mm x 8mm) |
| | IS61WV5128ALL-20TI | TSOP (Type II) |

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|------------|-----------------------|---|
| 10 | IS64WV5128BLL-10BA3 | 36-ball mini BGA (6mm x 8mm) |
| | IS64WV5128BLL-10BLA3 | 36-ball mini BGA (6mm x 8mm), Lead-free |
| | IS64WV5128BLL-10CTA3 | TSOP (Type II), Copper Leadframe |
| | IS64WV5128BLL-10CTLA3 | TSOP (Type II), Copper Leadframe Lead-free |

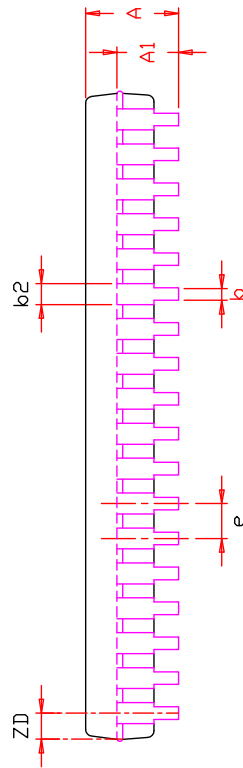
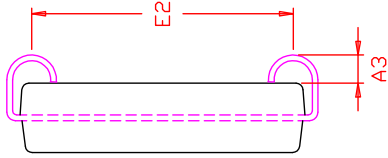
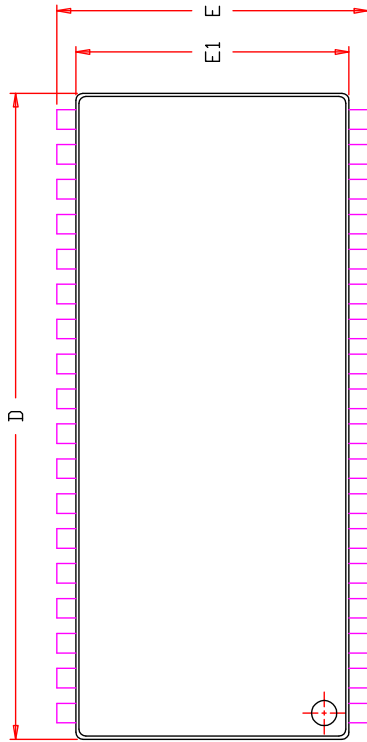


ORDERING INFORMATION (LOW POWER)

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|-------------------|-----------------------|---------------------------|
| 25 | IS61WV5128BLS-25TLI | TSOP (Type II), Lead-free |



| SYMBOL | DIMENSION IN MM | | DIMENSION IN INCH | |
|--------|-----------------|-------|-------------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 3.25 | 3.76 | 0.128 | 0.148 |
| A1 | 2.08 | | 0.082 | |
| A3 | 0.635 | | 0.025 | |
| b | 0.38 | 0.51 | 0.015 | 0.020 |
| b2 | 0.66 | 0.71 | 0.026 | 0.028 |
| D | 23.36 | 23.49 | 0.920 | 0.930 |
| E | 11.05 | 11.18 | 0.435 | 0.440 |
| E1 | 10.03 | 10.16 | 0.395 | 0.400 |
| E2 | 9.40 | BSC. | 0.370 | BSC. |
| e | 1.27 | BSC. | 0.050 | BSC. |
| ZD | 0.95 | REF. | 0.037 | REF. |

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.



TITLE

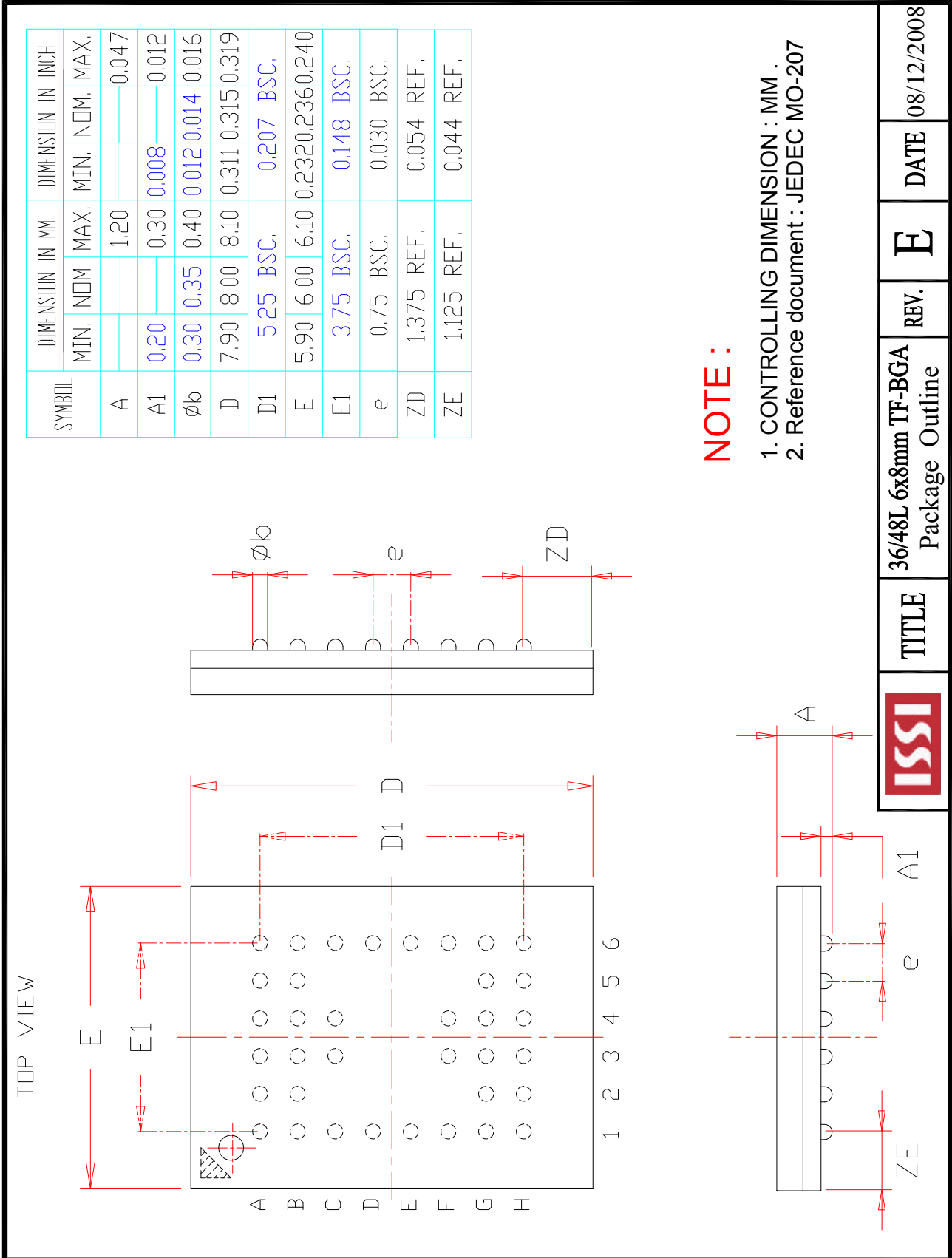
36L 400mil SOJ
Package Outline

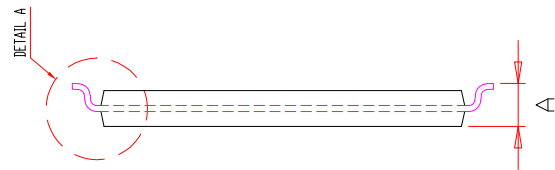
REV.

F

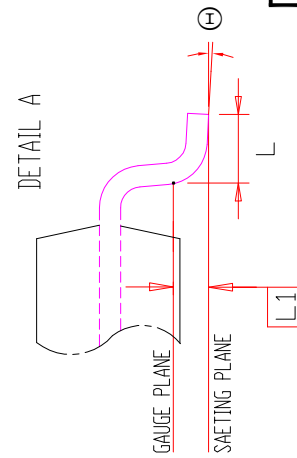
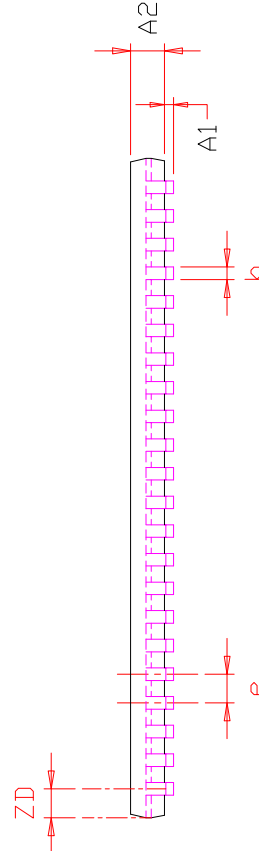
DATE

12/20/2007





| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|-----------|-----------------|--------------|--------------|-------------------|---------------|--------------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | | 1.20 | 0.039 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| k | 0.30 | | 0.45 | 0.012 | | 0.018 |
| D | 18.28 | 18.41 | 18.54 | 0.7200 | 0.7250 | 0.730 |
| E | 11.56 | 11.76 | 11.96 | 0.4550 | 0.4630 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.3950 | 0.4000 | 0.405 |
| e | 0.80 | BSC. | 0.031 | BSC. | | |
| L | 0.40 | | 0.69 | 0.016 | | 0.027 |
| L1 | 0.25 | BSC. | | 0.010 | BSC. | |
| ZD | 0.805 | REF. | 0.032 | REF. | | |
| ⊕ | 0 | | 8° | 0 | | 8° |



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

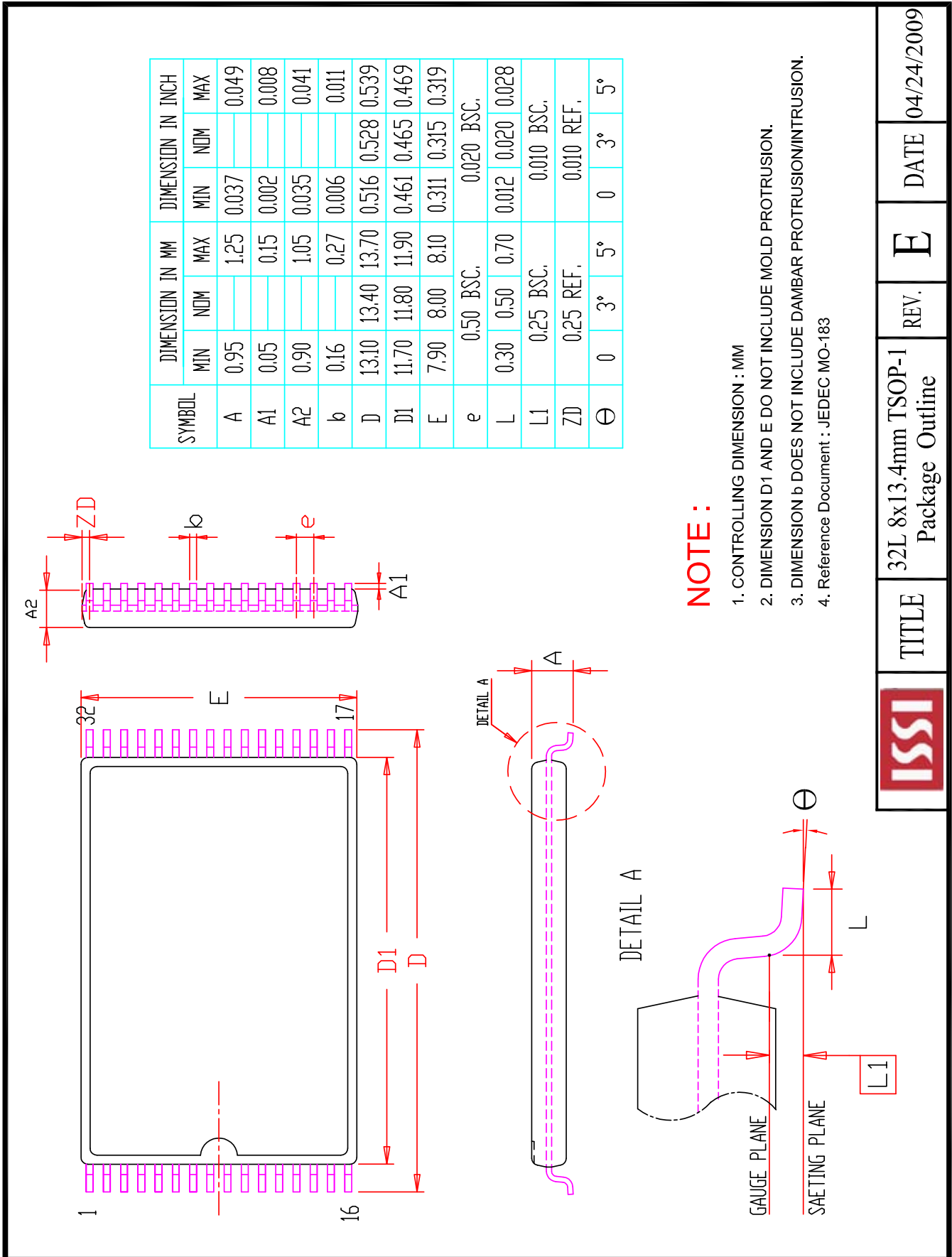
44L 400mil TSOP-2
Package Outline

REV.

F

DATE

06/04/2008

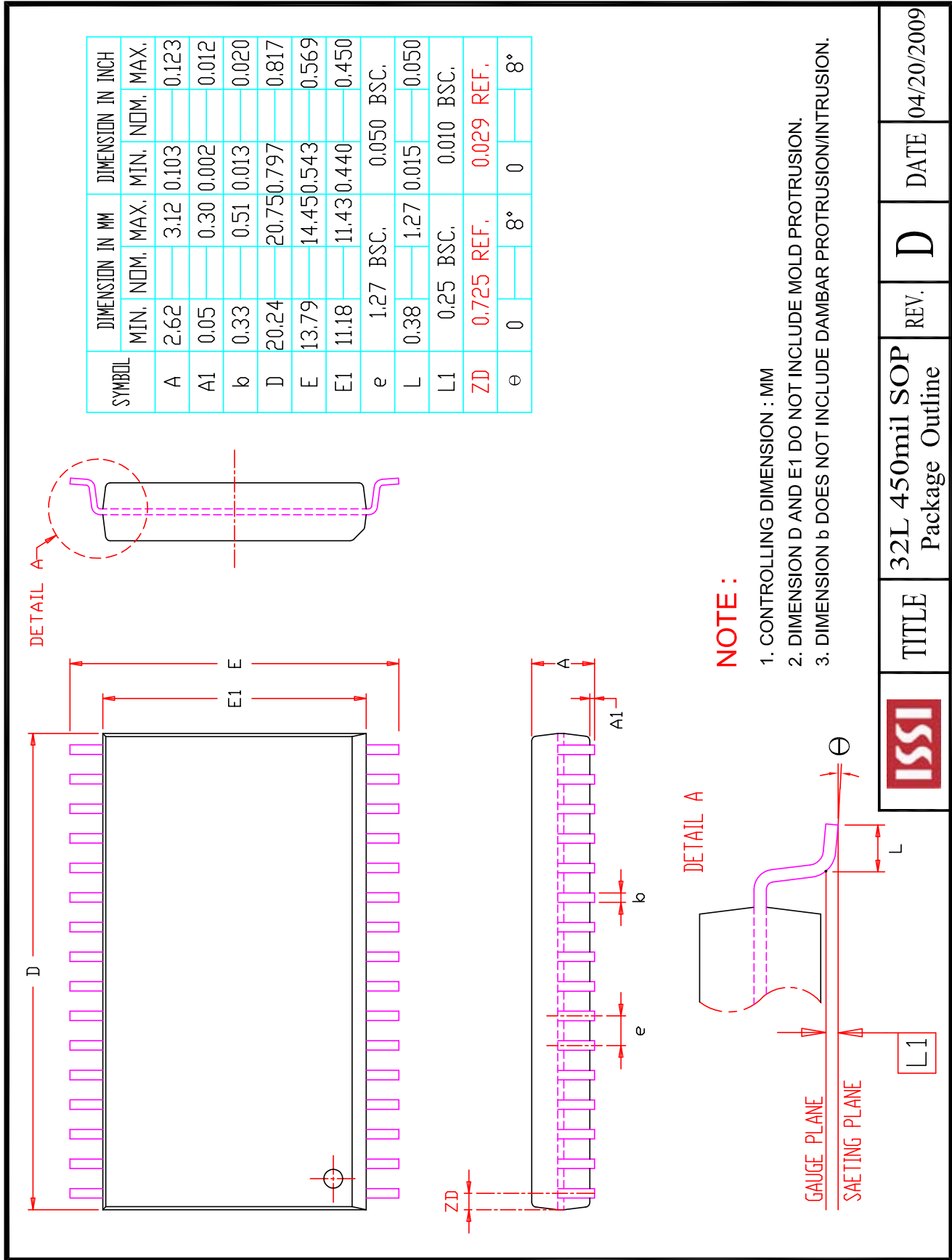


| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|----------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.95 | | 1.25 | 0.037 | | 0.049 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.008 |
| A2 | 0.90 | | 1.05 | 0.035 | | 0.041 |
| b | 0.16 | | 0.27 | 0.006 | | 0.011 |
| D | 13.10 | 13.40 | 13.70 | 0.516 | 0.528 | 0.539 |
| D1 | 11.70 | 11.80 | 11.90 | 0.461 | 0.465 | 0.469 |
| E | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| L | 0.30 | 0.50 | 0.70 | 0.012 | 0.020 | 0.028 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.25 REF. | | | 0.010 REF. | | |
| Θ | 0 | 3° | 5° | 0 | 3° | 5° |

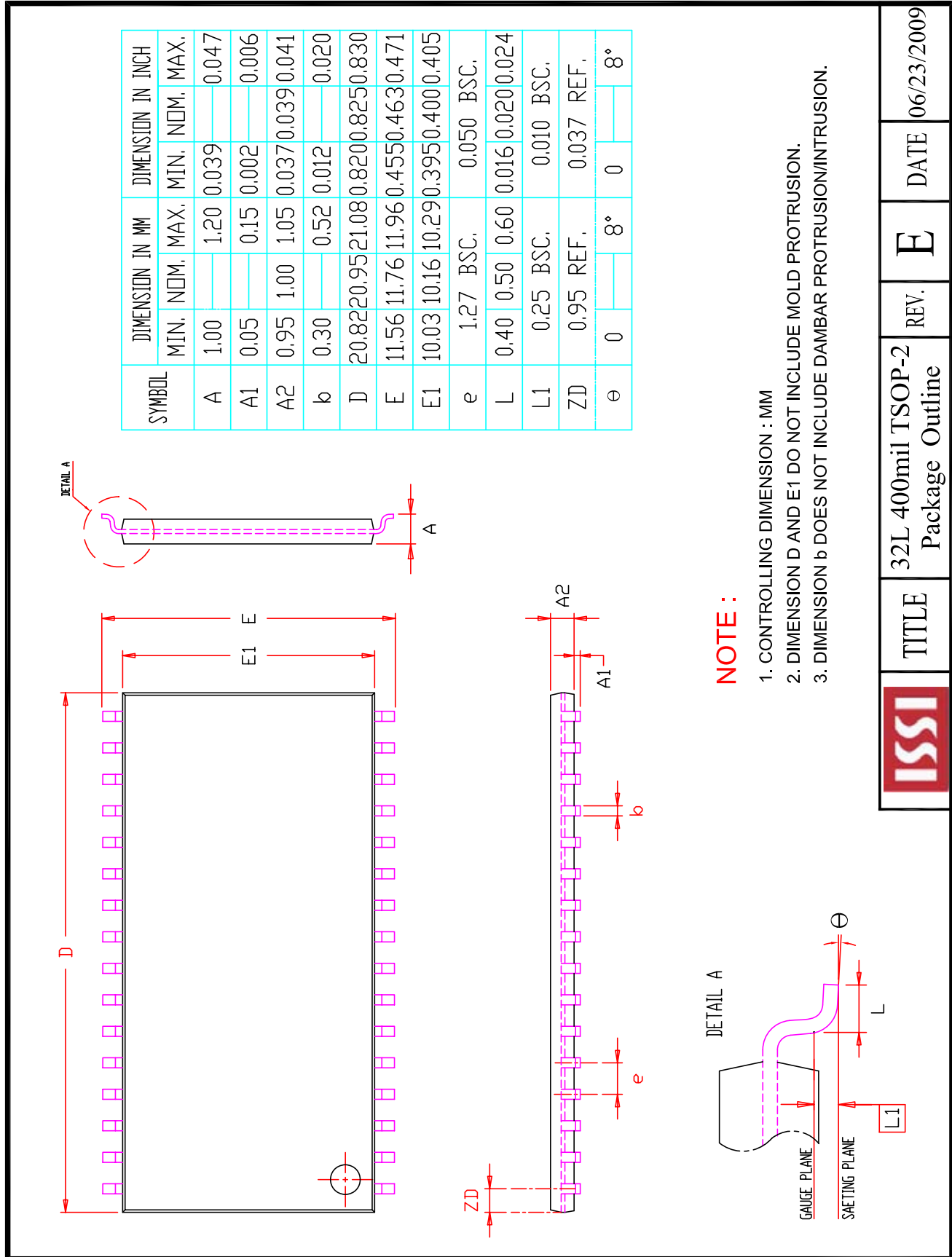
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

| | | | |
|--|--|------|------------|
| | TITLE | REV. | DATE |
| | 32L 8x13.4mm TSOP-1 Package Outline | E | 04/24/2009 |



| | | | | | | |
|--|-------|-----------------------------------|------|---|------|------------|
| | TITLE | 32L 450mil SOP Package Outline | REV. | D | DATE | 04/20/2009 |
|--|-------|-----------------------------------|------|---|------|------------|



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|----------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | | 1.20 | 0.039 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | | 0.52 | 0.012 | | 0.020 |
| D | 20.82 | 20.95 | 21.08 | 0.820 | 0.825 | 0.830 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 1.27 BSC. | | | 0.050 BSC. | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.95 REF. | | | 0.037 REF. | | |
| θ | 0 | | 8° | 0 | | 8° |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| | | | |
|--|--------------------------------------|------|------------|
| | TITLE | REV. | DATE |
| | 32L 400mil TSOP-2 Package Outline | E | 06/23/2009 |

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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