

RAA210870

Pin-Configurable 70A DC/DC Power Module with PMBus Interface

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The [RAA210870](#) is a pin-strap configurable 70A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally enhanced HDA packaging technology, the module can deliver up to 70A of continuous output current without the need for airflow or additional heat sinking. The RAA210870 simplifies configuration and control of Renesas [digital power technology](#) while offering an upgrade path to full PMBus configuration through the pin-compatible ISL8273M.

Operating over an input voltage range of 4.5V to 14V, the RAA210870 offers adjustable output voltages down to 0.6V and achieves up to 93% conversion efficiencies. A unique ChargeMode™ control architecture provides a single clock cycle response to an output load step and can support switching frequencies up to 1MHz. The power module integrates all power and most passive components and requires only a few external components to operate. A set of external resistors allows the user to easily configure the device for standard operation. A standard PMBus interface addresses fault management, in addition to real-time full telemetry and point-of-load monitoring.

A fully customizable voltage, current, and temperature protection scheme ensures safe operation for the RAA210870 under abnormal operating conditions. The device is also supported by the PowerNavigator™ software, a full digital power train development environment.

The RAA210870 is available in a low profile compact 18mmx23mmx7.5mm fully encapsulated thermally enhanced HDA package.

Applications

- Server, telecommunications, storage, and data communications
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

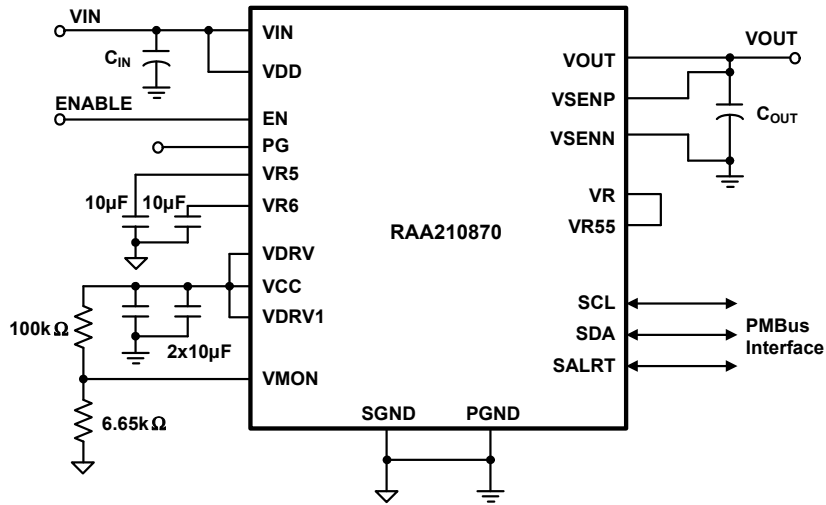
Features

- 70A single channel output current
 - 4.5V to 14V single rail input voltage
 - Up to 93% efficiency
- Programmable output voltage
 - 0.6V to 2.5V output voltage settings
 - ±1.2% accuracy over line, load, and temperature
- ChargeMode control loop architecture
 - 296kHz to 1.06MHz fixed switching frequency operations
 - No compensation required
 - Fast single clock cycle transient response
- PMBus interface and/or pin-strap mode
 - Programmable through PMBus
 - Pin-strap mode for standard settings
 - Real-time telemetry for V_{IN} , V_{OUT} , I_{OUT} , temperature, duty cycle, and f_{SW}
- Complete over/undervoltage, current, and temperature protections with fault logging
- [PowerNavigator](#) supported
- Thermally enhanced 18mmx23mmx7.5mm HDA package

Related Literature

For a full list of related documents, visit our website

- [RAA210870](#) product page



Note: Figure 1 represents a typical implementation of the RAA210870.
 For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

Figure 1. 70A Application Circuit

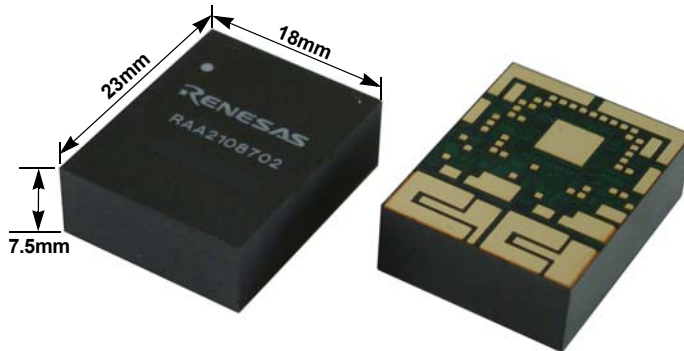


Figure 2. A Small Package for High Power Density

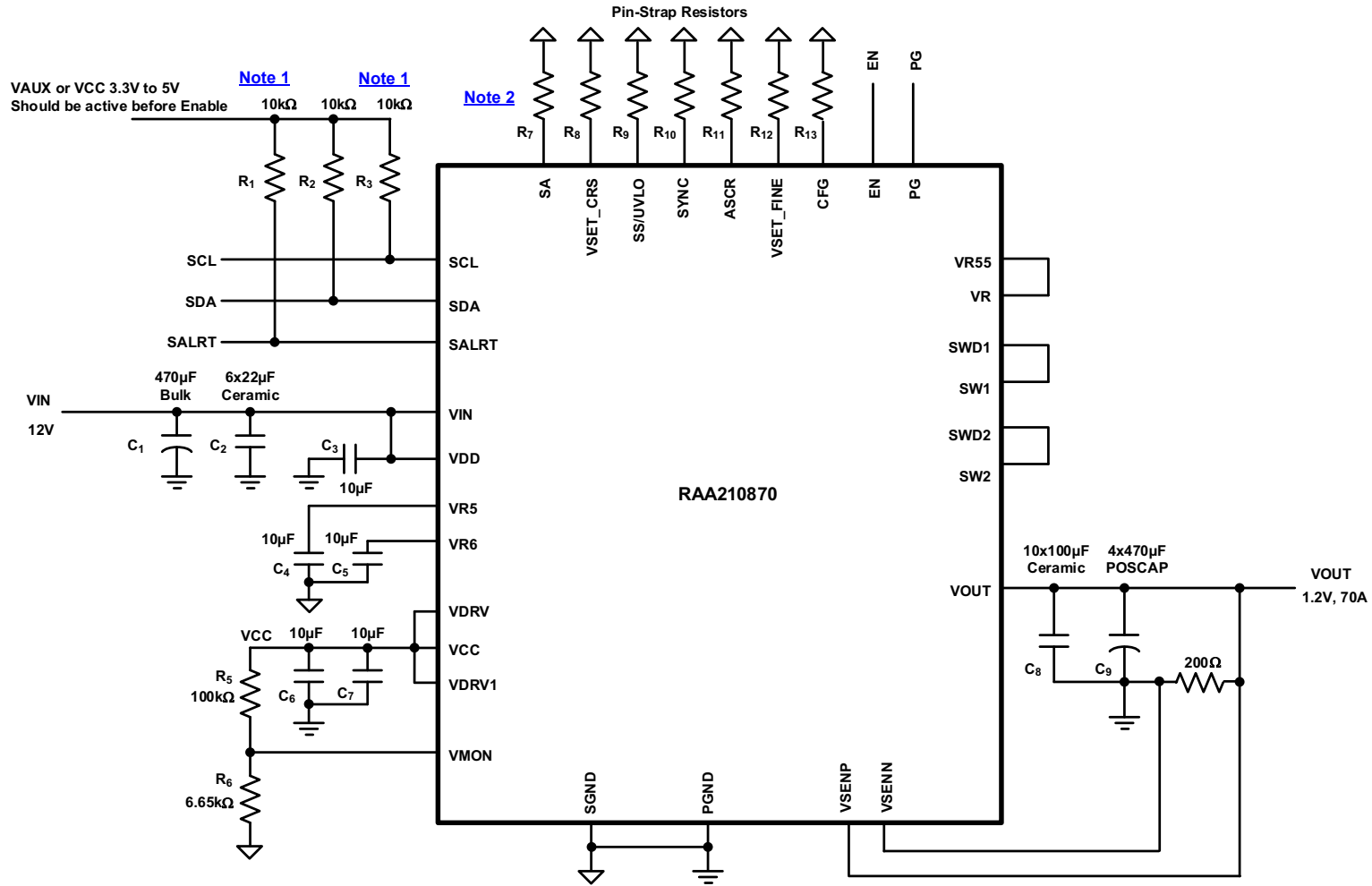
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1. Overview

1.1 Typical Application Circuit - Single Module



Notes:

1. R₂ and R₃ are not required if the PMBus host already has I²C pull-up resistors.
2. R₇ through R₁₂ can be selected according to the tables for the pin-strap resistor setting in this document.
3. V₂₅, VR, and VR55 do not need external capacitors. V₂₅ can be no connection.

Figure 3. Typical Application Circuit - Single Module

Table 1. RAA210870 Design Guide Matrix and Output Voltage Response

| V _{IN} (V) | V _{OUT} (V) | C _{OUT} (Bulk) (μF) | C _{OUT} (Ceramic) (μF) | ASCR Residual (Note 7) | ASCR Gain (Note 7) | P-P Deviation (mV) | Recovery Time (μs) | Load Step (A) (Note 6) | Freq. (kHz) |
|---------------------|----------------------|------------------------------|---------------------------------|------------------------|--------------------|--------------------|--------------------|------------------------|-------------|
| 12 | 0.7 | 6x680 | 13x100 | 90 | 320 | 64.21 | 14.72 | 0 - 35 | 364 |
| 12 | 0.7 | 5x680 | 9x100 | 90 | 550 | 62.6 | 9.43 | 0 - 35 | 615 |
| 5 | 0.7 | 6x680 | 13x100 | 90 | 320 | 61.62 | 17.57 | 0 - 35 | 364 |
| 5 | 0.7 | 5x680 | 9x100 | 90 | 550 | 57.08 | 9.99 | 0 - 35 | 615 |
| 12 | 0.8 | 6x680 | 11x100 | 90 | 280 | 70.61 | 16.3 | 0 - 35 | 364 |
| 12 | 0.8 | 4x680 | 10x100 | 90 | 400 | 74.14 | 11.43 | 0 - 35 | 615 |
| 5 | 0.8 | 6x680 | 11x100 | 90 | 280 | 66.84 | 19.56 | 0 - 35 | 364 |
| 5 | 0.8 | 4x680 | 10x100 | 90 | 400 | 69.59 | 11.19 | 0 - 35 | 615 |
| 12 | 0.9 | 6x680 | 7x100 | 90 | 280 | 74.3 | 11.13 | 0 - 35 | 364 |
| 12 | 0.9 | 4x680 | 10x100 | 90 | 400 | 75.18 | 10.45 | 0 - 35 | 615 |
| 5 | 0.9 | 6x680 | 7x100 | 90 | 240 | 73.32 | 17.57 | 0 - 35 | 364 |
| 5 | 0.9 | 4x680 | 10x100 | 90 | 400 | 71.58 | 12.45 | 0 - 35 | 615 |
| 12 | 1 | 5x680 | 9x100 | 90 | 240 | 83.46 | 13.52 | 0 - 35 | 364 |
| 12 | 1 | 3x680 | 12x100 | 90 | 360 | 97.73 | 10.45 | 0 - 35 | 615 |
| 5 | 1 | 5x680 | 9x100 | 90 | 240 | 77.09 | 18.37 | 0 - 35 | 364 |
| 5 | 1 | 3x680 | 12x100 | 90 | 360 | 93.11 | 10.45 | 0 - 35 | 615 |
| 12 | 1.2 | 4x470 | 10x100 | 90 | 220 | 105.75 | 11 | 0 - 35 | 421 |
| 12 | 1.2 | 3x470 | 10x100 | 90 | 360 | 97.3 | 8.46 | 0 - 35 | 727 |
| 5 | 1.2 | 4x470 | 10x100 | 90 | 220 | 107.39 | 17.99 | 0 - 35 | 421 |
| 5 | 1.2 | 3x470 | 10x100 | 90 | 360 | 93.39 | 9.25 | 0 - 35 | 727 |
| 12 | 1.5 | 3x470 | 9x100 | 90 | 200 | 129 | 9.93 | 0 - 35 | 471 |
| 12 | 1.5 | 2x470 | 8x100 | 100 | 280 | 141.29 | 10.41 | 0 - 35 | 727 |
| 5 | 1.5 | 3x470 | 9x100 | 90 | 200 | 129.66 | 20.38 | 0 - 35 | 471 |
| 5 | 1.5 | 2x470 | 8x100 | 100 | 280 | 137.26 | 20.78 | 0 - 35 | 727 |
| 12 | 1.8 | 2x470 | 12x100 | 100 | 180 | 148.86 | 13 | 0 - 35 | 471 |
| 12 | 1.8 | 1x470 | 11x100 | 100 | 240 | 167.2 | 10 | 0 - 35 | 727 |
| 5 | 1.8 | 2x470 | 12x100 | 100 | 180 | 130.41 | 24.37 | 0 - 35 | 471 |
| 5 | 1.8 | 1x470 | 11x100 | 100 | 240 | 163.79 | 19.98 | 0 - 35 | 727 |
| 12 | 2.5 | 2x470 | 6x100 | 90 | 140 | 191.78 | 11.13 | 0 - 35 | 533 |
| 5 | 2.5 | 2x470 | 6x100 | 90 | 140 | 181.48 | 37.9 | 0 - 35 | 533 |

Notes:

4. 1x470μF input bulk (EEE1EA471P) and 6x22μF input ceramic (GRM32ER71C226KE18L) capacitors are used for evaluating all test conditions above.
5. C_{IN} bulk capacitor is optional only for energy buffer from the long input power supply cable.
6. Output voltage response is tested with 0% - 50% load step and slew rate at 15A/μs.
7. ASCR gain and residual are selected to ensure a phase margin higher than 60° and a gain margin higher than 8dB at ambient room temperature.

Table 2. Recommended Input/Output Capacitor

| Vendors | Value | Part Number |
|------------------------|-------------------------|---------------------|
| Murata, Input Ceramic | 47 μ F, 16V, 1210 | GRM32ER61C476ME15L |
| Murata, Input Ceramic | 22 μ F, 25V, 1210 | GRM32ER61E226KE15L |
| Murata, Input Ceramic | 22 μ F, 16V, 1210 | GRM32ER71C226KE18L |
| Murata, Output Ceramic | 100 μ F, 6.3V, 1206 | GRM31CR60J107ME39L |
| TDK, Output Ceramic | 100 μ F, 6.3V, 1206 | C3216X5R0J107M160AB |
| Panasonic, Output Bulk | 680 μ F, 2.5V, 2917 | 2R5TPF680M6L |
| Panasonic, Output Bulk | 470 μ F, 4V, 2917 | 4TPE470MCL |
| Panasonic, Output Bulk | 470 μ F, 6.3V, 2917 | 6TPF470MAH |
| Panasonic, Input Bulk | 470 μ F, 25V | EEE1EA471P |

1.2 RAA210870 Internal Block Diagram

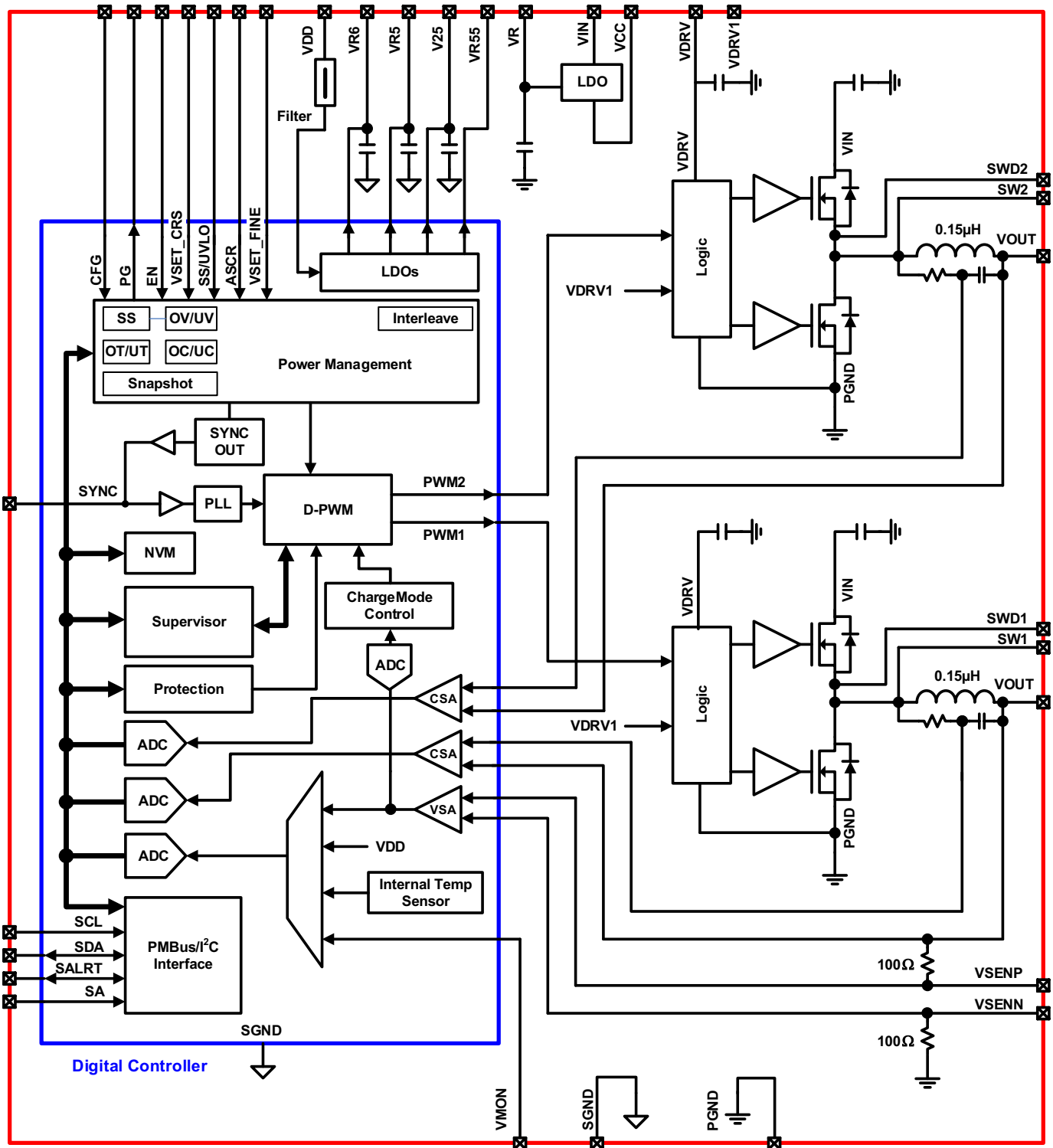


Figure 4. Internal Block Diagram

1.3 Ordering Information

| Part Number (Notes 9, 10) | Part Marking | Temp Range (°C) | Tape and Reel (Units) (Note 8) | Package (RoHS Compliant) | Pkg. Dwg. # |
|------------------------------|--------------------------------|-----------------|--------------------------------|--------------------------|-------------|
| RAA2108702GLG#AG0 | RAA2108702 | -40 to +85 | - | 58 Ld 18x23 HDA Module | Y58.18x23 |
| RAA2108702GLG#HG0 | RAA2108702 | -40 to +85 | 100 | 58 Ld 18x23 HDA Module | Y58.18x23 |
| RTKA2108702H00000BU | Single-Module Evaluation Board | | | | |

Notes:

8. Refer to [TB347](#) for details about reel specifications.
9. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
10. For Moisture Sensitivity Level (MSL), refer to the [RAA210870](#) device page. For more information about MSL, refer to [TB363](#).

Table 3. Key Differences between Family of Parts

| Part Number | Description | V _{IN} Range (V) | V _{OUT} Range (V) | I _{OUT} (A) |
|-------------|---|---------------------------|----------------------------|----------------------|
| RAA210833 | 33A DC/DC single channel power module | 4.5 - 14 | 0.6 - 5 | 33 |
| RAA210825 | 25A DC/DC single channel power module | 4.5 - 14 | 0.6 - 5 | 25 |
| RAA210850 | 50A DC/DC single channel power module | 4.5 - 14 | 0.6 - 5 | 50 |
| RAA210870 | 70A DC/DC single channel power module | 4.5 - 14 | 0.6 - 2.5 | 70 |
| RAA210925 | 25A/25A DC/DC dual channel power module | 4.5 - 14 | 0.6 - 5 | 25/25 |

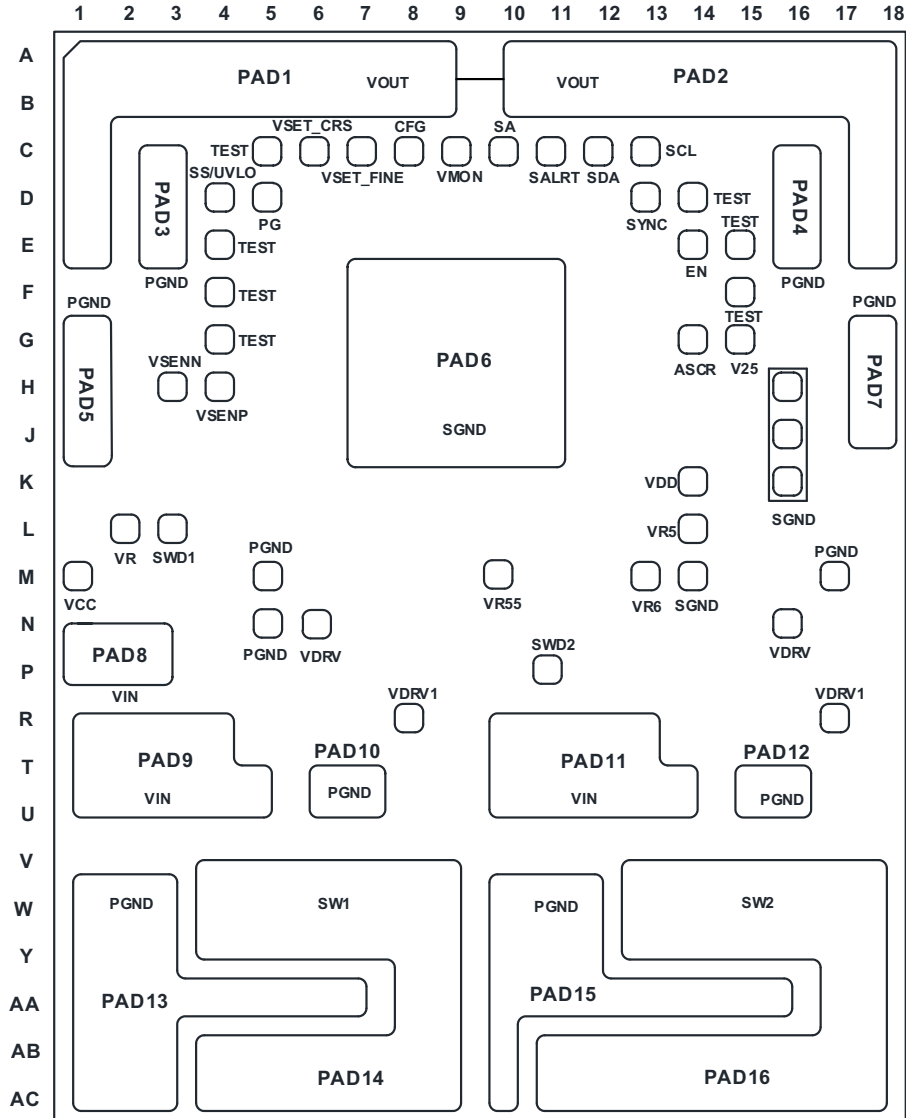
Table 4. Comparison of Simple Digital and Full Digital Parts

| | ISL8273M | RAA210870 |
|--|---|--|
| V _{IN} (V) | 4.5-14 | 4.5-14 |
| V _{OUT} (V) | 0.6-2.5 | 0.6-2.5 |
| I _{OUT} (Max) (A) | 80 | 70 |
| f _{SW} (kHz) | 296-1067 | 296-1067 |
| Digital PMBus Programmability for Configuration of Modules | All PMBus commands. NVM access to store module configuration. | Configuration of modules supported via pin-strap resistors. Digital programmability supports configuration changes during run-time operation with a subset of PMBus commands. No NVM access to store module configuration. |
| Power Navigator Support | Yes | Yes |
| SYNC Capability | Yes | Yes |
| Current Sharing Multi-Modules | Yes | No |
| DDC Pin (Inter-Device Communication) | Yes | No |

Note: For a full comparison of all the RAA210XXX and ISL827XM product offerings please visit the [simple-digital module family](#) page.

1.4 Pin Configuration

58 Ld HDA
Top View



1.5 Pin Descriptions

| Pin Number | Pin Name | Type | Description |
|--|-----------|------|--|
| PAD1, PAD2 | VOUT | PWR | Power supply output voltage. Output voltage ranges from 0.6V to 2.5V. Tie these two pads together to achieve a single output. For higher output voltage, refer to the derating curves starting on page 19 to set the maximum output current from these pads. |
| PAD3, PAD4, PAD5, PAD7, PAD10, PAD12, PAD13, PAD15 | PGND | PWR | Power ground. Refer to the " Layout Guide " on page 30 for the PGND pad connections and input/output capacitor placement. |
| PAD6 | SGND | PWR | Signal ground. Refer to " Layout Guide " for the SGND pad connections. |
| PAD8, PAD9, PAD11 | VIN | PWR | Input power supply voltage to power the module. Input voltage ranges from 4.5V to 14V. |
| PAD14 | SW1 | PWR | Switching node pads. The SW pads dissipate the heat and provide the good thermal performance. Refer to " Layout Guide " for the SW pad connections. |
| PAD16 | SW2 | | |
| C6 | VSET_CRS | I | Output voltage selection pin. Used to set V_{OUT} set point. Use VSET_FINE for fine tuning. |
| C7 | VSET_FINE | I | Output voltage fine tuning. Provides increased V_{OUT} resolution based on programmed VSET_CRS value. |
| C8 | CFG | I | Clock source configuration pin. If the clock source is set to internal, the internal frequency is set according to the SYNC pin resistor settings. If the clock source is set to external, the internal frequency is set according to the CFG pin resistor. See " Switching Frequency and PLL " on page 23 . |
| C9 | VMON | I | Driver voltage monitoring. Use this pin to monitor VDRV through an external 16:1 resistor divider. |
| C10 | SA | I | Serial address selection pin. Assigns a unique address for each individual device or enables certain management features. |
| C11 | SALRT | O | Serial alert. Connect to external host if desired. SALRT is asserted low upon a fault event and deasserted when the fault is cleared. A pull-up resistor is required. |
| C12 | SDA | I/O | Serial data. Connect to external host and/or to other Digital-DC™ devices. A pull-up resistor is required. |
| C13 | SCL | I/O | Serial clock. Connect to external host and/or to other Digital-DC devices. A pull-up resistor is required. |
| D4 | SS/ UVLO | I | Soft-start/stop and undervoltage lockout selection pin. Sets the turn on/off delay and ramp time in addition to the input UVLO threshold levels. |
| D5 | PG | O | Power-good output. The power-good is configured as an open-drain output. |
| D13 | SYNC | I/O | Clock synchronization input. Sets the frequency of the internal switch clock, syncs to an external clock, or outputs an internal clock. If external synchronization is used, the external clock must be active before enable. |
| E14 | EN | I | Enable pin. Set logic high to enable the module output. |
| C5, D14, E4, E15, F4, F15, G4 | TEST | - | Test pins. Do not connect these pins. |
| G14 | ASCR | I | ChargeMode control ASCR parameters selection pin. Sets the ASCR gain and residual values. |
| G15 | V25 | PWR | Internal 2.5V reference used to power internal circuitry. No external capacitor required for this pin. Not recommended to power external circuit. |
| H3 | VSENN | I | Differential output voltage sense feedback. Connect to a negative output regulation point. |
| H4 | VSENP | I | Differential output voltage sense feedback. Connect to a positive output regulation point. |
| H16, J16, K16, M14 | SGND | PWR | Signal grounds. Use multiple vias to connect the SGND pins to the internal SGND layer. |
| K14 | VDD | PWR | Input supply voltage for controller. Connect the VDD pad to the VIN supply. |

| Pin Number | Pin Name | Type | Description |
|-------------|----------|------|--|
| L2 | VR | PWR | Internal LDO bias pin. Tie VR to VR55 directly with a short loop trace. Do not use this pin to power the external circuit. |
| L3 | SWD1 | PWR | Switching node driving pins. Directly connect to the SW1 and SW2 pads with short loop wires. |
| P11 | SWD2 | | |
| L14 | VR5 | PWR | Internal 5V reference used to power internal circuitry. Place a 10 μ F decoupling capacitor for this pin. Maximum external loading current is 5mA. |
| M1 | VCC | PWR | Internal LDO output. Connect VCC to VDRV for internal LDO driving. |
| M5, M17, N5 | PGND | PWR | Power grounds. Use multiple vias to connect the PGND pins to the internal PGND layer. |
| M10 | VR55 | PWR | Internal 5.5V bias voltage for internal LDO use only. Tie VR55 pin directly to the VR pin. Not recommended to power external circuits. |
| M13 | VR6 | PWR | Internal 6V reference used to power internal circuitry. Place a 10 μ F decoupling capacitor for this pin. Not recommended to power external circuits. |
| N6, N16 | VDRV | PWR | Power supply for internal FET drivers. Connect a 10 μ F bypass capacitor to each of these pins. These pins can be driven by the internal LDO through VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input applications, use an external supply or connect this pin to VIN. |
| R8, R17 | VDRV1 | I | Bias pin of the internal FET drivers. Always tie to VDRV. |

2. Specifications

2.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|--------------|---------|-------------|
| Input Supply Voltage, VIN Pin | 0.3V | +17 | V |
| Input Supply Voltage for Controller, VDD Pin | -0.3 | +17 | V |
| MOSFET Switch Node Voltage, SW1/2, SWD1/2 | -0.3 | +17 | V |
| MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin | -0.3 | +6.0 | V |
| Output Voltage, VOUT pin | -0.3 | +6.0 | V |
| Internal Reference Supply Voltage, VR6 Pin | -0.3 | +6.6 | V |
| Internal Reference Supply Voltage, VR, VR5, VR55 Pin | -0.3 | +6.5 | V |
| Internal Reference Supply Voltage, V25 Pin | -0.3 | +3 | V |
| Logic I/O Voltage for EN, CFG, PG, ASCR, VSET_FINE, SA, SCL, SDA, SALRT, SYNC, SS/UVLO, VMON, VSET_CRIS | -0.3 | +6.0 | V |
| Analog Input Voltages | | | |
| VSENP | -0.3 | +6.0 | V |
| VSENN | -0.3 | +0.3 | V |
| ESD Rating | Value | | Unit |
| Human Body Model (Tested per JESD22-A114F) | 2 | | kV |
| Machine Model (Tested per JESD22-A115C) | 200 | | V |
| Charged Device Model (Tested per JESD22-C110D) | 750 | | V |
| Latch-up (Tested per JESD78C; Class 2, Level A) | 100 | | mA |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
|--|----------------------|----------------------|
| 58 Ld HDA Package (Notes 11, 12) | 5.3 | 1.1 |

Notes:

11. θ_{JA} is measured in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers and multiple via interconnects as specified in the RTKA2108702H00000BU evaluation board user guide.

12. For θ_{JC} , the "case temp" location is the center of the package underside.

| Parameter | Minimum | Maximum | Unit |
|--|--|---------|------|
| Maximum Junction Temperature (Plastic Package) | | +125 | °C |
| Storage Temperature Range | -55 | +150 | °C |
| Pb-Free Reflow Profile | See Figure 25 on page 32 | | |

2.3 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---------|---------|------|
| Input Supply Voltage Range, V_{IN} | 4.5 | 14 | V |
| Input Supply Voltage Range for Controller, V_{DD} | 4.5 | 14 | V |
| Output Voltage Range, V_{OUT} | 0.6 | 2.5 | V |
| Output Current Range, $I_{OUT(DC)}$ (Note 15) | 0 | 70 | A |
| Operating Junction Temperature Range, T_J | -40 | +125 | °C |

2.4 Electrical Specifications

$V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$.**

| Parameter | Symbol | Test Conditions | Min (Note 13) | Typ | Max (Note 13) | Unit |
|--|-----------------------|--|------------------|-------------|------------------|------|
| Input and Supply Characteristics | | | | | | |
| Input Supply Current for Controller | I_{DD} | $V_{IN} = V_{DD} = 12V$, $V_{OUT} = 0V$, module not enabled | | 40 | 50 | mA |
| 6V Internal Reference Supply Voltage | V_{R6} | | 5.5 | 6.1 | 6.6 | V |
| 5V Internal Reference Supply | V_{R5} | $I_{VR5} < 5mA$ | 4.5 | 5.2 | 5.5 | V |
| 2.5V Internal Reference Supply | V_{25} | | 2.25 | 2.5 | 2.75 | V |
| Internal LDO Output Voltage | V_{CC} | | | 5.3 | | V |
| Internal LDO Output Current | I_{VCC} | $V_{IN} = V_{DD} = 12V$, V_{CC} connected to VDRV, module enabled | 50 | | | mA |
| Input Supply Voltage for Controller Read Back Resolution | $V_{DD_READ_RES}$ | | | ± 20 | | mV |
| Input Supply Voltage for Controller Read Back Total Error (Note 16) | $V_{DD_READ_ERR}$ | PMBus Read | | ± 2 | | % FS |
| Output Characteristics | | | | | | |
| Output Voltage Adjustment Range | V_{OUT_RANGE} | $V_{IN} > V_{OUT} + 1.8V$ | 0.54 | | 2.75 | V |
| Output Voltage Set-Point Range | V_{OUT_RES} | Configured using PMBus | | ± 0.025 | | % |
| Output Voltage Set-Point Accuracy (Notes 14, 16) | V_{OUT_ACCY} | Includes line, load, and temperature ($-20^{\circ}C \leq T_A \leq +85^{\circ}C$) | -1.2 | | +1.2 | % FS |
| Output Voltage Read Back Resolution | $V_{OUT_READ_RES}$ | | | ± 0.15 | | % FS |
| Output Voltage Read Back Total Error (Note 16) | $V_{OUT_READ_ERR}$ | PMBus read | -2 | | +2 | % FS |
| Output Ripple Voltage | V_{OUT_RIPPLE} | $V_{OUT} = 1V$, $C_{OUT} = 6 \times 470\mu F$ POSCAP + $12 \times 100\mu F$ Ceramic | | 8 | | mV |
| Output Current Read Back Resolution | $I_{OUT_READ_RES}$ | | | 0.087 | | A |
| Output Current Range (Note 15) | I_{OUT_RANGE} | | | | 70 | A |
| Output Current Read Back Total Error | $I_{OUT_READ_ERR}$ | PMBus read at max load. $V_{OUT} = 1V$ | | ± 3 | | A |
| Soft-Start and Sequencing | | | | | | |
| Delay Time from Enable to V_{OUT} Rise | t_{ON_DELAY} | Configured using pin-strap resistors or PMBus | 2 | | 300 | ms |
| t_{ON_DELAY} Accuracy | $t_{ON_DELAY_ACCY}$ | | | ± 2 | | ms |

$V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$.** (Continued)

| Parameter | Symbol | Test Conditions | Min (Note 13) | Typ | Max (Note 13) | Unit |
|--|-------------------------|--|---------------------------------|---------------|----------------------------------|-----------------------|
| Output Voltage Ramp-Up Time | t_{ON_RISE} | Configured using pin-strap resistors or PMBus | 0.5 | | 120 | ms |
| Output Voltage Ramp-Up Time Accuracy | $t_{ON_RISE_ACCY}$ | | | ± 250 | | μs |
| Delay Time from Disable to V_{OUT} Fall | t_{OFF_DELAY} | Configured using pin-strap resistors or PMBus | 2 | | 300 | ms |
| t_{OFF_DELAY} Accuracy | $t_{OFF_DELAY_ACCY}$ | | | ± 2 | | ms |
| Output Voltage Fall Time | t_{OFF_FALL} | Configured using pin-strap resistors or PMBus | 0.5 | | 120 | ms |
| Output Voltage Fall Time Accuracy | $t_{ON_FALL_ACCY}$ | | | ± 250 | | μs |
| Power-Good | | | | | | |
| Power-Good Delay | V_{PG_DELAY} | Configured using PMBus | | 3 | | ms |
| Temperature Sense | | | | | | |
| Temperature Sense Range | T_{SENSE_RANGE} | Configurable using PMBus | -50 | | 150 | $^{\circ}C$ |
| Internal Temperature Sensor Accuracy | INT_TEMP_ACCY | Tested at $+100^{\circ}C$ | -5 | | +5 | $^{\circ}C$ |
| Fault Protection | | | | | | |
| V_{DD} Undervoltage Threshold Range | $V_{DD_UVLO_RANGE}$ | Measured internally | 4.18 | | 16 | V |
| V_{DD} Undervoltage Threshold Accuracy (Note 16) | $V_{DD_UVLO_ACCY}$ | | | ± 2 | | %FS |
| V_{DD} Undervoltage Response Time | $V_{DD_UVLO_DELAY}$ | | | 10 | | μs |
| V_{OUT} Overvoltage Threshold Range | $V_{OUT_OV_RANGE}$ | Factory default | | $1.15V_{OUT}$ | | V |
| | | Configured using PMBus | $1.05V_{OUT}$ | | V_{OUT_MAX} | V |
| V_{OUT} Undervoltage Threshold Range | $V_{OUT_UV_RANGE}$ | Factory default | | $0.85V_{OUT}$ | | V |
| | | Configured using PMBus | 0 | | $0.95V_{OUT}$ | V |
| V_{OUT} OV/UV Threshold Accuracy (Note 14) | V_{OUT_OV/UV_ACCY} | | -2 | | +2 | % |
| V_{OUT} OV/UV Response Time | V_{OUT_OV/UV_DELAY} | | | 10 | | μs |
| Output Current Limit Set-Point Accuracy (Note 16) | I_{LIMIT_ACCY} | Tested at $I_{OUT_OC_FAULT_LIMIT} = 80A$ | | ± 10 | | % FS |
| Output Current Fault Response Time | I_{LIMIT_DELAY} | Factory default | | 3 | | t_{sw} (Note 17) |
| Over-temperature Protection Threshold (Controller Junction Temperature) | $T_{JUNCTION}$ | Factory default | | 115 | | $^{\circ}C$ |
| | | Configured using PMBus | -40 | | 125 | $^{\circ}C$ |
| Thermal Protection Hysteresis | $T_{JUNCTION_HYS}$ | | | 15 | | $^{\circ}C$ |
| Oscillator and Switching Characteristics | | | | | | |
| Switching Frequency Range | f_{SW_RANGE} | | 296 | | 1067 | kHz |
| Switching Frequency Set-Point Accuracy | f_{SW_ACCY} | | -5 | | +5 | % |
| Minimum Pulse Width Required from External SYNC Clock | EXT_SYNC_{PW} | Measured at 50% Amplitude | 150 | | | ns |
| Drift Tolerance for External SYNC Clock | EXT_SYNC_{DRIFT} | External SYNC Clock equal to 500kHz is not supported | -10 | | +10 | % |

$V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$.** (Continued)

| Parameter | Symbol | Test Conditions | Min (Note 13) | Typ | Max (Note 13) | Unit |
|--|------------------------|--|------------------|-----|------------------|------|
| Logic Input/Output Characteristics | | | | | | |
| Bias Current at the Logic Input Pins | I_{LOGIC_BIAS} | EN, CFG, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, V_{MON} , VSET_CRS | -100 | | +100 | nA |
| Logic Input Low Threshold Voltage | $V_{LOGIC_IN_LOW}$ | | | | 0.8 | V |
| Logic Input High Threshold Voltage | $V_{LOGIC_IN_HIGH}$ | | 2.0 | | | V |
| Logic Output Low Threshold Voltage | $V_{LOGIC_OUT_LOW}$ | 2mA sinking | | | 0.5 | V |
| Logic Output High Threshold Voltage | $V_{LOGIC_OUT_HIGH}$ | 2mA sourcing | 2.25 | | | V |
| PMBus Interface Timing Characteristic | | | | | | |
| PMBus Operating Frequency | f_{SMB} | | 100 | | 400 | kHz |

Notes:

13. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design. Controller is independently tested before module assembly.
14. V_{OUT} measured at the termination of the VSENP and VSENN sense points.
15. The MAX load current is determined by the thermal ["Derating Curves" on page 19](#).
16. "FS" stands for full scale of recommended maximum operation range.
17. " t_{SW} " stands for time period of operation switching frequency.

3. Typical Performance Curves

3.1 Efficiency Performance

$T_A = +25^\circ\text{C}$, no air flow. $C_{OUT} = 6 \times 470\mu\text{F POSCAP} + 12 \times 100\mu\text{F Ceramic}$. Typical values are used unless otherwise noted.

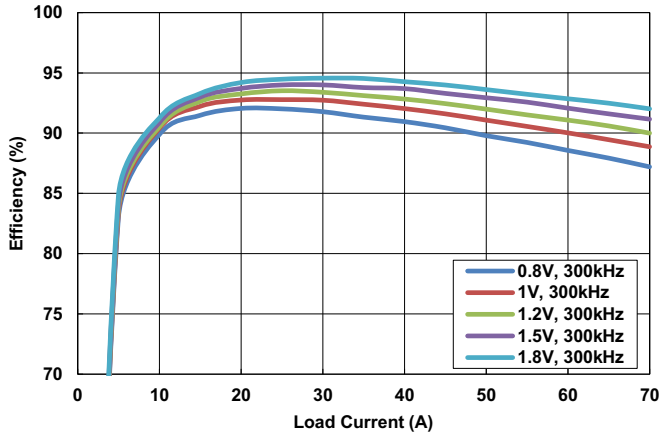


Figure 5. Efficiency vs Output Current at $V_{IN} = 5\text{V}$, $f_{SW} = 300\text{kHz}$ for Various Output Voltages

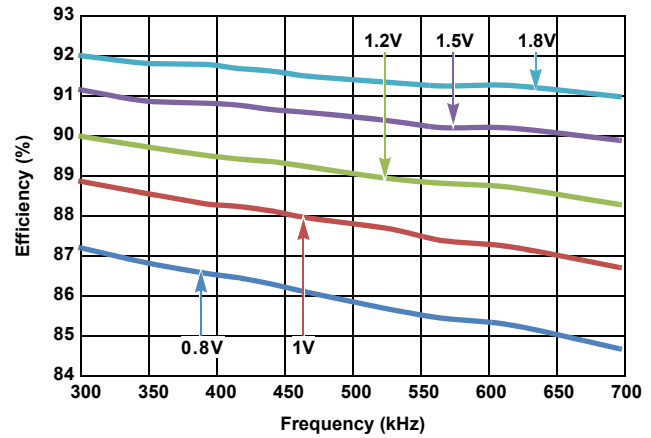


Figure 6. Efficiency vs Switching Frequency at $V_{IN} = 5\text{V}$, $I_{OUT} = 70\text{A}$ for Various Output Voltages

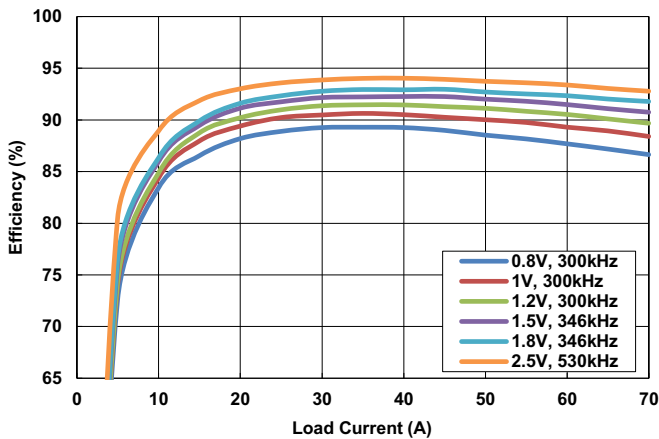


Figure 7. Efficiency vs Output Current at $V_{IN} = 9\text{V}$, for Various Output Voltages

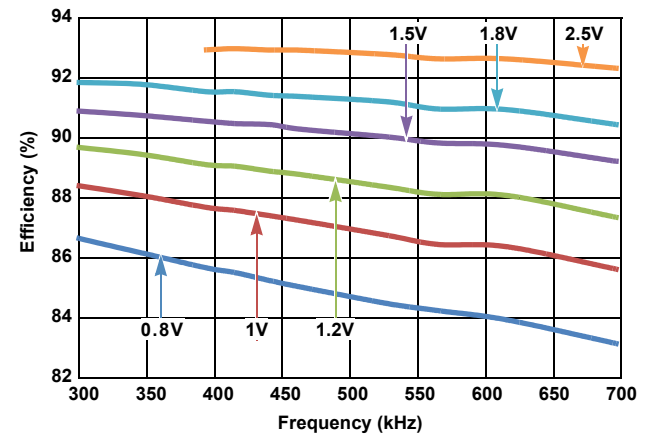


Figure 8. Efficiency vs Switching Frequency at $V_{IN} = 9\text{V}$, $I_{OUT} = 70\text{A}$ for Various Output Voltages

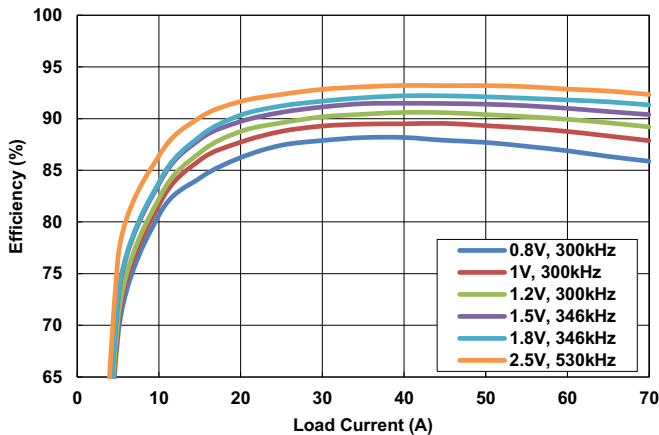


Figure 9. Efficiency vs Output Current at $V_{IN} = 12\text{V}$, for Various Output Voltages

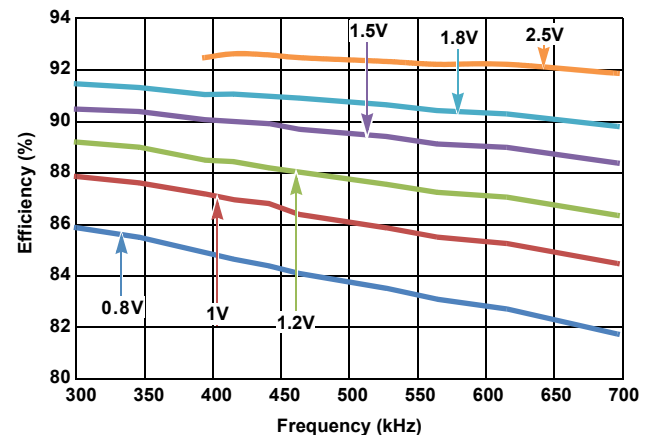


Figure 10. Efficiency vs Switching Frequency at $V_{IN} = 12\text{V}$, $I_{OUT} = 70\text{A}$ for Various Output Voltages

3.2 Transient Response Performance

Operating Conditions: $I_{OUT} = 0A/35A$, I_{OUT} slew rate = $15A/\mu s$, $T_A = +25^\circ C$, 0LFM. Typical values are used unless otherwise noted.

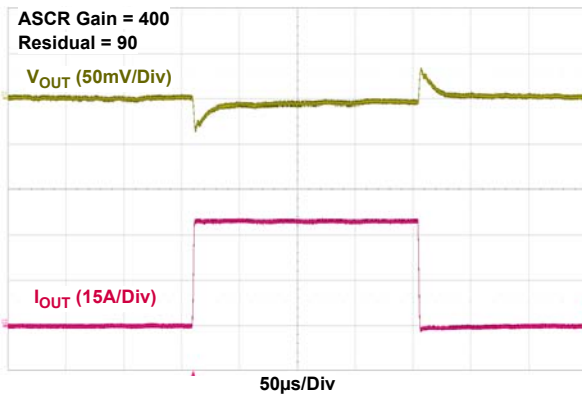


Figure 11. $5V_{IN}$ to $0.9V_{OUT}$ Transient Response, $f_{SW} = 615kHz$, $C_{OUT} = 10 \times 100\mu F$ Ceramic + $4 \times 680\mu F$ POSCAP

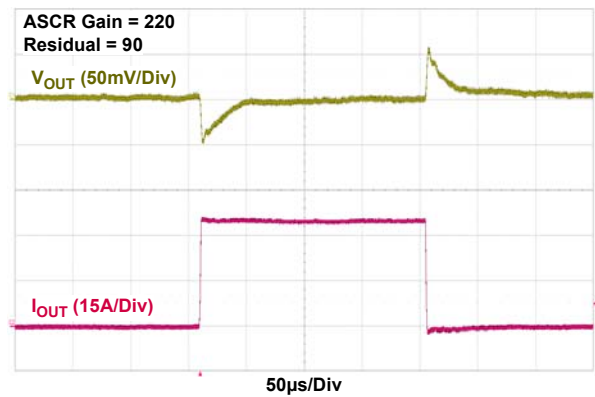


Figure 12. $5V_{IN}$ to $1.2V_{OUT}$ Transient Response, $f_{SW} = 421kHz$, $C_{OUT} = 10 \times 100\mu F$ Ceramic + $4 \times 470\mu F$ POSCAP

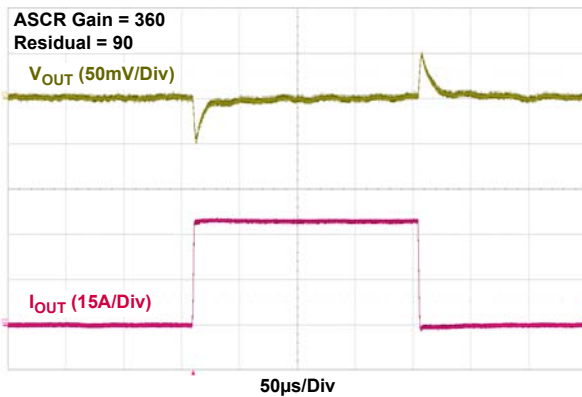


Figure 13. $12V_{IN}$ to $1V_{OUT}$ Transient Response, $f_{SW} = 615kHz$, $C_{OUT} = 12 \times 100\mu F$ Ceramic + $3 \times 680\mu F$ POSCAP

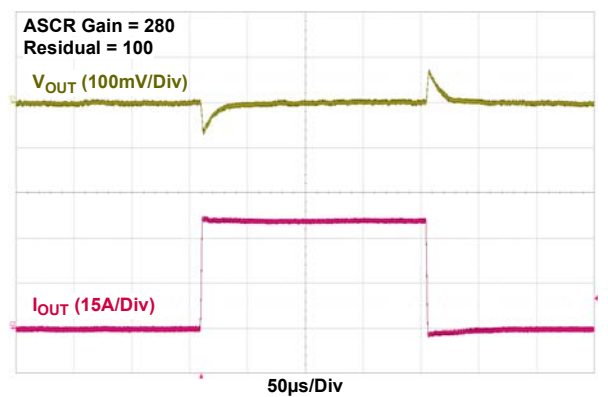


Figure 14. $12V_{IN}$ to $1.5V_{OUT}$ Transient Response, $f_{SW} = 727kHz$, $C_{OUT} = 8 \times 100\mu F$ Ceramic + $2 \times 470\mu F$ POSCAP

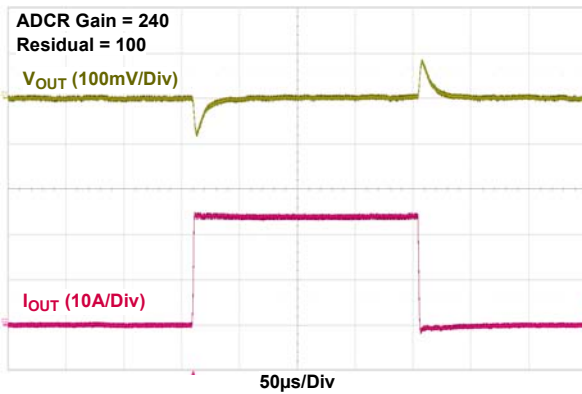


Figure 15. $12V_{IN}$ to $1.8V_{OUT}$ Transient Response, $f_{SW} = 727kHz$, $C_{OUT} = 11 \times 100\mu F$ Ceramic + $1 \times 470\mu F$ POSCAP

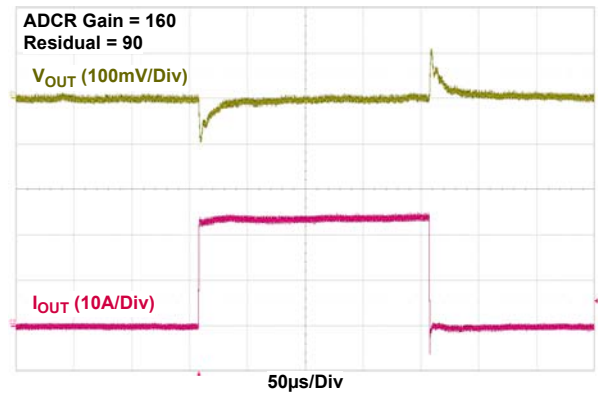


Figure 16. $12V_{IN}$ to $2.5V_{OUT}$ Transient Response, $f_{SW} = 533kHz$, $C_{OUT} = 6 \times 100\mu F$ Ceramic + $2 \times 470\mu F$ POSCAP

3.3 Derating Curves

All of the following curves were plotted at $T_J = +120^\circ\text{C}$.

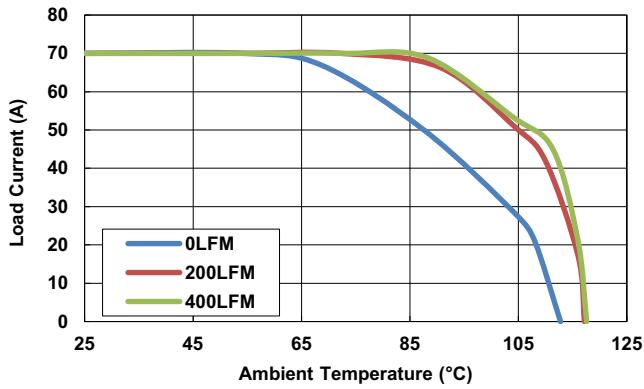


Figure 17. $5V_{IN}$ to $1V_{OUT}$, $f_{SW} = 300\text{kHz}$

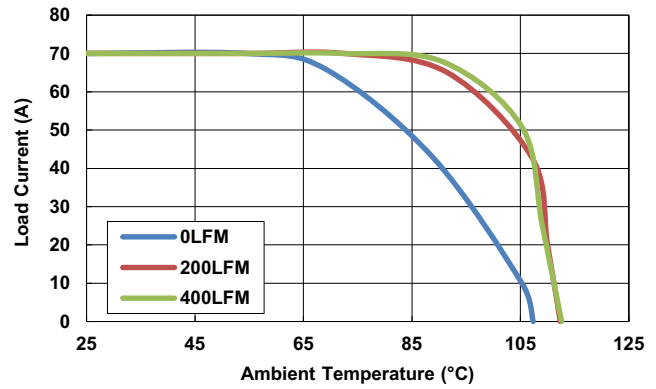


Figure 18. $12V_{IN}$ to $1V_{OUT}$, $f_{SW} = 300\text{kHz}$

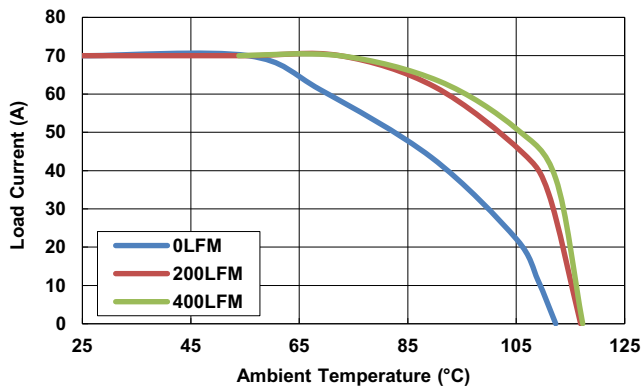


Figure 19. $5V_{IN}$ to $1.5V_{OUT}$, $f_{SW} = 300\text{kHz}$

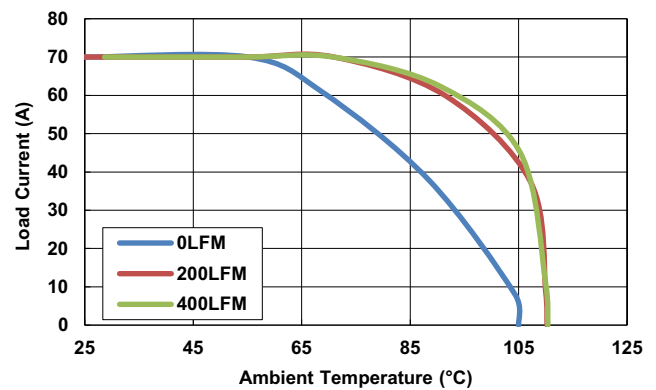


Figure 20. $12V_{IN}$ to $1.5V_{OUT}$, $f_{SW} = 364\text{kHz}$

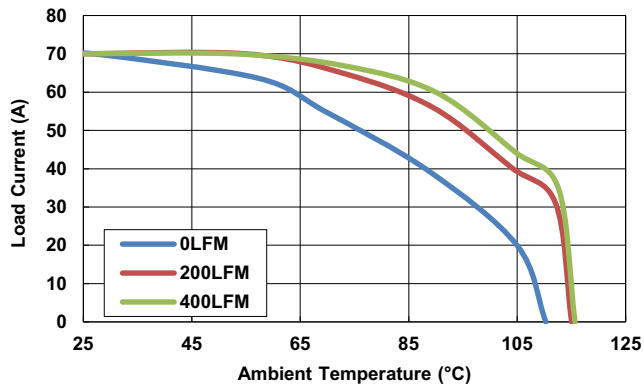


Figure 21. $5V_{IN}$ to $2.5V_{OUT}$, $f_{SW} = 364\text{kHz}$

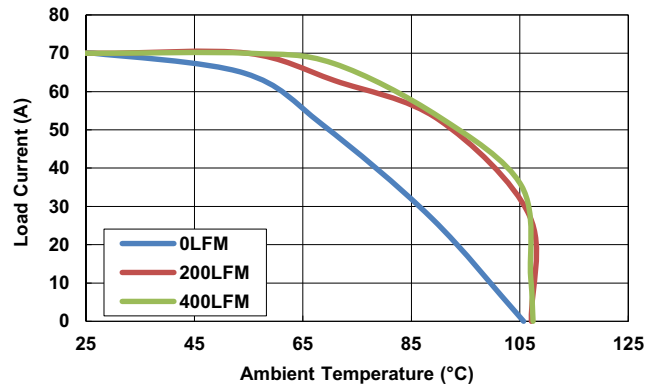


Figure 22. $12V_{IN}$ to $2.5V_{OUT}$, $f_{SW} = 533\text{kHz}$

4. Functional Description

4.1 SMBus Communications

The RAA210870 provides a SMBus digital interface that enables the user to configure the module in addition to monitor the input and output parameters. The RAA210870 can be used with any SMBus host device. The module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The RAA210870 accepts most standard PMBus commands. When PMBus commands are issued, it is recommended to tie the enable pin to SGND.

The SMBus device address is the only parameter that must be set by the external pins.

4.2 Output Voltage Selection

The output voltage can be set to a voltage between 0.6V and 2.5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET_CRG (VOOUT Coarse) and VSET_FINE (VOOUT Fine) pins are used to set the output voltage. A resistor placed between the VSET_CRG pin and SGND is used to program the VOOUT_CRG (VOOUT Coarse) voltage according to resistor settings in [Table 5](#). A standard 1% resistor is required.

If higher resolution is desired, then VSET_FINE pin can be used to fine tune the output voltage settings according to the following command set:

$$\text{VOOUT_COMMAND} = \begin{cases} \text{VOOUT_CRG} + 5\text{mV} \cdot \text{N}, & \text{if } 0.6\text{V} \leq \text{VOOUT_CRG} \leq 1.4\text{V} \\ \text{VOOUT_CRG} + 10\text{mV} \cdot \text{N}, & \text{if } 1.5\text{V} \leq \text{VOOUT_CRG} \leq 2.4\text{V} \\ \text{VOOUT_CRG}, & \text{if } \text{VOOUT_CRG} = 2.5\text{V} \end{cases}$$

Use the resistor values from [Table 6 on page 21](#) to set the appropriate value of N for calculating the final output voltage.

Table 5. VSET_COARSE Resistor Settings

| VOOUT_CRG (V) | R _{SET} (kΩ) |
|---------------|--------------------------|
| 0.600 | 10 |
| 0.675 | 11 |
| 0.700 | 12.1 |
| 0.720 | 13.3 |
| 0.750 | 14.7 |
| 0.800 | 16.2 |
| 0.850 | 17.8 |
| 0.900 | 19.6 |
| 0.930 | 21.5 |
| 0.950 | 23.7 |
| 0.980 | 26.1 |
| 1.000 | 28.7, or connect to SGND |
| 1.030 | 31.6 |
| 1.050 | 34.8 |
| 1.100 | 38.3 |
| 1.120 | 42.2 |
| 1.150 | 46.4 |
| 1.200 | 51.1, or OPEN |
| 1.250 | 56.2 |

Table 5. VSET_COARSE Resistor Settings (Continued)

| VOUT_CRS (V) | R _{SET} (kΩ) |
|--------------|------------------------|
| 1.300 | 61.9 |
| 1.350 | 68.1 |
| 1.400 | 75 |
| 1.500 | 82.5 |
| 1.650 | 90.9 |
| 1.800 | 100 |
| 1.850 | 110 |
| 2.000 | 121 |
| 2.200 | 133 |
| 2.400 | 147 |
| 2.500 | 162, or Connect to V25 |

Table 6. VSET_FINE Resistor Settings

| N | R _{SET} (kΩ) |
|----|--------------------------|
| 0 | 10, or OPEN |
| 1 | 11 |
| 2 | 12.1 |
| 3 | 13.3 |
| 4 | 14.7 |
| 5 | 16.2 |
| 6 | 17.8 |
| 7 | 19.6 |
| 8 | 21.5 |
| 9 | 23.7, or Connect to SGND |
| 10 | 26.1 |
| 11 | 28.7 |
| 12 | 31.6 |
| 13 | 34.8 |
| 14 | 38.3 |
| 15 | 42.2 |
| 16 | 46.4 |
| 17 | 51.1 |
| 18 | 56.2 |
| 19 | 61.9 |
| 20 | 68.1, or Connect to V25 |

The output voltage can be set to any value between 0.6V and 2.5V using the pin-strap settings provided in [Tables 5](#) and [6](#).

By default, V_{OUT_MAX} is set to 110% of V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 2.75V by the PMBus command VOUT_MAX.

4.3 Soft-Start, Stop Delay, and Ramp Times

The RAA210870 follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. When this process is complete, the device is ready to accept commands from the PMBus interface and the module is ready to be enabled. If the module is synchronizing to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The RAA210870 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp-up time can be programmed to custom values using the PMBus commands TON_DELAY and TON_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. In general, set the soft-start ramp to a value greater than 1ms to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay and ramp down time for soft-stop/off can be programmed using the PMBus commands TOFF_DELAY and TOFF_FALL. In addition, the module can be configured as “immediate off” using the command ON_OFF_CONFIG, so that the internal MOSFETs are turned off immediately after the delay time expires.

The SS/UVLO pin can be used to program the soft-start/stop delay time and ramp time to some typical values as shown in [Table 7](#).

Table 7. UVLO and Soft-Start/Stop Resistor Settings

| Resistor (k Ω) | UVLO (V) | Delay Time (ms) | Ramp Time (ms) |
|------------------------|----------|-----------------|----------------|
| 10 | 4.5 | 5 | 2 |
| 11 | 4.5 | 5 | 2 |
| 12.1 | 4.5 | 5 | 2 |
| 13.3 | 4.5 | 5 | 2 |
| 14.7 | 4.5 | 5 | 2 |
| 16.2 | 4.5 | 5 | 2 |
| 17.8 | 4.5 | 5 | 2 |
| 19.6 | 4.5 | 5 | 2 |
| 21.5 | 4.5 | 10 | 2 |
| 23.7 | 4.5 | 5 | 5 |
| 26.1 | 4.5 | 10 | 5 |
| 28.7 | 4.5 | 20 | 5 |
| 31.6 | 4.5 | 5 | 10 |
| 34.8 | 4.5 | 10 | 10 |
| 38.3 | 4.5 | 20 | 10 |
| 42.2 | 10.8 | 5 | 2 |
| 46.4 | 10.8 | 10 | 2 |
| 51.1 | 10.8 | 5 | 5 |
| 56.2 | 10.8 | 10 | 5 |
| 61.9 | 10.8 | 20 | 5 |

Table 7. UVLO and Soft-Start/Stop Resistor Settings (Continued)

| Resistor (k Ω) | UVLO (V) | Delay Time (ms) | Ramp Time (ms) |
|------------------------|----------|-----------------|----------------|
| 68.1 | 10.8 | 5 | 10 |
| 75 | 10.8 | 10 | 10 |
| 82.5 | 10.8 | 20 | 10 |
| Connect to SGND | 4.5 | 5 | 2 |
| OPEN | 4.2 | 5 | 5 |
| Connect to V25 | 4.5 | 10 | 10 |

4.4 Input Undervoltage Lockout (UVLO)

The input Undervoltage Lockout (UVLO) prevents the RAA210870 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V by using the PMBus command `VIN_UV_FAULT_LIMIT`. Use the pin-strap method (SS/UVLO pin) as shown in [Table 7](#) to set the V_{UVLO} to three typical values.

When the module falls below the UVLO threshold, it shuts down immediately. The fault needs to be cleared before the module can restart.

4.5 Power-Good

The RAA210870 provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit can be changed using the PMBus command `POWER_GOOD_ON`.

A PG delay period is defined as the time from when all conditions within the RAA210870 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A fixed PG delay of 3ms is programmed for the RAA210870.

4.6 Switching Frequency and PLL

The device's switching frequency is configurable from 296kHz to 1067kHz using the pin-strap method as shown in [Table 9](#), or by using the PMBus command `FREQUENCY_SWITCH`.

Table 8. Switching Frequency Resistor Settings

| f_{sw} (kHz) | R_{SET} (k Ω) |
|----------------|--------------------------|
| 296 | 14.7, or connect to SGND |
| 300 | 16.2 |
| 320 | 17.8 |
| 364 | 19.6 |
| 400 | 21.5 |
| 421 | 23.7, or OPEN |
| 471 | 26.1 |
| 533 | 28.7 |
| 571 | 31.6 |
| 615 | 34.8, or connect to V25 |
| 727 | 38.3 |
| 800 | 42.2 |
| 842 | 46.4 |
| 889 | 51.1 |
| 1067 | 56.2 |

The RAA210870 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can also be driven by an external clock source connected to the SYNC pin. This configuration can be achieved by connecting a resistor to the CFG pin. If the clock source is set to be internal, the internal frequency is set according to the SYNC pin resistor settings as shown in [Table 8 on page 23](#). If clock source is programmed to be external, then the internal frequency is set according to the resistor connected to the CFG pin as shown in [Table 9](#). The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns. The external clock frequency should be within $\pm 10\%$ of the listed options shown in [Table 9](#).

Table 9. External Frequency Sync Settings

| Clock Source | Internal FREQUENCY_SWITCH (kHz) | R _{SET} (k Ω) |
|--------------|---------------------------------|--------------------------------|
| Internal | Determined by SYNC resistor | 10, or OPEN |
| External | 296 | 11 |
| External | 340 | 12.1 |
| External | 390 | 13.3 |
| External | 444 | 14.7 |
| External | 516 | 16.2, or connect to SGND |
| External | 593 | 17.8 |
| External | 696 | 19.6 |
| External | 800 | 21.5 |
| External | 941 | 23.7 |
| External | 1067 | 26.1, or Connect to V25 |

4.7 Loop Compensation

The module loop response is programmable using the pin-strap method or by using the PMBus command ASCR_CONFIG according to [Table 10](#). The RAA210870 uses the ChargeMode control algorithm that responds to the output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

Table 10. ASCR Resistor Settings

| ASCR Gain | ASCR Residual | R _{SET} (k Ω) |
|-----------|---------------|--------------------------------|
| 100 | 90 | 10 |
| 110 | 90 | 11 |
| 120 | 90 | Connect to SGND |
| 140 | 90 | 12.1 |
| 160 | 90 | 13.3 |
| 180 | 90 | 14.7 |
| 200 | 90 | OPEN |
| 220 | 90 | 16.2 |
| 240 | 90 | 17.8 |
| 280 | 90 | 19.6 |
| 320 | 90 | 21.5 |
| 360 | 90 | 23.7 |
| 400 | 90 | 26.1 |
| 450 | 90 | 28.7 |
| 500 | 90 | 31.6 |
| 550 | 90 | 34.8 |

Table 10. ASCR Resistor Settings (Continued)

| ASCR Gain | ASCR Residual | R _{SET} (kΩ) |
|-----------|---------------|-----------------------|
| 600 | 90 | 38.3 |
| 700 | 90 | 42.2 |
| 800 | 90 | 46.4 |
| 80 | 100 | 51.1 |
| 120 | 100 | 56.2 |
| 160 | 100 | 61.9 |
| 200 | 100 | 68.1 |
| 240 | 100 | 75 |
| 280 | 100 | 82.5 |
| 320 | 100 | 90.9 |
| 360 | 100 | 100 |
| 400 | 100 | 110 |
| 450 | 100 | 121 |
| 500 | 100 | Connect to V25 |
| 550 | 100 | 133 |
| 600 | 100 | 147 |
| 700 | 100 | 162 |
| 800 | 100 | 178 |

4.8 SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between pins SA and SGND. [Table 11](#) lists the available module addresses.

Table 11. SMBus Address Resistor Selection

| R _{SA} (kΩ) | SMBus Address |
|--------------------------|---------------|
| 10 | 19h |
| 11 | 1Ah |
| 12.1 | 1Bh |
| 13.3 | 1Ch |
| 14.7 | 1Dh |
| 16.2 | 1Eh |
| 17.8 | 1Fh |
| 19.6 | 20h |
| 21.5 | 21h |
| 23.7 | 22h |
| 26.1 | 23h |
| 28.7 | 24h |
| 31.6 | 25h |
| 34.8, or connect to SGND | 26h |
| 38.3 | 27h |
| 42.2, or Open | 28h |
| 46.4 | 29h |

Table 11. SMBus Address Resistor Selection (Continued)

| R_{SA} (k Ω) | SMBus Address |
|------------------------|---------------|
| 51.1 | 2Ah |
| 56.2 | 2Bh |
| 61.9 | 2Ch |
| 68.1 | 2Dh |
| 75 | 2Eh |
| 82.5 | 2Fh |
| 90.9 | 30h |
| 100 | 31h |
| 110 | 32h |
| 121 | 33h |
| 133 | 34h |
| 147 | 35h |
| 162 | 36h |
| 178 | 37h |

4.9 Output Overvoltage Protection

The RAA210870 has an internal output overvoltage protection circuit that can protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at pins VSENP, VSENN) to a threshold set to 15% higher than the target output voltage. The fault threshold can be programmed to a desired level by the PMBus command VOUT_OV_FAULT_LIMIT. If the VSENP - VSENN voltage exceeds this threshold, the module initiates an immediate shutdown without retry.

Internal to the module, two 100 Ω resistors are populated from V_{OUT} to VSENP and SGND to VSENN to protect the module from overvoltage conditions in case of open at the voltage sensing pins and differential remote sense traces due to assembly error. As long as differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not compromised.

4.10 Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The RAA210870 provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage. However, the total time elapsed from when the delay period expires to when the output reaches its target value matches the preconfigured ramp time (see [Figure 23](#)).

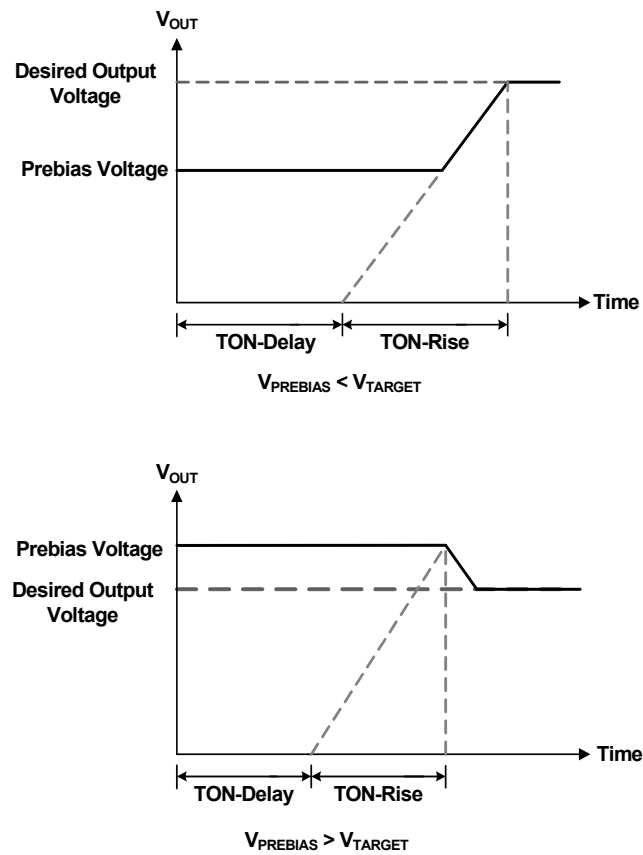


Figure 23. Output Responses to Prebias Voltages

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, so both drivers are enabled with a PWM duty cycle that ideally creates the prebias voltage.

When the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition.

4.11 Output Overcurrent Protection

The RAA210870 is protected from damage if the output is shorted to ground or if an overload condition is imposed on the output. The average output overcurrent fault threshold can be programmed by the PMBus command IOUT_OC_FAULT_LIMIT. The module automatically programs the peak inductor current fault threshold by calculating inductor ripple current based on input voltage, switching frequency, and VOUT_COMMAND.

The response from an overcurrent fault is an immediate shutdown with 70ms retry.

4.12 Thermal Overload Protection

The RAA210870 includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The factory default temperature limit is set to +115°C. The temperature limit can be changed using the PMBus command OT_FAULT_LIMIT.

The response from an over-temperature fault is an immediate shutdown without retry.

4.13 Phase Spreading

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device, so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset between devices is determined from the lower four bits of the SMBus address of each interleaved device. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments. The internal two phases of the module always maintain a phase difference of 180° .

This functionality can also be accessed using the PMBus command INTERLEAVE.

Table 12. Interleave

| SA | SA in Binary | Low 4-Bits | Interleave | Phase Shift in Degrees | Rail ID |
|-----|--------------|------------|------------|------------------------|---------|
| 19h | 00011001 | 1001 | 9 | 202.5 | 25 |
| 1Ah | 00011010 | 1010 | 10 | 225 | 26 |
| 1Bh | 00011011 | 1011 | 11 | 247.5 | 27 |
| 1Ch | 00011100 | 1100 | 12 | 270 | 28 |
| 1Dh | 00011101 | 1101 | 13 | 292.5 | 29 |
| 1Eh | 00011110 | 1110 | 14 | 315 | 30 |
| 1Fh | 00011111 | 1111 | 15 | 337.5 | 31 |
| 20h | 00100000 | 0000 | 0 | 0 | 0 |
| 21h | 00100001 | 0001 | 1 | 22.5 | 1 |
| 22h | 00100010 | 0010 | 2 | 45 | 2 |
| 23h | 00100011 | 0011 | 3 | 67.5 | 3 |
| 24h | 00100100 | 0100 | 4 | 90 | 4 |
| 25h | 00100101 | 0101 | 5 | 112.5 | 5 |
| 26h | 00100110 | 0110 | 6 | 135 | 6 |
| 27h | 00100111 | 0111 | 7 | 157.5 | 7 |
| 28h | 00101000 | 1000 | 8 | 180 | 8 |
| 29h | 00101001 | 1001 | 9 | 202.5 | 9 |
| 2Ah | 00101010 | 1010 | 10 | 225 | 10 |
| 2Bh | 00101011 | 1011 | 11 | 247.5 | 11 |
| 2Ch | 00101100 | 1100 | 12 | 270 | 12 |
| 2Dh | 00101101 | 1101 | 13 | 292.5 | 13 |
| 2Eh | 00101110 | 1110 | 14 | 315 | 14 |
| 2Fh | 00101111 | 1111 | 15 | 337.5 | 15 |
| 30h | 00110000 | 0000 | 0 | 0 | 16 |
| 31h | 00110001 | 0001 | 1 | 22.5 | 17 |
| 32h | 00110010 | 0010 | 2 | 45 | 18 |
| 33h | 00110011 | 0011 | 3 | 67.5 | 19 |
| 34h | 00110100 | 0100 | 4 | 90 | 20 |
| 35h | 00110101 | 0101 | 5 | 112.5 | 21 |
| 36h | 00110110 | 0110 | 6 | 135 | 22 |
| 37h | 00110111 | 0111 | 7 | 157.5 | 23 |

4.14 Monitoring with SMBus

The RAA210870 can monitor a wide variety of different system parameters using the following PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQUENCY
- READ_VMON

4.15 Snapshot Parameter Capture

The RAA210870 offers a special feature to capture parametric data and fault status following a fault event. A detailed description is provided in the [“SNAPSHOT \(EAh\)”](#) and [“SNAPSHOT_CONTROL \(F3h\)”](#) sections of [“PMBus Commands Description”](#) on page 36.

5. Layout Guide

To achieve stable operation, low losses and good thermal performance some layout considerations are necessary. See [Figure 24](#) for the recommended layout.

- Establish separate SGND and PGND planes, then connect SGND to PGND on a middle layer and underneath PAD6 with a single point connection. For SGND and PGND pin connections, such as small pins H16, J16, M5, and M17..., use multiple vias for each pin to connect to the inner SGND or PGND layer.
- To minimize high frequency noise, place enough ceramic capacitors between VIN and PGND and VOUT and PGND. Place bypass capacitors between VDD, VDRV, and the ground plane, as close to the module as possible. It is critical to place the output ceramic capacitors close to the VOUT pads and in the direction of the load current path to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for the power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. It is recommended to enlarge PAD11 and 15 and place more vias on them. The ceramic capacitors CIN can be placed on the bottom layer under these two pads.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation and place the two traces in parallel. Route a trace from VSENN and VSENP to the point of load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN, VSENP sensing lines near the SW pins.
- PAD14 and 16 (SW1 and SW2) are noisy pads, but they are beneficial for thermal dissipation. If the noise issue is critical for the application, it is recommended to use only the top layer for the SW pads. For better thermal performance, use multiple vias on these pads to connect into the SW inner and bottom layers. However, caution must be taken when placing a limited area of SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid the noise coupling.
- For pins SWD1 (L3) and SWD2 (P10), it is recommended to connect to the related SW1 and SW2 pads with short loop wires. The wire width should be more than 20 mils.

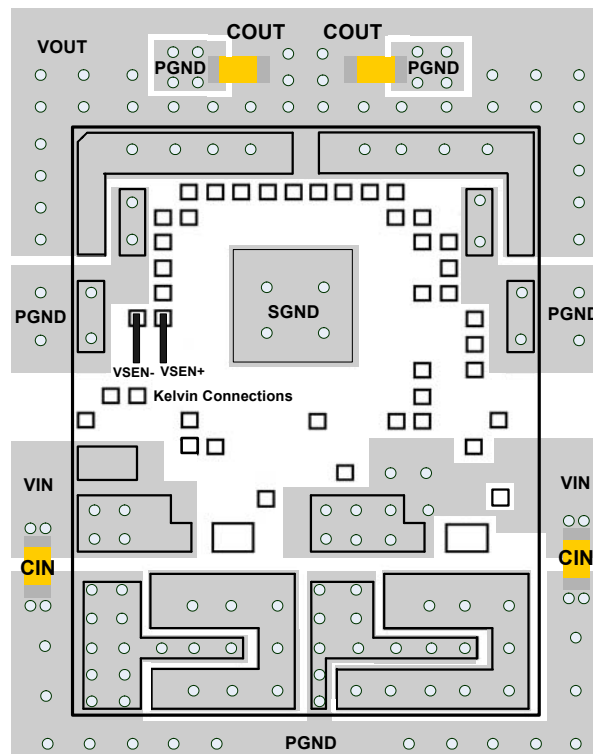


Figure 24. Recommended Layout

5.1 Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In the actual application, consider other heat sources and design margins.

5.2 Package Description

The RAA210870 uses the High Density Array no-lead package (HDA). This kind of package has advantages such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The RAA210870 contains several types of devices, including resistors, capacitors, inductors, and control ICs. The RAA210870 is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline and typical Printed Circuit Board (PCB) layout pattern design and typical stencil pattern design are shown on [pages 51](#) through [57](#). The module has a small size of 18mm x 23mm x 7.5mm.

5.3 PCB Layout Pattern Design

The bottom of the RAA210870 is a leadframe footprint, which is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on [pages 56](#) through [57](#). The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

5.4 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, diminishing returns are seen as the number of vias is increased. Use as many vias as practical for the thermal land size and your board design rules allow.

5.5 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. Stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the [“Package Outline Drawing”](#) section starting on [page 53](#). Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

5.6 Reflow Parameters

Due to the low mount height of the HDA, “No-Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in [Figure 25](#) is provided as a guideline, which can be customized for varying manufacturing practices and applications.

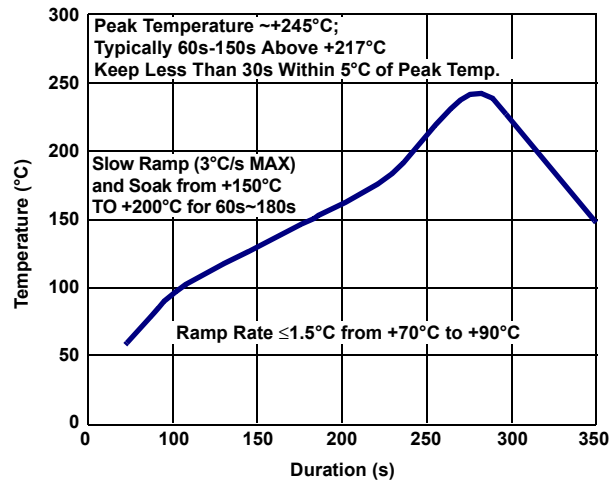


Figure 25. Typical Reflow Profile

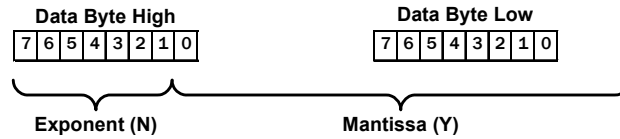
6. PMBus Command Summary

| Command Code | Command Name | Description | Type | Data Format | Default Value | Default Setting | Pg# |
|--------------|---------------------|--|-----------|-------------|---------------|--|--------------------|
| 01h | OPERATION | Sets enable and disable settings. | R/W Byte | BIT | | | 36 |
| 02h | ON_OFF_CONFIG | Configures the EN pin and PMBus commands to turn the unit ON/OFF | R/W Byte | BIT | 16h | Hardware enable, soft off | 36 |
| 03h | CLEAR_FAULTS | Clears fault indications. | Send Byte | | | | 36 |
| 21h | VOUT_COMMAND | Sets the nominal value of the output voltage. | R/W Word | L16u | | V _{OUT} Pin-strap (set based on VSET_CRS and VSET_FINE) | 37 |
| 24h | VOUT_MAX | Sets the maximum possible value of V _{OUT} . 110% of pin-strap V _{OUT} . | R/W Word | L16u | | 1.1*V _{OUT} Pin-strap | 37 |
| 33h | FREQUENCY_SWITCH | Sets the switching frequency. | R/W Word | L11 | | Pin-strap | 37 |
| 37h | INTERLEAVE | Configures a phase offset between devices sharing a SYNC clock. | R/W Word | BIT | 0000h | Pin-strap (set based on SMBus address) | 38 |
| 40h | VOUT_OV_FAULT_LIMIT | Sets the V _{OUT} overvoltage fault threshold. | R/W Word | L16u | | 1.15*V _{OUT} Pin-strap | 38 |
| 44h | VOUT_UV_FAULT_LIMIT | Sets the V _{OUT} undervoltage fault threshold. | R/W Word | L16u | | 0.85*V _{OUT} Pin-strap | 38 |
| 46h | IOUT_OC_FAULT_LIMIT | Sets the I _{OUT} average overcurrent fault threshold. | R/W Word | L11 | EAD0h | 90A | 38 |
| 4Bh | IOUT_UC_FAULT_LIMIT | Sets the I _{OUT} average undercurrent fault threshold. | R/W Word | L11 | E4E0h | -50A | 39 |
| 4Fh | OT_FAULT_LIMIT | Sets the over-temperature fault threshold. | R/W Word | L11 | EB98h | +115°C | 39 |
| 53h | UT_FAULT_LIMIT | Sets the under-temperature fault threshold. | R/W Word | L11 | E530h | -45°C | 39 |
| 55h | VIN_OV_FAULT_LIMIT | Sets the V _{IN} overvoltage fault threshold. | R/W Word | L11 | D3A0h | 14.5V | 39 |
| 59h | VIN_UV_FAULT_LIMIT | Sets the V _{IN} undervoltage fault threshold. | R/W Word | L11 | | Pin-strap | 40 |
| 5Eh | POWER_GOOD_ON | Sets the voltage threshold for Power-good indication. | R/W Word | L16u | | 0.9*V _{OUT} Pin-strap | 40 |
| 60h | TON_DELAY | Sets the delay time from ENABLE to start of V _{OUT} rise. | R/W Word | L11 | | Pin-strap | 40 |
| 61h | TON_RISE | Sets the rise time of V _{OUT} after ENABLE and TON_DELAY. | R/W Word | L11 | | Pin-strap | 40 |
| 64h | TOFF_DELAY | Sets the delay time from DISABLE to start of V _{OUT} fall. | R/W Word | L11 | | Pin-strap | 41 |
| 65h | TOFF_FALL | Sets the fall time for V _{OUT} after DISABLE and TOFF_DELAY. | R/W Word | L11 | | Pin-strap | 41 |
| 78h | STATUS_BYTE | Returns an abbreviated status for fast reads. | Read Byte | BIT | 00h | No faults | 41 |
| 79h | STATUS_WORD | Returns information with a summary of the unit's fault condition. | Read Word | BIT | 0000h | No faults | 42 |
| 7Ah | STATUS_VOUT | Returns the V _{OUT} specific status. | Read Byte | BIT | 00h | No faults | 42 |
| 7Bh | STATUS_IOUT | Returns the I _{OUT} specific status. | Read Byte | BIT | 00h | No faults | 43 |

| Command Code | Command Name | Description | Type | Data Format | Default Value | Default Setting | Pg# |
|--------------|----------------------------|---|------------|-------------|---------------|-----------------------------------|--------------------|
| 7Ch | STATUS_INPUT | Returns specific status specific to the input. | Read Byte | BIT | 00h | No faults | 43 |
| 7Dh | STATUS_TEMP | Returns the temperature specific status. | Read Byte | BIT | 00h | No faults | 43 |
| 7Eh | STATUS_CML | Returns the communication, logic, and memory specific status. | Read Byte | BIT | 00h | No faults | 44 |
| 80h | STATUS_MFR_SPECIFIC | Returns the VMON and external sync clock specific status. | Read Byte | BIT | 00h | No faults | 44 |
| 88h | READ_VIN | Returns the input voltage reading. | Read Word | L11 | | | 44 |
| 8Bh | READ_VOUT | Returns the output voltage reading. | Read Word | L16u | | | 45 |
| 8Ch | READ_IOUT | Returns the output current reading. | Read Word | L11 | | | 45 |
| 8Dh | READ_INTERNAL_TEMP | Returns the temperature reading internal to the device. | Read Word | L11 | | | 45 |
| 94h | READ_DUTY_CYCLE | Returns the duty cycle reading during the ENABLE state. | Read Word | L11 | | | 45 |
| 95h | READ_FREQUENCY | Returns the measured operating switch frequency. | Read Word | L11 | | | 45 |
| 96h | READ_IOUT_0 | Returns the phase 1 current reading. | Read Word | L11 | | | 46 |
| 97h | READ_IOUT_1 | Returns the phase 2 current reading. | Read Word | L11 | | | 46 |
| DFh | ASCR_CONFIG | Configures ASCR control loop. | R/W Block | CUS | | Pin-strap | 46 |
| E4h | DEVICE_ID | Returns the 16-byte (character) device identifier string. | Read Block | ASC | | Reads device version | 46 |
| E5h | MFR_IOUT_OC_FAULT_RESPONSE | Configures the I _{OUT} overcurrent fault response. | R/W Byte | BIT | B9h | Disable and 70ms continuous retry | 47 |
| E6h | MFR_IOUT_UC_FAULT_RESPONSE | Configures the I _{OUT} undercurrent fault response. | R/W Byte | BIT | B9h | Disable and 70ms continuous retry | 47 |
| EAh | SNAPSHOT | Returns 32-byte read-back of parametric and status values. | Read Block | BIT | | | 48 |
| F3h | SNAPSHOT_CONTROL | Snapshot feature control command. | R/W Byte | BIT | | | 48 |
| F5h | MFR_VMON_OV_FAULT_LIMIT | Returns the VMON overvoltage threshold. | Read Word | L11 | CB00h | 6V | 49 |
| F6h | MFR_VMON_UV_FAULT_LIMIT | Returns the VMON undervoltage threshold. | Read Word | L11 | CA00h | 4V | 49 |
| F7h | MFR_READ_VMON | Returns the VMON voltage reading. | Read Word | L11 | | | 49 |

6.1 PMBus Data Formats

- **Linear-11 (L11)** - The L11 data format uses 5-bit two’s complement exponent (N) and 11-bit two’s complement mantissa (Y) to represent real world decimal value (X).



The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^N$

- **Linear-16 Unsigned (L16u)** - The L16u data format uses a fixed exponent (hard-coded to $N = -13h$) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$
- **Linear-16 Signed (L16s)** - The L16s data format uses a fixed exponent (hard-coded to $N = -13h$) and a 16-bit two’s complement mantissa (Y) to represent real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$
- **Bit Field (BIT)** - An explanation of the Bit Field for each command is provided in [“PMBus Commands Description” on page 36](#).
- **Custom (CUS)** - An explanation of the Custom data format for each command is provided in [“PMBus Commands Description” on page 36](#). A combination of Bit Field and integer is a common type of Custom data format.
- **ASCII (ASC)** - A variable length string of text characters using the ASCII data format.

6.2 PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, and ASCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Commands not listed in the PMBus command summary are not allowed for customer use, and are reserved for factory use only. Issuing reserved commands can result in unexpected operation.

7. PMBus Commands Description

OPERATION (01h)

Definition: Sets the Enable and Disable settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value:

Units: N/A

| Settings | Actions |
|----------|---------------|
| 00h | Immediate off |
| 40h | Soft off |
| 80h | On |

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 16h (Device starts from ENABLE pin with soft-off)

Units: N/A

| Settings | Actions |
|----------|--|
| 16h | Device starts from the ENABLE pin with soft off. |
| 17h | Device starts from the ENABLE pin with immediate off. |
| 1Ah | Device starts from the OPERATION command with soft off. |
| 1Bh | Device starts from the OPERATION command with immediate off. |

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it only clears the faults.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

Reference: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than VOUT_MAX.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting (set based on VSET_CRS and VSET_FINE)

Units: Volts

Range: 0V to VOUT_MAX

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The command provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. The default value can be changed using PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10 x VOUT pin-strap setting

Units: Volts

Range: 0V to 5.5V

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. The initial default value is defined by a pin-strap, and this value can be overridden by writing this command from the PMBus. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 296kHz to 1067kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: Pin-strap (set based on SMBus address)

Units: N/A

| Bits | Purpose | Value | Description |
|------|-------------------|---------|---|
| 15:8 | Reserved | 0 | These bits are reserved |
| 7:4 | Group Number | 0 to 15 | Sets the group number. A value of 0 is interpreted as 16. |
| 3:0 | Position in Group | 0 to 15 | Sets position of the device's rail within the group. |

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85xVOUT pin-strap setting

Units: V

Range: 0V to VOUT_MAX

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. The device automatically calculates peak inductor overcurrent fault limit for each phase based on the equation: $I_{OUT(PEAK OC LIMIT)} = (0.5 * I_{OUT_OC_FAULT_LIMIT} + 0.5 * I_{RIPPLE(P-P)}) * 120\%$. A hard bound of 55A is applied to the peak overcurrent fault limit per phase.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EAD0h (90A)

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} average undercurrent fault threshold. The device automatically calculates the valley inductor undercurrent fault limit for each phase based on the equation: $I_{OUT(VALLEY UC LIMIT)} = (0.5 * I_{OUT_UC_FAULT_LIMIT} - 0.5 * I_{RIPPLE(P-P)}) * 120\%$. A hard bound of -55A is applied to the valley undercurrent fault limit per phase.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E4E0h (-50A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below the fault level to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB98h (+115°C)

Units: Celsius

Range: 0°C to +150°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E530h (-45°C)

Units: Celsius

Range: -55°C to +25°C

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D3A0h (14.5V)

Units: V

Range: 0V to 16V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for Power-good indication. Power-good asserts after the output voltage exceeds POWER_GOOD_ON . It is recommended to set POWER_GOOD_ON higher than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x VOUT pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2ms to 300ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0ms to 120ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2ms to 300ms

TOFF_FALL (65h)

Definition: Sets the soft-off fall time for V_{OUT} after DISABLE and TOFF_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0ms to 120ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

| Bit Number | Status Bit Name | Meaning |
|------------|-------------------|--|
| 7 | BUSY | A fault was declared because the device was busy and unable to respond. |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault has occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault has occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault has occurred. |
| 2 | TEMPERATURE | A temperature fault has occurred. |
| 1 | CML | A communications, memory, or logic fault has occurred. |
| 0 | None of the Above | A fault not listed in bits 7:1 has occurred. |

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read-only

Default Value: 0000h

Units: N/A

| Bit Number | Status Bit Name | Meaning |
|------------|-------------------|--|
| 15 | VOUT | An output voltage fault has occurred. |
| 14 | IOUT/POUT | An output current or output power fault has occurred. |
| 13 | INPUT | An input voltage, input current, or input power fault has occurred. |
| 12 | MFG_SPECIFIC | A manufacturer specific fault has occurred. |
| 11 | POWER_GOOD# | The POWER_GOOD signal, if present, is negated. |
| 10 | Reserved | This bit is reserved. |
| 9 | OTHER | A bit in STATUS_OTHER is set. |
| 8 | UNKNOWN | A fault type not given in Bits 15:1 of the STATUS_WORD has been detected. |
| 7 | BUSY | A fault was declared because the device was busy and unable to respond. |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault has occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault has occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault has occurred. |
| 2 | TEMPERATURE | A temperature fault has occurred. |
| 1 | CML | A communications, memory, or logic fault has occurred. |
| 0 | None of the Above | A fault not listed in Bits 7:1 has occurred. |

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|---|
| 7 | VOUT_OV_FAULT | Indicates an output overvoltage fault. |
| 6 | Reserved | This bit is reserved. |
| 5 | Reserved | This bit is reserved. |
| 4 | VOUT_UV_FAULT | Indicates an output undervoltage fault. |
| 3:0 | N/A | These bits are not used. |

STATUS_IOUT (7Bh)**Definition:** Returns one data byte with the status of the output current.**Data Length in Bytes:** 1**Data Format:** BIT**Type:** Read-only**Default Value:** 00h**Units:** N/A

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|--|
| 7 | IOUT_OC_FAULT | An output overcurrent fault has occurred. |
| 6 | Reserved | This bit is reserved. |
| 5 | Reserved | This bit is reserved. |
| 4 | IOUT_UC_FAULT | An output undercurrent fault has occurred. |
| 3:0 | N/A | These bits are not used. |

STATUS_INPUT (7Ch)**Definition:** Returns the input voltage and input current status information.**Data Length in Bytes:** 1**Data Format:** BIT**Type:** Read-only**Default Value:** 00h**Units:** N/A

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|---|
| 7 | VIN_OV_FAULT | An input overvoltage fault has occurred. |
| 6 | Reserved | This bit is reserved. |
| 5 | Reserved | This bit is reserved. |
| 4 | VIN_UV_FAULT | An input undervoltage fault has occurred. |
| 3:0 | N/A | These bits are not used. |

STATUS_TEMPERATURE (7Dh)**Definition:** Returns one byte of information with a summary of any temperature related faults.**Data Length in Bytes:** 1**Data Format:** BIT**Type:** Read-only**Default Value:** 00h**Units:** N/A

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|--|
| 7 | OT_FAULT | An over-temperature fault has occurred. |
| 6 | Reserved | This bit is reserved. |
| 5 | Reserved | This bit is reserved. |
| 4 | UT_FAULT | An under-temperature fault has occurred. |
| 3:0 | N/A | These bits are not used. |

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

| Bit Number | Meaning |
|------------|---|
| 7 | Invalid or unsupported PMBus command was received. |
| 6 | The PMBus command was sent with invalid or unsupported data. |
| 5 | Packet error was detected in the PMBus command. |
| 4 | Mem/Logic fault. |
| 3:2 | Reserved. |
| 1 | A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred. |
| 0 | Reserved |

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default value: 00h

Units: N/A

| Bit Number | Field Name | Meaning |
|------------|---------------------------------|---|
| 7:4 | Reserved | These bits are reserved. |
| 3 | External Switching Period Fault | Loss of external clock synchronization has occurred. |
| 2 | Reserved | This bit is reserved. |
| 1 | VMON UV Fault | The voltage on the VMON pin has dropped below the level set by VMON_UV_FAULT_LIMIT. |
| 0 | VMON OV Fault | The voltage on the VMON pin has risen above the level set by VMON_OV_FAULT_LIMIT. |

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: L16u

Type: Read-only

Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Default Value: N/A

Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor. Note that the junction temperature of the power stage in the module may be higher than the READ_INTERNAL_TEMP command value, and the temperature difference depends on the operating condition. In some cases, the power stage junction temperature can be 30°C higher than the READ_INTERNAL_TEMP command value.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: kHz

READ_IOUT_0 (96h)**Definition:** Returns the Phase 1 current reading.**Data Length in Bytes:** 2**Data Format:** L11**Type:** Read-only**Default Value:** N/A**Units:** A**READ_IOUT_1 (97h)****Definition:** Returns the Phase 2 current reading.**Data Length in Bytes:** 2**Data Format:** L11**Type:** Read-only**Default Value:** N/A**Units:** A**ASCR_CONFIG (DFh)**

Definition: Allows user configuration of ASCR settings. ASCR gain is analogous to bandwidth and ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation. Typical ASCR gain settings range from 50 to 1000, and ASCR residual settings range from 10 to 100.

Data Length in Bytes: 4**Data Format:** CUS**Type:** R/W**Default Value:** Pin-strap setting

| Bit | Purpose | Data Format | Value | Description |
|-------|-----------------------|-------------|----------|----------------------|
| 31:24 | Unused | | 0000000h | Unused |
| 24 | Reserved | | | This bit is reserved |
| 23:16 | ASCR Residual Setting | Integer | | ASCR residual |
| 15:0 | ASCR Gain Setting | Integer | | ASCR gain |

DEVICE_ID (E4h)**Definition:** Returns the 16-byte (character) device identifier string.**Data Length in Bytes:** 16**Data Format:** ASC**Type:** Block Read**Default Value:** Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable, and 70ms continuous retry)

Units: N/A

| Field Name | Actions |
|------------|--|
| 80h | Disable with no retry. |
| B9h | Disable and continuous retry with 70ms delay |

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and 70ms continuous retry)

Units: N/A

| Field Name | Actions |
|------------|--|
| 80h | Disable with no retry. |
| B9h | Disable and continuous retry with 70ms delay |

SNAPSHOT (EAh)

Definition: 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, last updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is set to stored, the device no longer automatically captures parametric and status values following fault until stored data are erased. Use the SNAPSHOT_CONTROL command to erase store data and clear the status bit before next ramp up. Data erase is not allowed when the module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

| Byte Number | Value | Pmbus Command | Format |
|-------------|--|---------------------------|--------|
| 31:23 | Reserved | These bits are reserved | 00h |
| 22 | Flash Memory Status Byte FF - Not Stored 00 - Stored | N/A | BIT |
| 21 | Manufacturer Specific Status Byte | STATUS_MFR_SPECIFIC (80h) | Byte |
| 20 | CML Status Byte | STATUS_CML (7Eh) | Byte |
| 19 | Temperature Status Byte | STATUS_TEMPERATURE (7Dh) | Byte |
| 18 | Input Status Byte | STATUS_INPUT (7Ch) | Byte |
| 17 | I _{OUT} Status Byte | STATUS_IOUT (7Bh) | Byte |
| 16 | V _{OUT} Status Byte | STATUS_VOUT (7Ah) | Byte |
| 15:14 | Switching Frequency | READ_FREQUENCY (95h) | L11 |
| 13:12 | Reserved | These bits are reserved | 00h |
| 11:10 | Internal Temperature | READ_INTERNAL_TEMP (8Dh) | L11 |
| 9:8 | Duty Cycle | READ_DUTY_CYCLE (94h) | L11 |
| 7:6 | Reserved | These bits are reserved | L11 |
| 5:4 | Output Current | READ_IOUT (8Ch) | L11 |
| 3:2 | Output Voltage | READ_VOUT (8Bh) | L16u |
| 1:0 | Input Voltage | READ_VIN (88h) | L11 |

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h causes the device to copy the current Snapshot values from NVRAM to the 32-byte Snapshot command parameter. Writing a 02h causes the device to write the current Snapshot values to NVRAM. Writing an 03h erases all Snapshot values from NVRAM. Write (02h) and Erase (03h) can be used only when the device is disabled. All other values are ignored.

Data Length in Bytes: 1

Data Format: Bit field

Type: R/W byte

| Value | Description |
|-------|---|
| 01h | Read Snapshot values from NV RAM |
| 02h | Write Snapshot values to NV RAM |
| 03h | Erase Snapshot values stored in NV RAM. |

MFR_VMON_OV_FAULT_LIMIT (F5h)**Definition:** Reads the VMON OV fault threshold.**Data Length in Bytes:** 2**Data Format:** L11**Type:** Read only**Default Value:** CB00h (6V)**Units:** V**Range:** 4V to 6V**MFR_VMON_UV_FAULT_LIMIT (F6h)****Definition:** Reads the VMON UV fault threshold**Data Length in Bytes:** 2**Data Format:** L11**Type:** Read only**Default Value:** CA00h (4V)**Units:** V**Range:** 4V to 6V**MFR_READ_VMON (F7h)****Definition:** Reads the VMON voltage.**Data Length in Bytes:** 2**Data Format:** L11**Type:** Read only**Default Value:** N/A**Units:** V**Range:** 4V to 6V

8. Revision History

8.1 Firmware

Table 13. RAA210870 Nomenclature Guide

| Firmware Revision Code | Change Description | Note |
|------------------------|--------------------|-----------------------------|
| RAA210870--G0100 | Initial Release | Recommended for new designs |

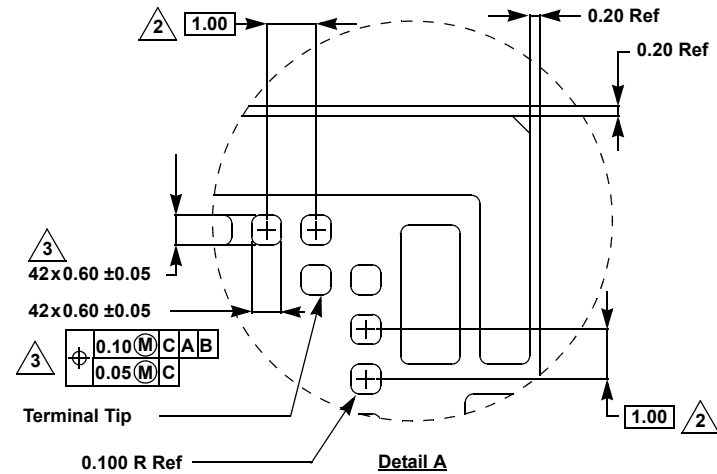
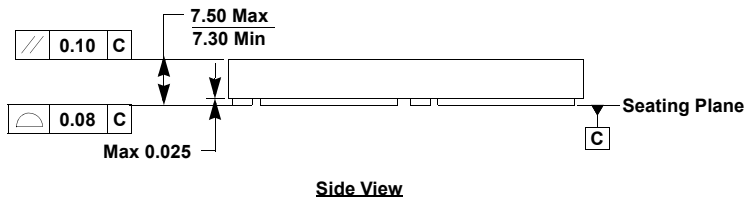
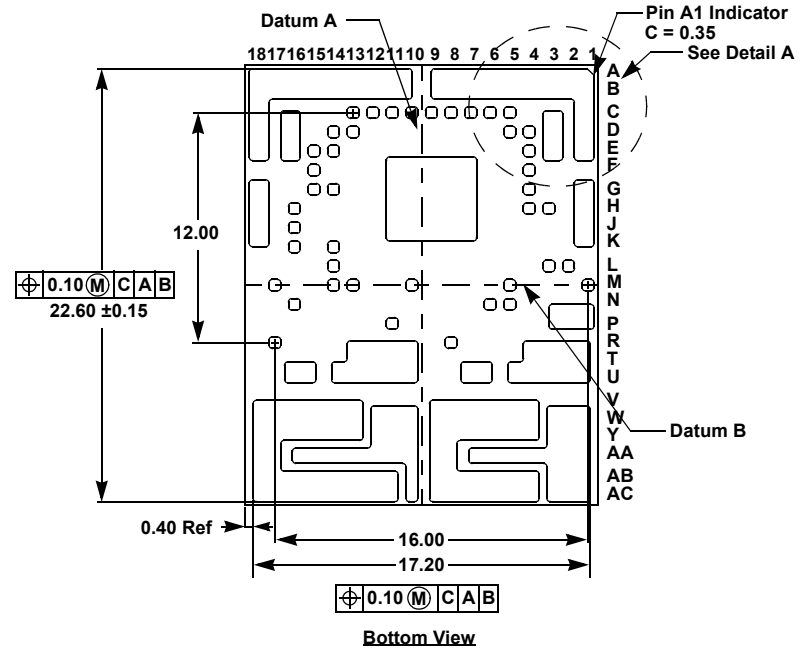
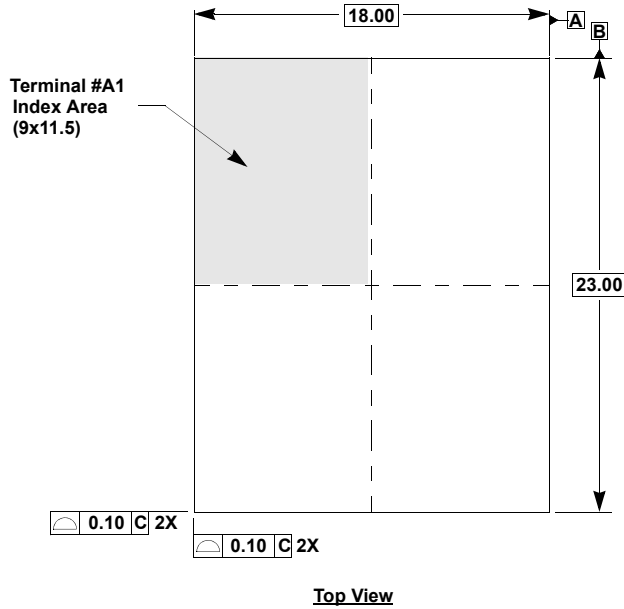
8.2 Datasheet

| Rev. | Date | Description |
|------|--------------|---|
| 1.0 | Oct 23, 2018 | Updated PG pin description on page 11. Updated pin configuration to show correct location for M5 and N5. Changed PMBus to SMBus in the SMBus Communications section. Changed 5V to 2.5V in the sentence after Table 6 on page 21. Changed On-Nominal to On in the table under the OPERATION section on page 36. Changed Reserved to Output Current for Bits5:4 value in the SNAPSHOT section on page 48. |
| 0.00 | Sep 10, 2018 | Initial release |

9. Package Outline Drawing

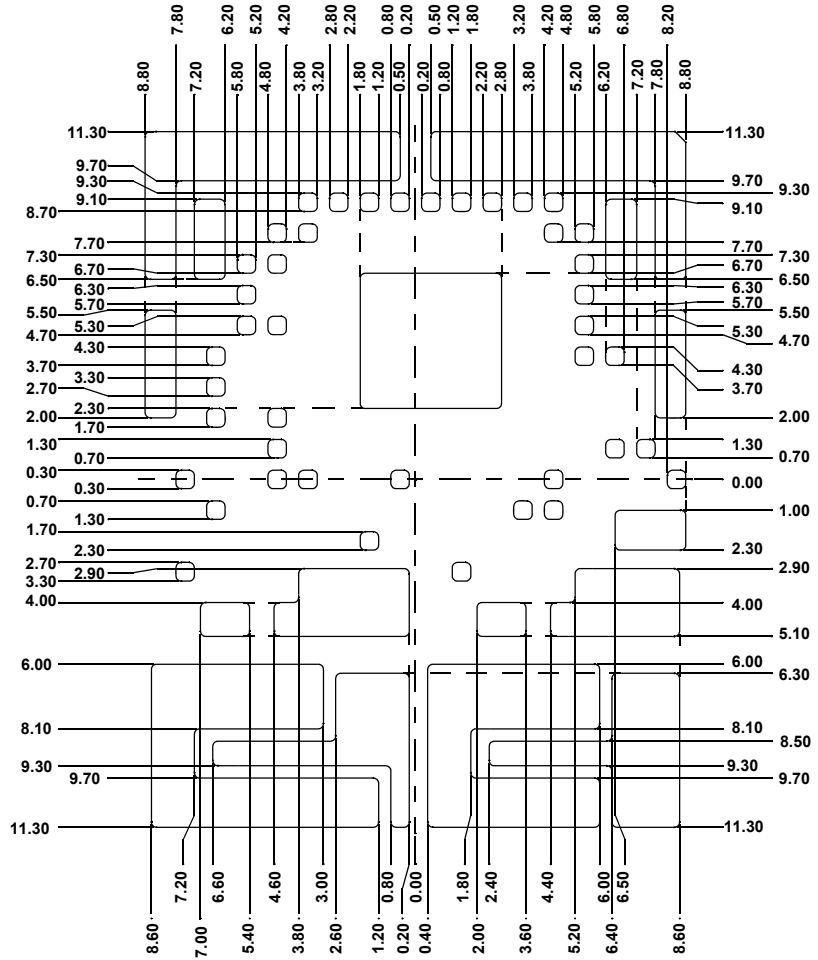
Y58.18x23
58 I/O 18mmx23mmx7.5mm Custom HDA Module
Rev 4, 4/18

For the most recent package outline drawing, see [Y58.18x23](#).

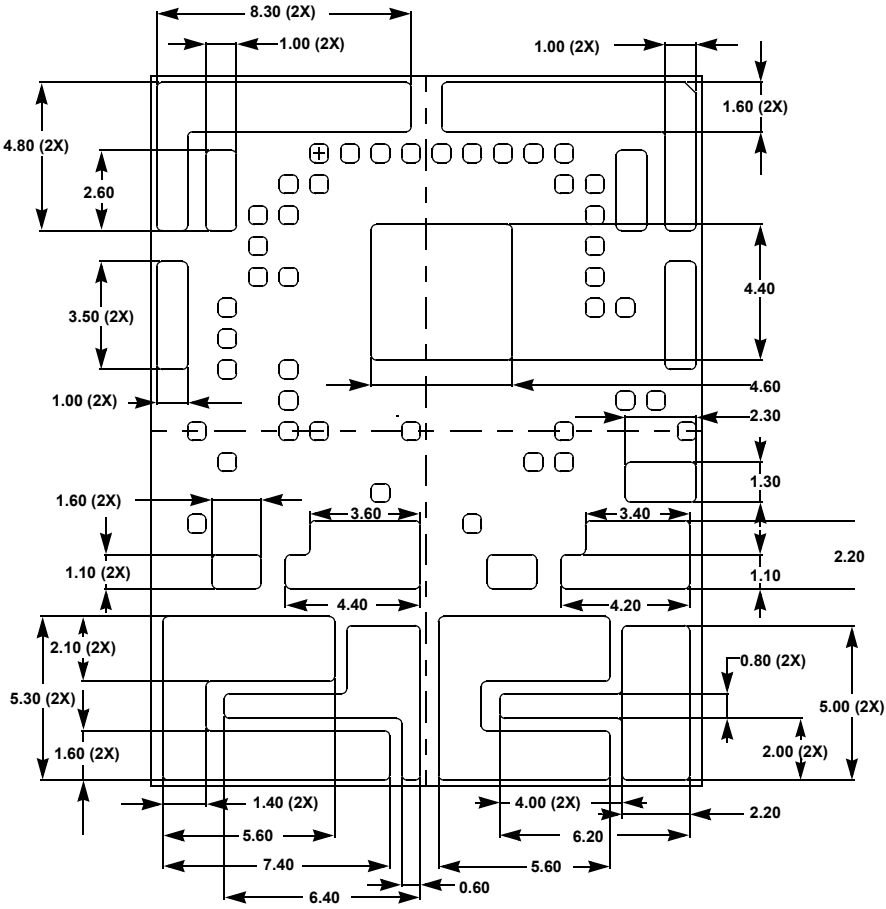


Notes:

1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 42 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension on page 3 is ±0.1mm.

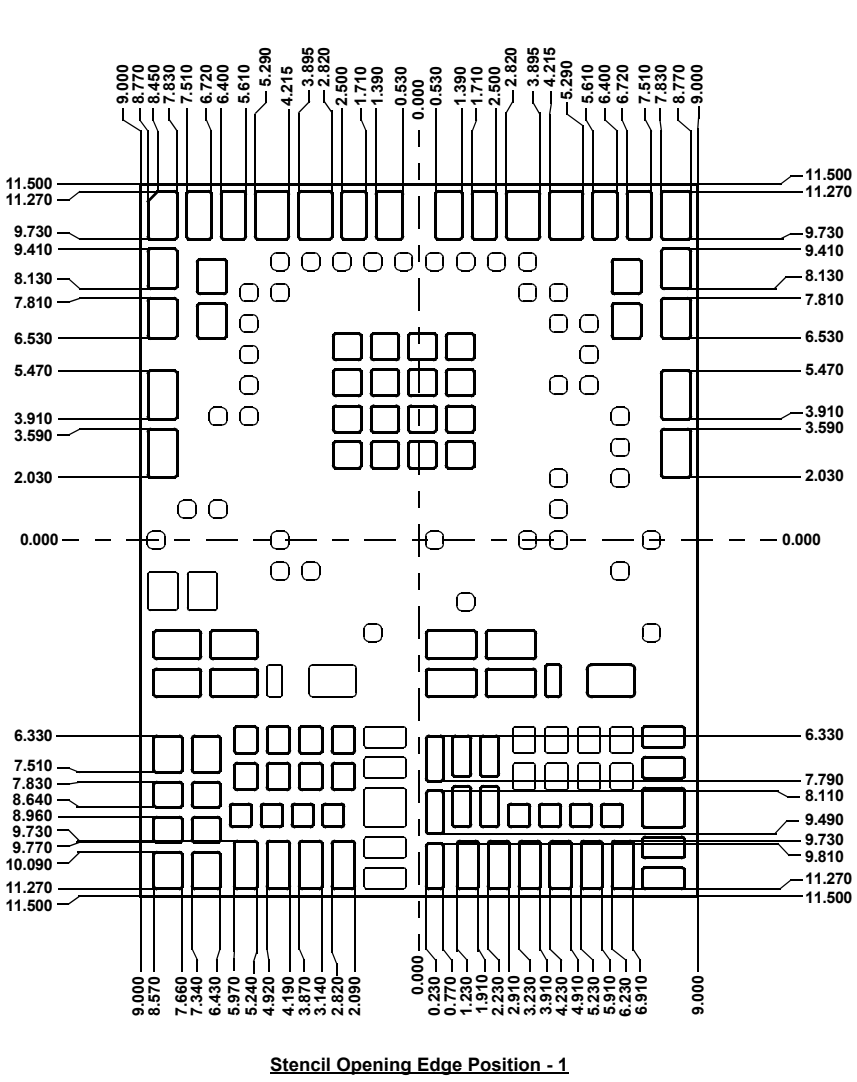
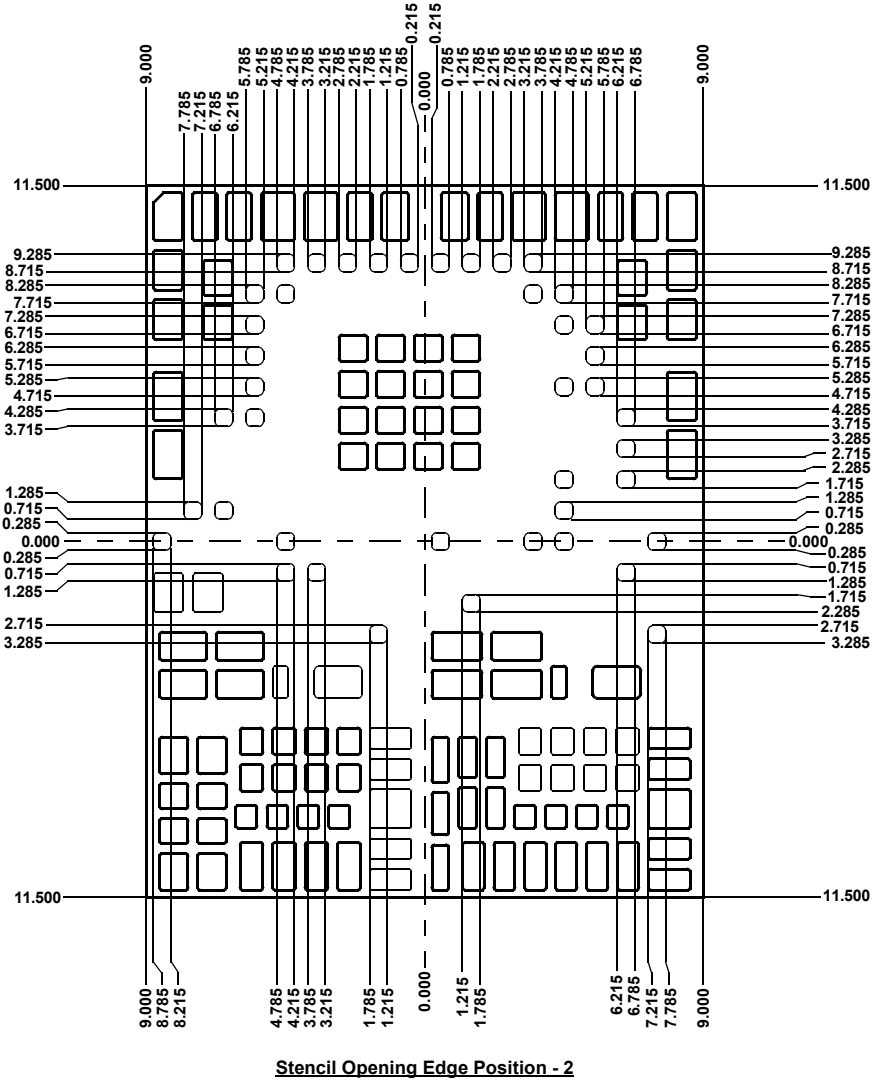


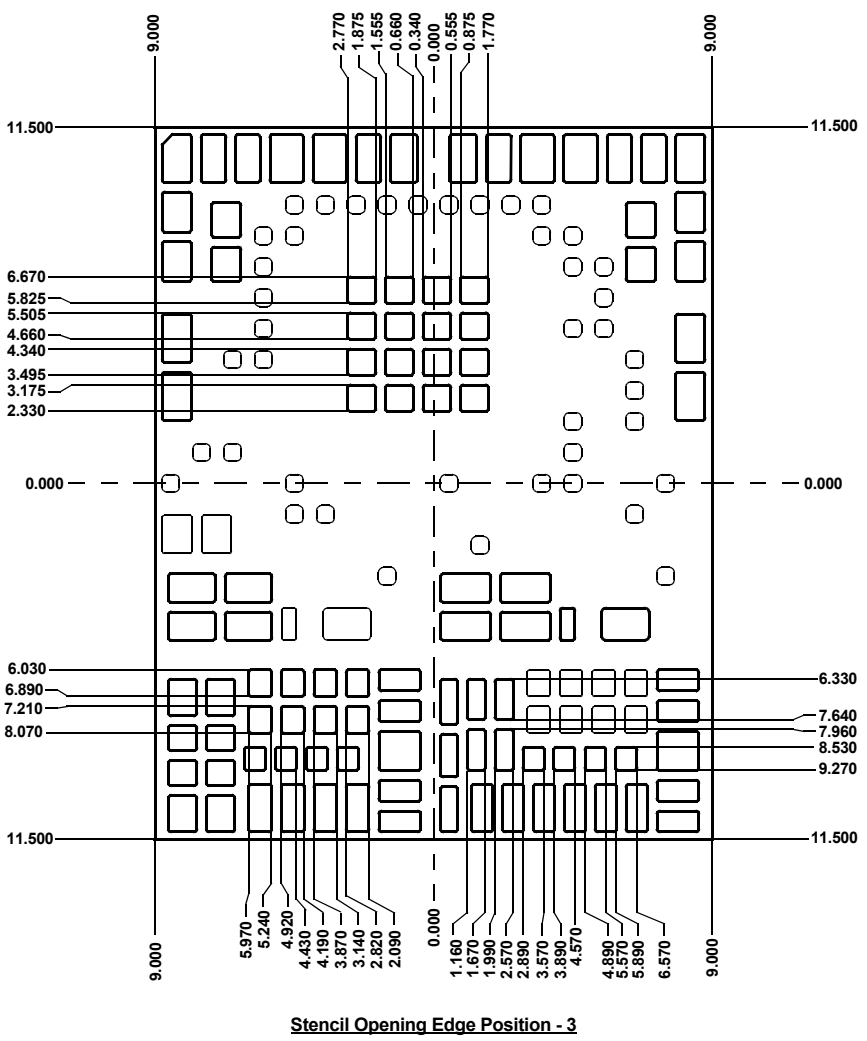
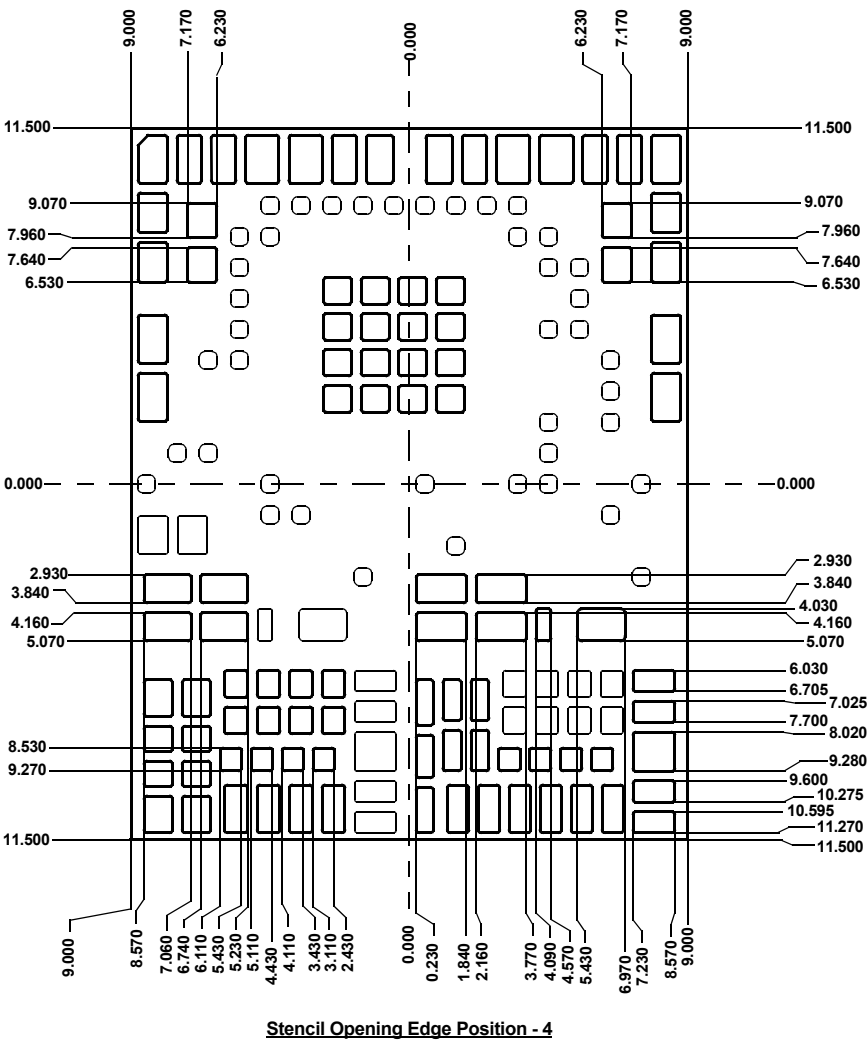
Terminal and Pad Edge Details

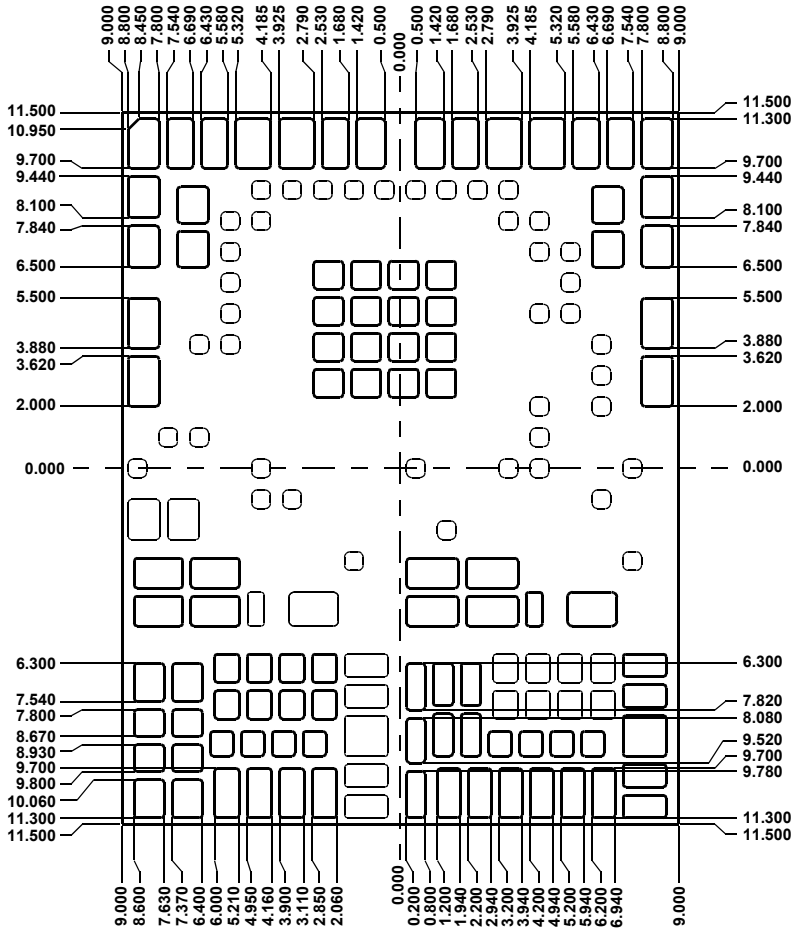


Size Details for the 16 Exposed Pads

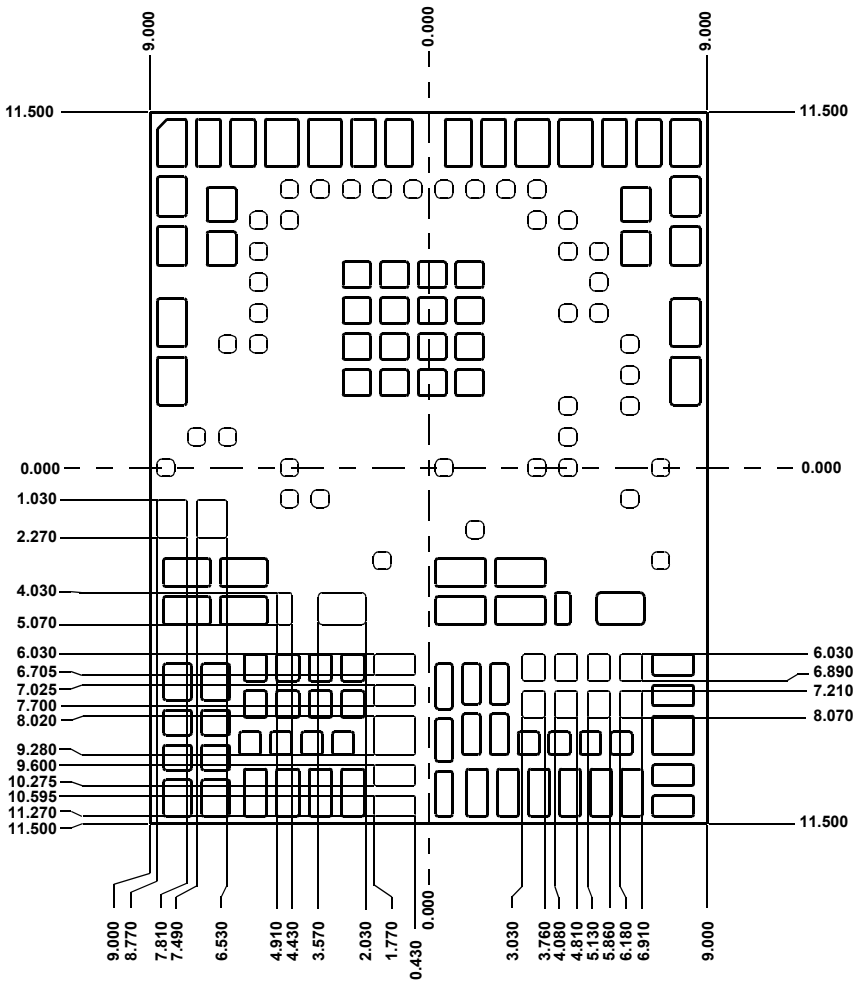
Bottom View



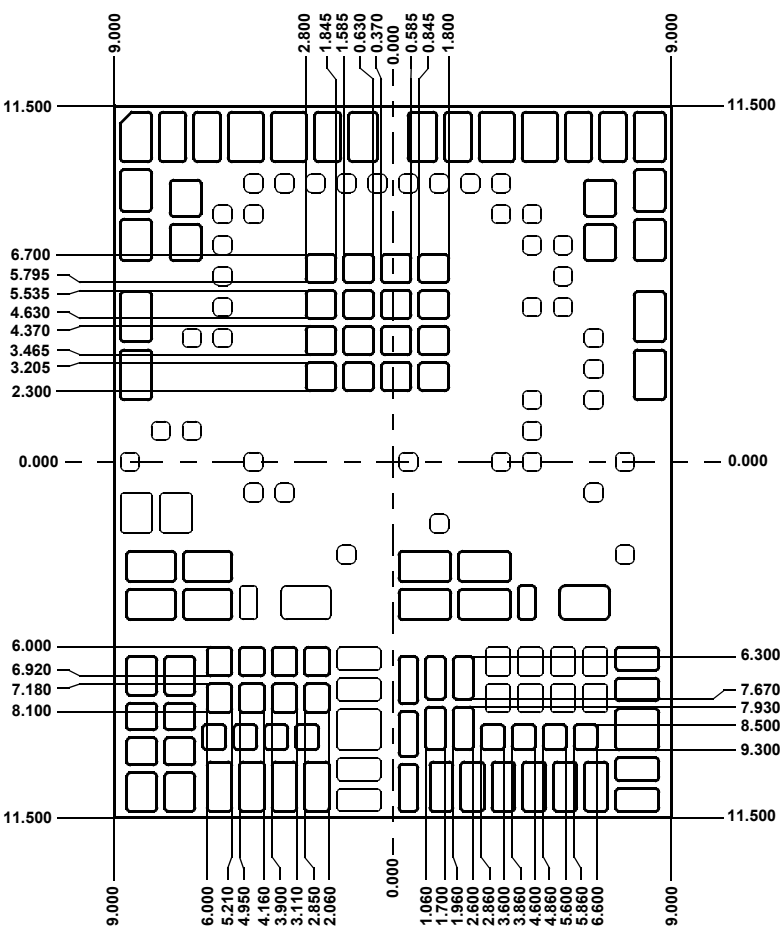




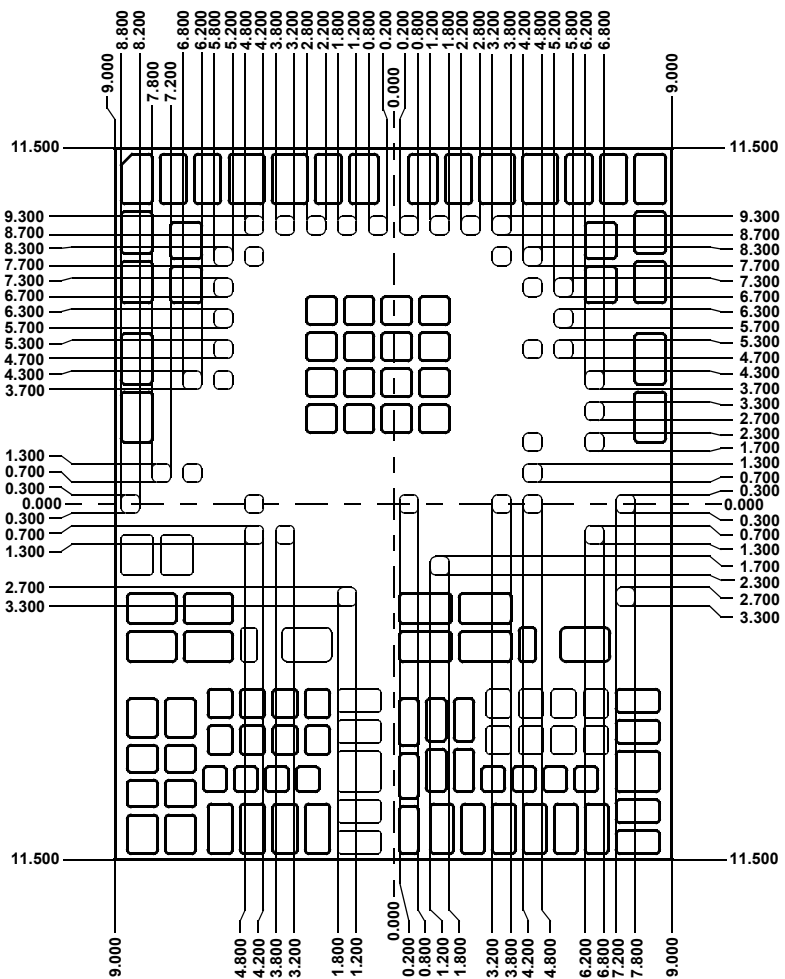
PCB Land Pattern - 1 (for Reference)



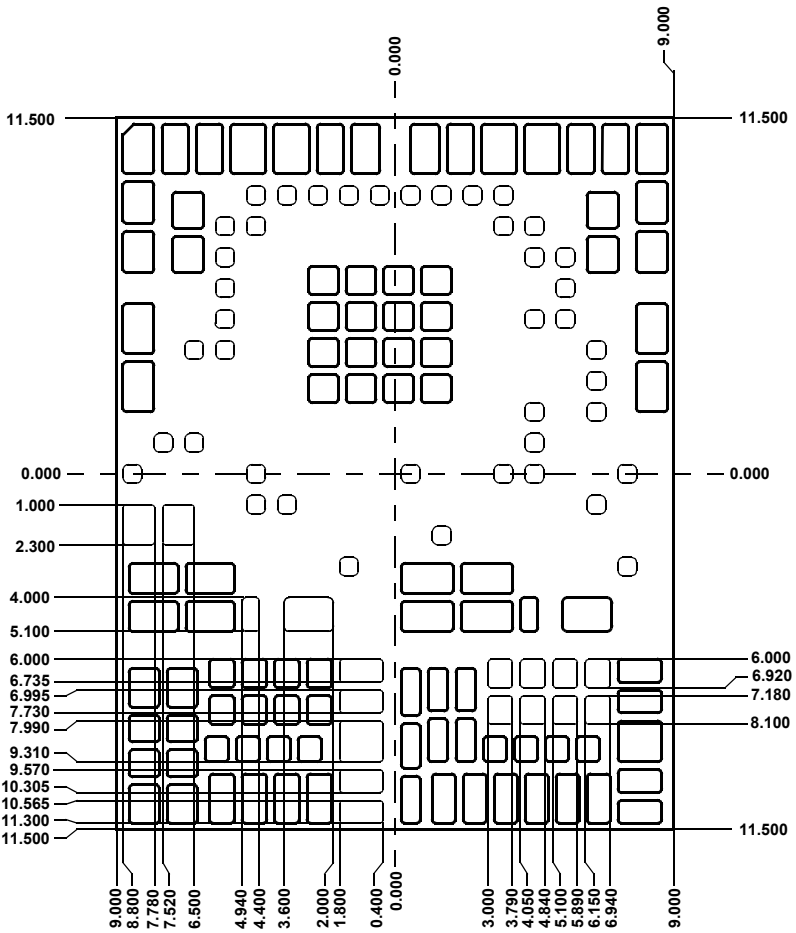
Stencil Opening Edge Position - 5



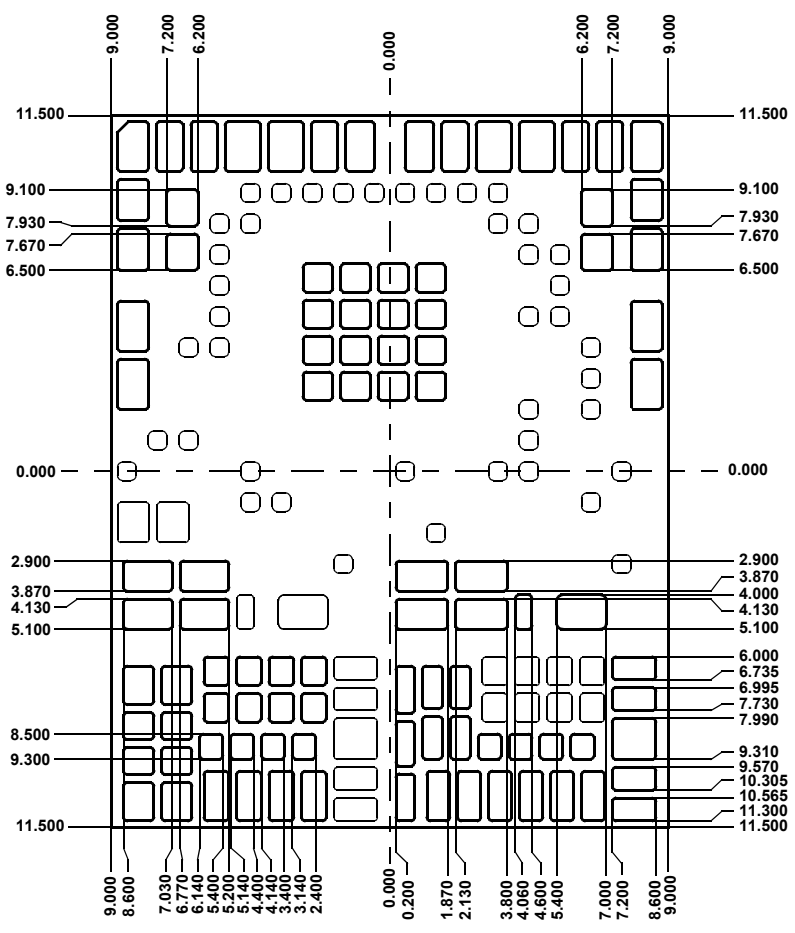
PCB Land Pattern - 3 (for Reference)



PCB Land Pattern - 2 (for Reference)



PCB Land Pattern - 5 (for Reference)



PCB Land Pattern - 4 (for Reference)

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(Rev.4.0-1 November 2017)



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Renesas Electronics Corporation

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.

1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.

17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А