

## N-channel 30 V, 6 mΩ typ., 11 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data

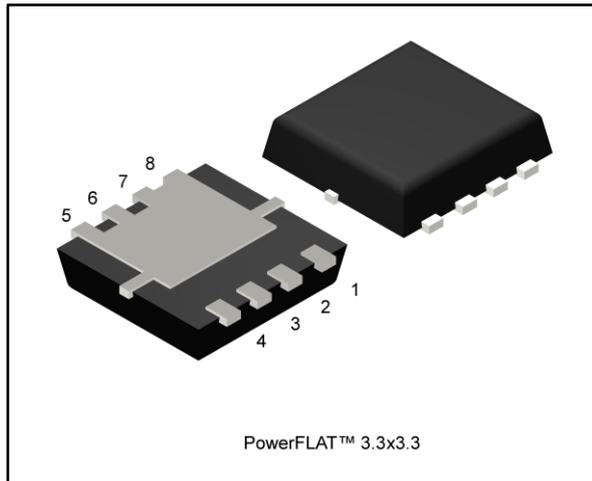
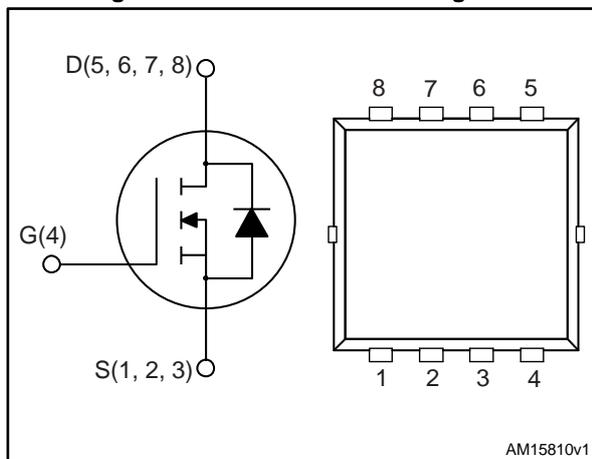


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL11N3LLH6	30 V	7.5 mΩ	11 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL11N3LLH6	11N3L	PowerFLAT™ 3.3x3.3	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	11	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	6.9	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	2.9	W
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ °C}$	45	W
$T_j$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		

**Notes:**

(1) This value is rated according to  $R_{thj-pcb}$ .

(2) Pulse width limited by safe operating area.

(3) The value is rated according to  $R_{thj-c}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.8	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	°C/W

**Notes:**

(1) When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = 5.5\text{ A}$ , $L = 6\text{ mH}$ )	90	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified).

**Table 5: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}$ <sup>(1)</sup>			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.5\text{ A}$		6	7.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 5.5\text{ A}$		8.4	9.5	m $\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1690	-	pF
$C_{oss}$	Output capacitance		-	290	-	pF
$C_{rss}$	Reverse transfer capacitance		-	176	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 11\text{ A}$ , $V_{GS} = 0\text{ to }4.5\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	17	-	nC
$Q_{gs}$	Gate-source charge		-	8	-	nC
$Q_{gd}$	Gate-drain charge		-	7	-	nC
$R_G$	Gate input resistance charge	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.7	-	$\Omega$

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 5.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> : "Test circuit for resistive load switching times")	-	9.5	-	ns
$t_r$	Rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	37	-	ns
$t_f$	Fall time		-	12	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 11\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_D = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 24\text{ V}$	-	24		ns
$Q_{rr}$	Reverse recovery charge		-	16.8		nC
$I_{RRM}$	Reverse recovery current		-	1.4		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

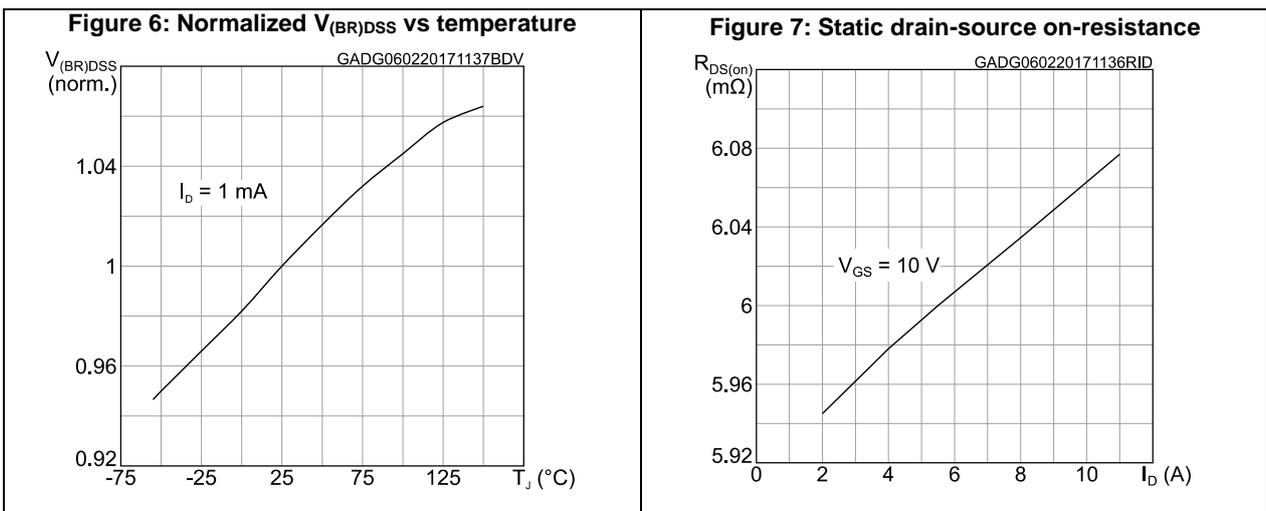
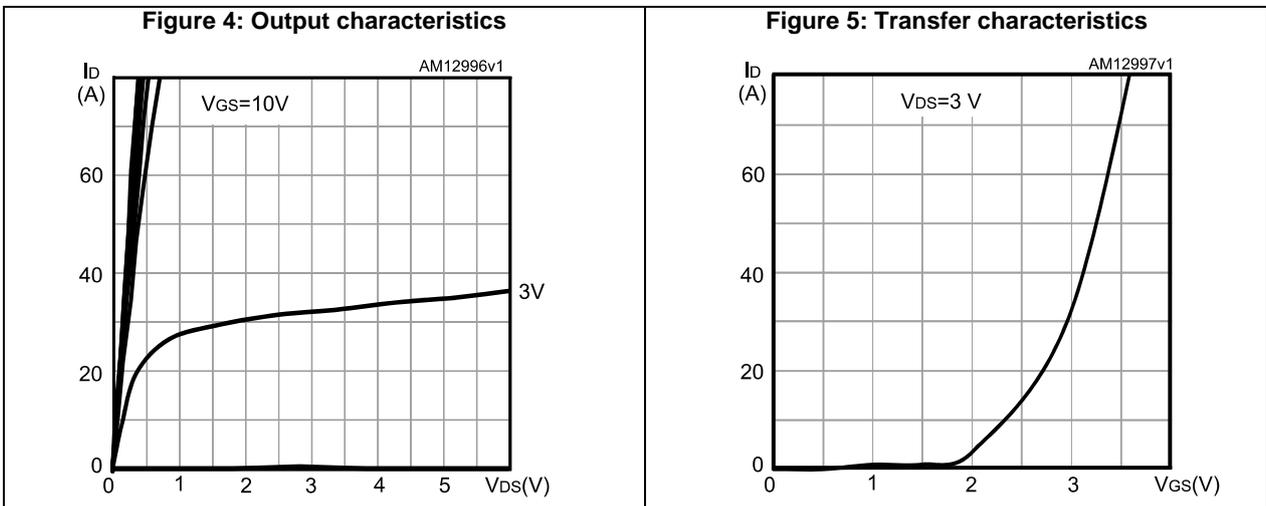
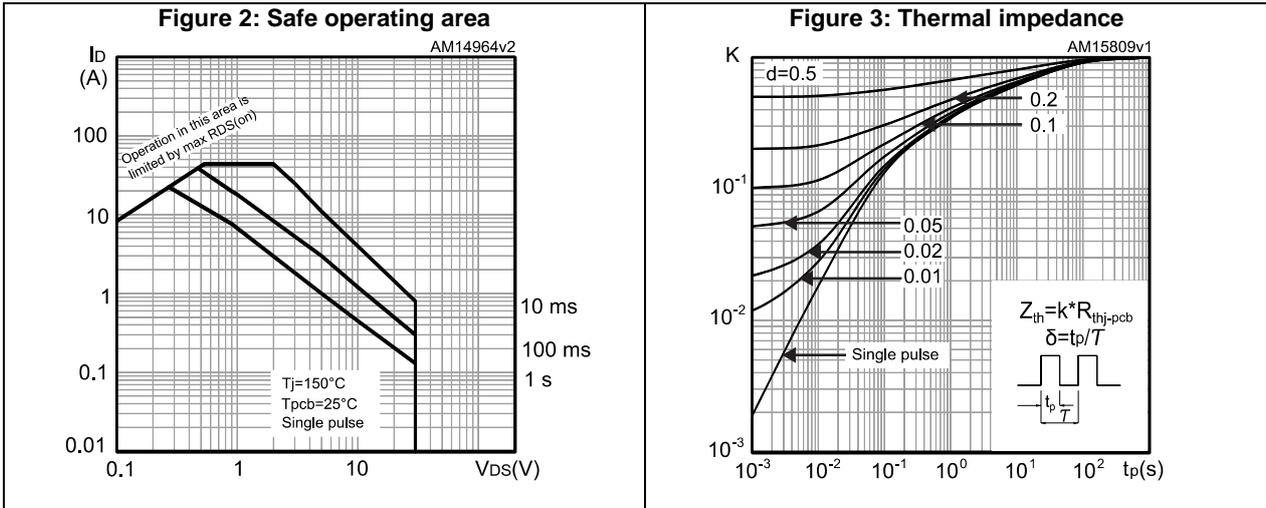


Figure 8: Gate charge vs gate-source voltage

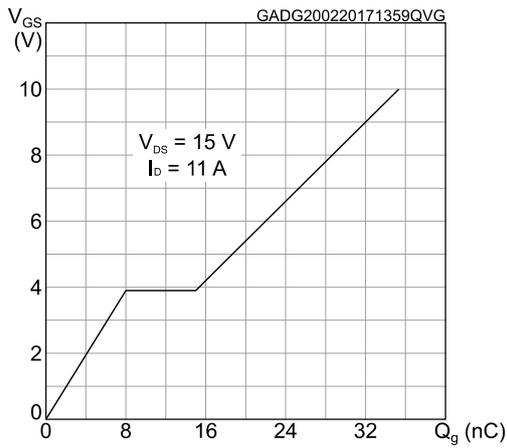


Figure 9: Capacitance variations

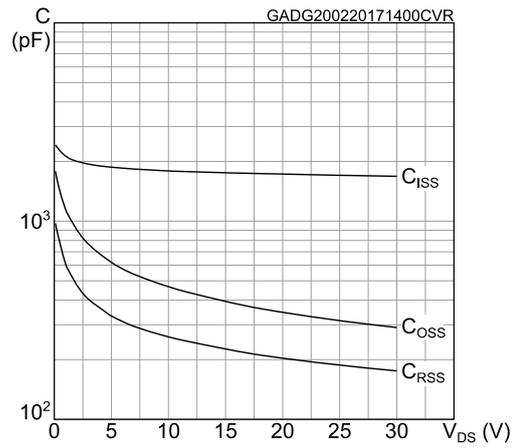


Figure 10: Normalized gate threshold voltage vs temperature

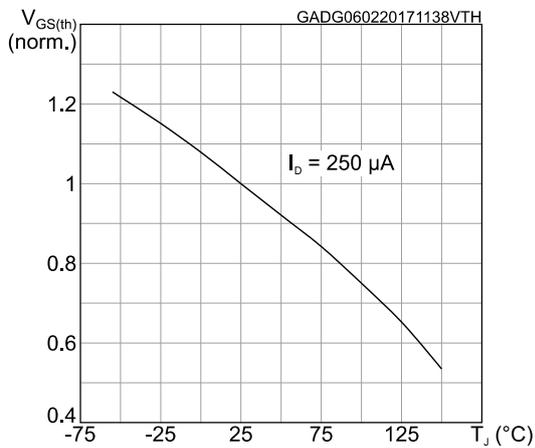


Figure 11: Normalized on-resistance vs temperature

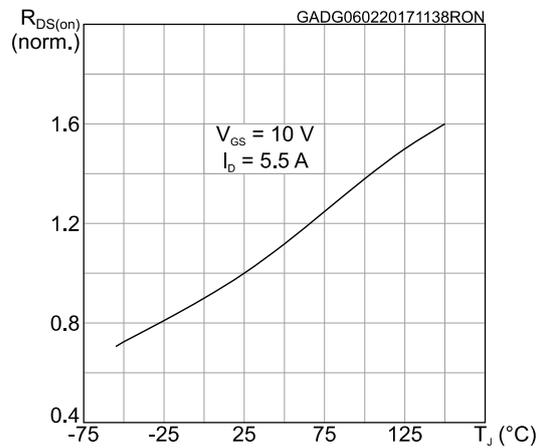
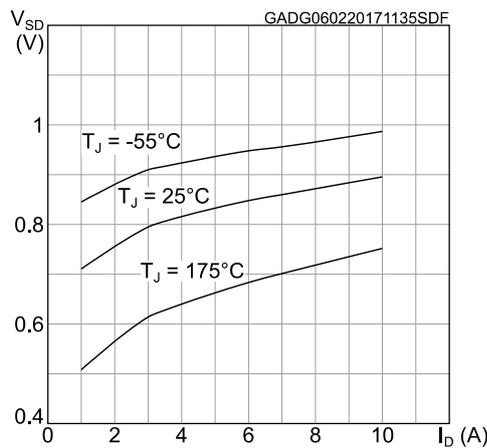
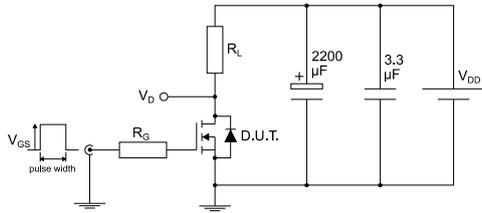


Figure 12: Source-drain diode forward characteristics



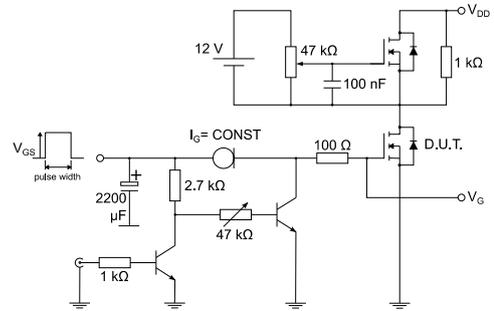
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



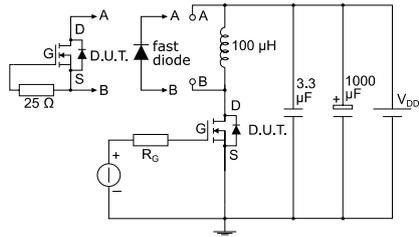
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**Figure 14: Test circuit for gate charge behavior**



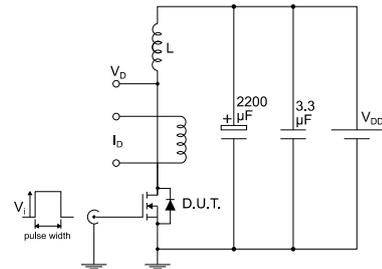
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



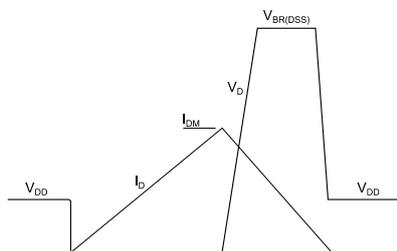
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**Figure 16: Unclamped inductive load test circuit**



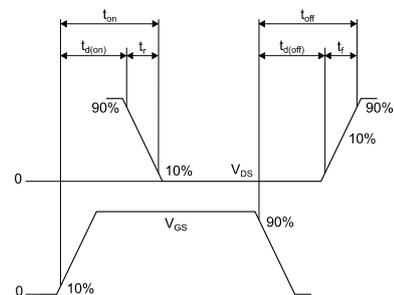
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 3.3x3.3 package information

Figure 19: PowerFLAT™ 3.3x3.3 package outline

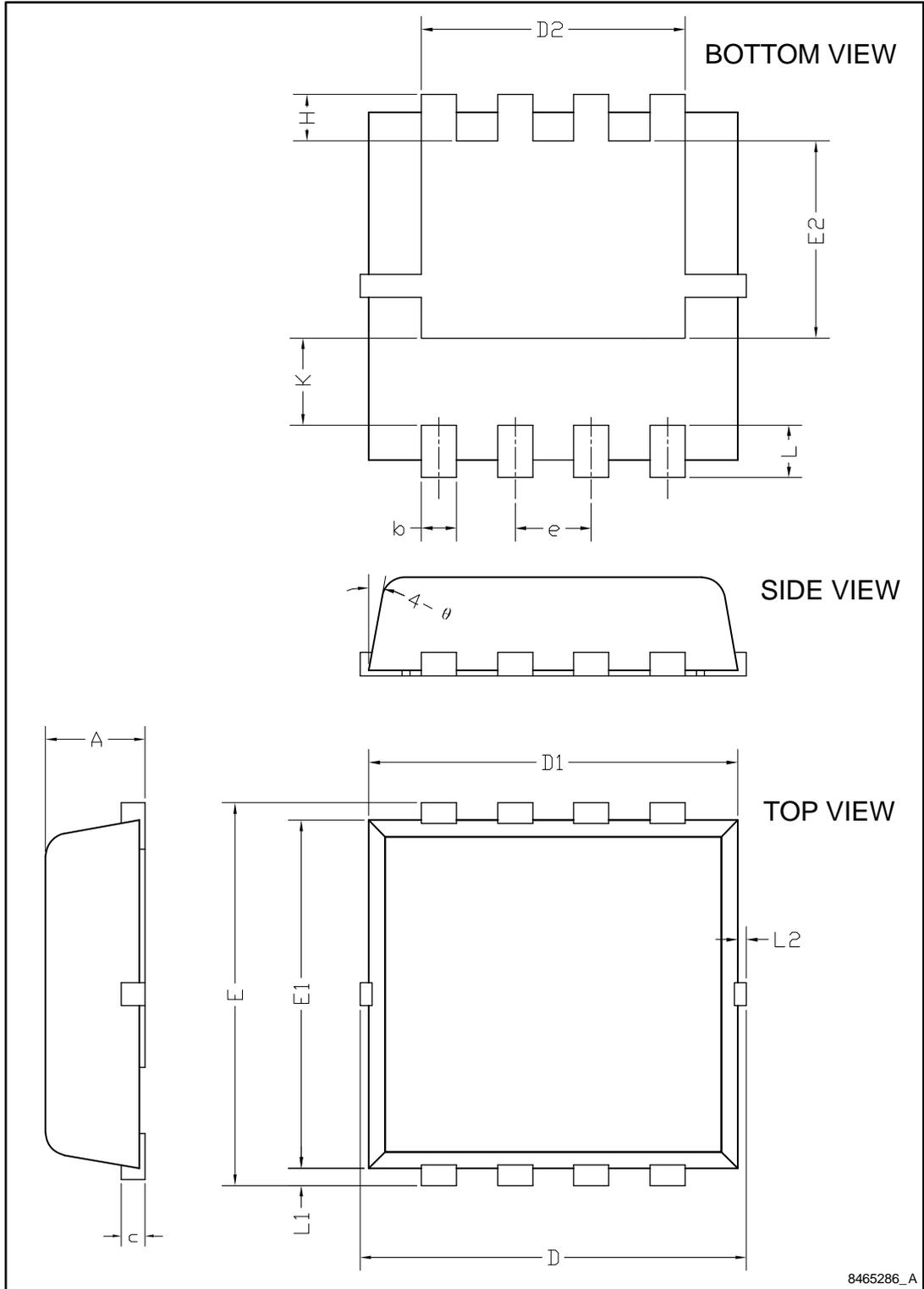
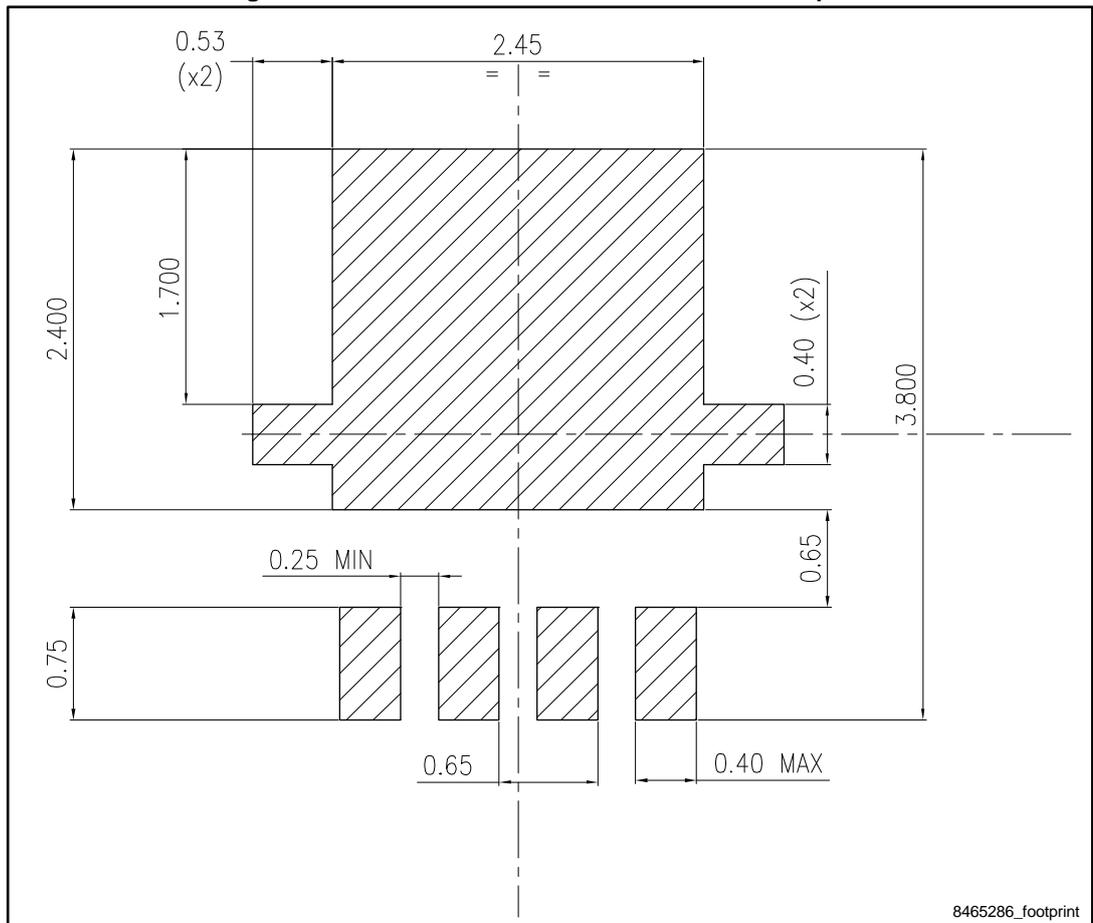


Table 9: PowerFLAT™ 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
$\theta$	8°	10°	12°

Figure 20: PowerFLAT™ 3.3x3.3 recommended footprint



## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
04-Jan-2017	1	First release
11-Jan-2017	2	Updated information on cover page.
20-Feb-2017	3	Updated title, features and description on cover page. Updated <a href="#">Section 1: "Electrical ratings"</a> . Updated <a href="#">Section 2: "Electrical characteristics"</a> . Minor text changes

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