80296SA COMMERCIAL CHMOS 16-BIT MICROCONTROLLER

- **50 MHz Operation**†
- **6 Mbytes of Linear Address Space**
- **512 Bytes of Register RAM**
- **2 Kbytes of Code/Data RAM**
- **Register-register Architecture**
- **Footprint and Functionally Compatible Upgrade for the 8XC196NP and 80C196NU**
- **Optional Phase-locked Loop (PLL) Circuitry with 2x or 4x Clock Multiplier**
- **32 I/O Port Pins**
- **19 Interrupt Sources, 14 with Programmable Priorities**
- **4 External Interrupt Pins and NMI Pin**
- **2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability**
- **3 Pulse-width Modulator (PWM) Outputs with High Drive Capability**
- **Full-duplex Serial Port with Dedicated Baud-rate Generator**

† 40 MHz standard; 50 MHz is Speed Premium

- **Chip-select Unit**
  - **— 6 Chip-select Pins**
  - **— Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select**
  - **— Programmable Wait States (0–15) for Each Chip Select**
  - **— Programmable Bus Width (8- or 16-bit) for Each Chip Select**
  - **— Programmable Address Range for Each Chip Select**
- **Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels**
- **Multiply and Accumulate Executes in 80 ns Using the 40-bit Hardware Accumulator**
- **880 ns 32/16 Unsigned Division**
- **100-pin QFP Package**
- **Complete System Development Support**
- **High-speed CHMOS Technology**

The 80296SA is a member of Intel's 16-bit MCS® 96 microcontroller family. The 80296SA features 6 Mbytes of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. The device has hardware and instructions to support various digital signal processing algorithms.

NOTE

This datasheet contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

January 1997 **Order Number:** 272748-003

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641
or call 1-800-548-4725

80296SA Commercial
CHMOS 16-bit Microcontroller

FIGURES

TABLES

1.0 PRODUCT OVERVIEW

The 80296SA is a member of Intel's 16-bit MCS® 96 microcontroller family. The 80296SA features 6 Mbytes of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. The device has hardware and instructions to support various digital signal processing algorithms.

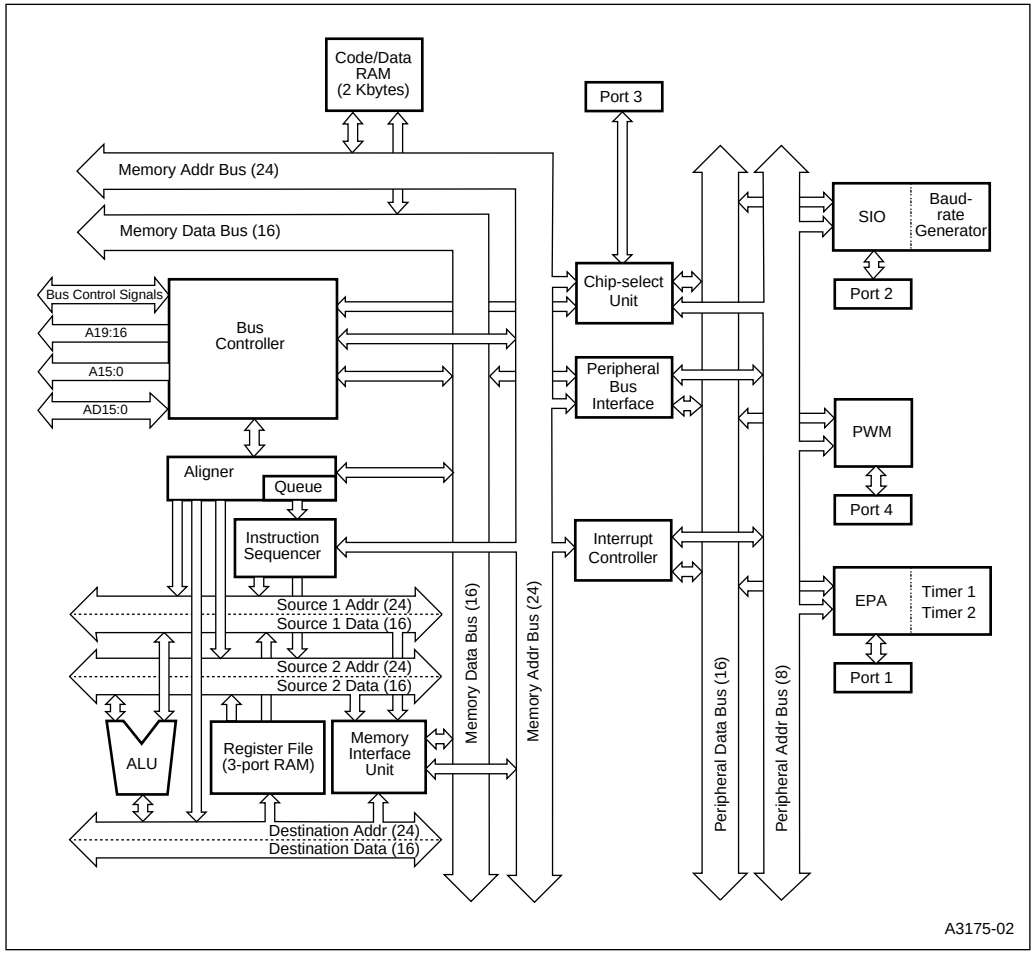


Figure 1. 80296SA Block Diagram

2.0 NOMENCLATURE OVERVIEW

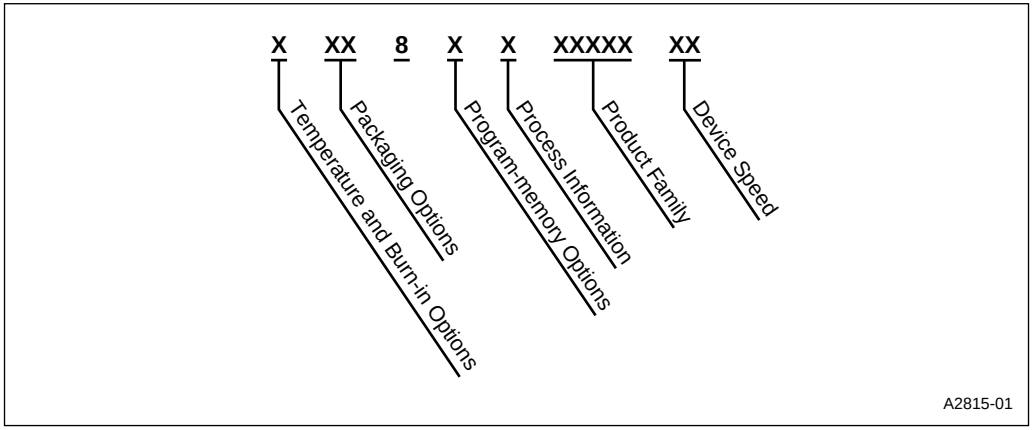


Figure 2. The 80296SA Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	S	QFP
Program–memory Options	0	Without ROM
Process Information	no mark	CHMOS
Product Family	296SA	—
Device Speed	40	40 MHz
	50	50 MHz

3.0 PINOUT

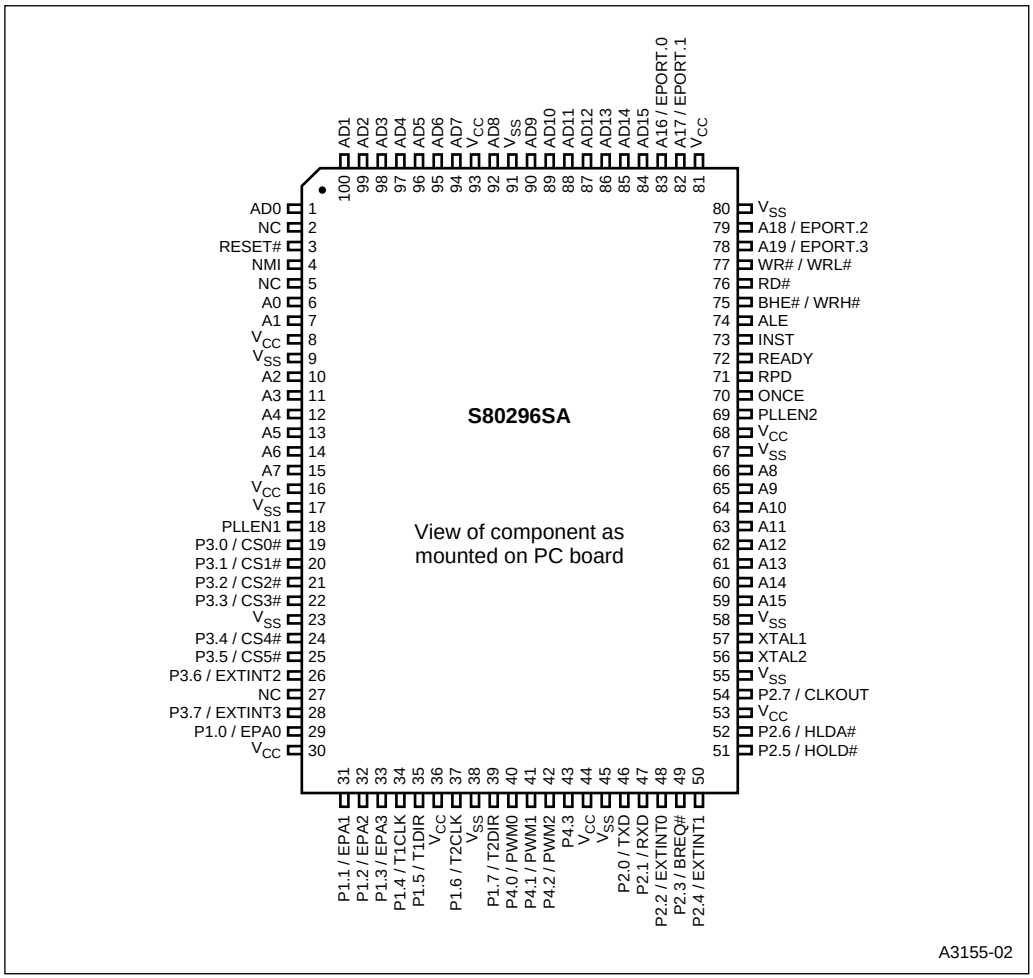


Figure 3. 80296SA 100-pin QFP Package

Table 2. 80296SA 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	NC (see Note)	27	NC (see Note)	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	V_{CC}	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	NC (see Note)	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	PLLEN1	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	PLLEN2	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

NOTE: For compatibility with future products, tie pin 5 to V_{CC} and leave pins 2 and 27 unconnected.

Table 3. 80296SA 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88

Address & Data (continued)	
Name	**Pin**
AD12	87
AD13	86
AD14	85
AD15	84
Bus Control & Status	
Name	**Pin**
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	**Pin**
CLKOUT	54
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56
PLLEN1	18
PLLEN2	69

Input/Output	
Name	**Pin**
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	**Pin**
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	53
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	80
V_{SS}	91

No Connection	
Name	**Pin**
NC	2
NC	5
NC	27

4.0 SIGNALS

Table 4. Signal Descriptions

Name	Type	Description
A15:0	I/O	System Address Bus These address pins provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.
A19:16	I/O	Address Pins 16–19 These address pins provide address bits 16–19 during the entire external memory cycle during both multiplexed and demultiplexed bus modes, supporting extended addressing of the 1-Mbyte address space. **NOTE:** Internally, there are 24 address bits; however, only 20 external address pins (A19:0) are implemented. The internal address space is 16 Mbytes (000000–FFFFFFH) and the external address space is 1 Mbyte (00000–FFFFFH). The microcontroller resets to FF2080H. A19:16 share package pins with EPORT.3:0.
AD15:0	I/O	Address/Data Lines These pins provide a multiplexed address and data bus. During the address phase of the bus cycle, address bits 0–15 are presented on the bus and can be latched using ALE or ADV#. During the data phase, 8- or 16-bit data is transferred. AD7:0 share package pins with P3.7:0. AD15:8 share package pins with P4.7:0.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). An external latch can use this signal to demultiplex address bits 0–15 from the address/data bus in multiplexed mode.
BHE#	O	Byte High Enable† During 16-bit bus cycles, this active-low output signal is asserted for word and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with address bit 0 (A0 for a demultiplexed address bus, AD0 for a multiplexed address/data bus), to determine which memory byte is being transferred over the system bus: **BHE# AD0 or A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only BHE# shares a package pin with WRH#. † Chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or as WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. When the bus-hold protocol is enabled (WSR.7 is set), the P2.3/BREQ# pin can function only as BREQ#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). The microcontroller can assert BREQ# at the same time as or after it asserts HLDA#. Once it is asserted, BREQ# remains asserted until HOLD# is deasserted. BREQ# shares a package pin with P2.3.
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (f). CLKOUT has a 50% duty cycle. CLKOUT shares a package pin with P2.7.
CS5:0#	O	Chip-select Lines 0–5 The active-low output CS*x*# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select *x* or chip select *x*+1 if remapping is enabled. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values. Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH. CS5:0# share package pins with P3.5:0.
EPA3:0	I/O	Event Processor Array (EPA) Capture/Compare Channels High-speed input/output signals for the EPA capture/compare channels. For high-speed PWM applications, the outputs of two EPA channels (either EPA0 and EPA1 or EPA2 and EPA3) can be remapped to produce a PWM waveform on a shared output pin. EPA3:0 share package pins with P1.3:0.
EPORT.3:0	I/O	Extended Addressing Port This is a standard 4-bit, bidirectional port. EPORT.3:0 share package pins with A19:16.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
EXTINT3:0	I	External Interrupts These programmable interrupts are controlled by the EXTINT_CON register. This register controls whether the interrupt is edge-triggered or level-sensitive and whether a rising edge/high level or falling edge/low level activates the interrupt. In standby and powerdown modes, asserting the EXTINT*x* signal causes the device to resume normal operation. The interrupt does not need to be enabled, but the pin must be configured as a special-function input. If the EXTINT*x* interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. EXTINT0 shares a package pin with P2.2, EXTINT1 shares a package pin with P2.4, EXTINT2 shares a package pin with P3.6, and EXTINT3 shares a package pin with P3.7.
HLDA#	O	Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#. When the bus-hold protocol is enabled (WSR.7 is set), the P2.6/HLDA# pin can function only as HLDA#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HLDA# shares a package pin with P2.6.
HOLD#	I	Bus Hold Request An external device uses this active-low input signal to request control of the bus. When the bus-hold protocol is enabled (WSR.7 is set), the P2.5/HOLD# pin can function only as HOLD#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HOLD# shares a package pin with P2.5.
INST	O	Instruction Fetch When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all interrupts except trap and unimplemented opcode. Assert NMI for greater than one state time to guarantee that it is recognized. If NMI is held high during and immediately following reset, the microcontroller will execute the NMI interrupt service routine when code execution begins. To prevent an inadvertent NMI interrupt vector, the first instruction (at F2080H) must clear the NMI pending interrupt bit. ANDB INT_PEND1, #7FH. During idle mode, a rising edge on NMI causes the microcontroller to exit idle mode and branch to the interrupt service routine.
ONCE	I	On-circuit Emulation Holding ONCE high during the rising edge of RESET# places the microcontroller into on-circuit emulation (ONCE) mode. This mode puts all pins, except READY, RESET#, ONCE, and NMI, into a high-impedance state, thereby isolating the microcontroller from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the microcontroller is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the microcontroller by pulling the RESET# signal low. To prevent inadvertent entry into ONCE mode, connect the ONCE pin to V_{SS}.
P1.7:0	I/O	Port 1 This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals. Port 1 shares package pins with the following signals: P1.0/EPA0, P1.1/EPA1, P1.2/EPA2, P1.3/EPA3, P1.4/T1CLK, P1.5/T1DIR, P1.6/T2CLK, and P1.7/T2DIR.
P2.7:0	I/O	Port 2 This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals. Port 2 shares package pins with the following signals: P2.0/TXD, P2.1/RXD, P2.2/EXTINT0, P2.3/BREQ#, P2.4/EXTINT1, P2.5/HOLD#, P2.6/HLDA#, and P2.7/CLKOUT.
P3.7:0	I/O	Port 3 This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals. Port 3 shares package pins with the following signals: P3.0/CS0#, P3.1/CS1#, P3.2/CS2#, P3.3/CS3#, P3.4/CS4#, P3.5/CS5#, P3.6/EXTINT2, and P3.7/EXTINT3.
P4.3:0	I/O	Port 4 Port 4 is a standard, 4-bit, bidirectional I/O port with high-current drive capability. Port 4 shares package pins with the following signals: P4.0/PWM0, P4.1/PWM1, and P4.2/PWM2. P4.3 has a dedicated package pin.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
PLLEN2:1	I	Phase-locked Loop 1 and 2 Enable These input pins enable the on-chip clock multiplier feature and select either the doubled or the quadrupled clock speed: **PLLEN2** **PLLEN1** **Mode** 0 0 1x mode; PLL disabled; f = F_{XTAL1} 0 1 2x mode; PLL enabled; f = $2F_{XTAL1}$ 1 0 Reserved † 1 1 4x mode; PLL enabled; f = $4F_{XTAL1}$ † **CAUTION:** This reserved combination causes the device to enter an unsupported test mode.
PWM2:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable. PWM2:0 share package pins with P4.2:0.
RD#	O	Read Read-signal output to external memory. RD# is asserted during external memory reads.
READY	I	Ready Input This active-high input can be used to insert wait states in addition to those programmed in chip configuration byte 0 (CCB0) and the bus control *x* register (BUSCON*x).* CCB0 is programmed with the minimum number of wait states (0, 5, 10, 15) for an external fetch of CCB1, and BUSCON*x* is programmed with the minimum number of wait states (0–15) for all external accesses to the address range assigned to the chip-select *x* channel. If the programmed number of wait states is greater than zero and READY is low when this programmed number of wait states is reached, additional wait states are added until READY is pulled high. If the programmed number of wait states is equal to zero, hold the READY pin high. Programming the number of wait states equal to zero and holding the READY pin low produces unpredictable results.
RESET#	I/O	Reset A level-sensitive reset input to, and an open-drain system reset output from, the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the microcontroller to reset and return to normal operating mode. If the phase-locked loop (PLL) clock circuitry is enabled, you must hold RESET# low for at least 2 ms to allow the PLL to stabilize before the internal CPU and peripheral clocks are enabled. After a reset, the first instruction fetch is from FF2080H.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if **either** of the following conditions are true. • the internal oscillator is the clock source • the phase-locked loop (PLL) circuitry is enabled (see PLLEN2:1 signal description) The capacitor causes a delay (at least 2 ms) that enables the oscillator and PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled. Refer to the "Special Operating Modes" chapter of the *80296SA Microcontroller User's Manual* for details on selecting the capacitor. The capacitor is not required if your application uses powerdown mode and if **both** of the following conditions are true. • an external clock input is the clock source • the phase-locked loop circuitry is disabled If your application does not use powerdown mode, leave this pin unconnected.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD shares a package pin with P2.1.
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. **and** External clock for the serial I/O baud-rate generator input (program selectable). T1CLK shares a package pin with P1.4.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. It is also used in conjunction with T2DIR for quadrature counting mode. T2CLK shares a package pin with P1.6.
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode. T1DIR shares a package pin with P1.5.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. It is also used in conjunction with T2CLK for quadrature counting mode. T2DIR shares a package pin with P1.7.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD shares a package pin with P2.0.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{SS}	GND	Digital Circuit Ground These pins supply ground for the digital circuitry. Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# shares a package pin with WRL#. † Chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRH#	O	Write High† During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# shares a package pin with BHE#. † Chip configuration registrer 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
WRL#	O	Write Low† During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# shares a package pin with WR#. † Chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator, internal phase-locked loop circuitry, and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.

5.0 ADDRESS MAP

Table 5. 80296SA Address Map

Hex Address	Description (Note 1, Note 2)	Addressing Modes for Data Accesses
FFFFFF FFF800	External device (memory or I/O) in 1-Mbyte mode (CCB1.1=0) A copy of internal code RAM in 64-Kbyte mode (CCB1.1=1)	Extended
FFF7FF FF2080	External program memory (Note 3)	Extended
FF207F FF2000	External special-purpose memory (CCBs and interrupt vectors)	Extended
FF1FFF FF0400	External device (memory or I/O) connected to address/data bus	Extended
FF03FF FF0000	Reserved for in-circuit emulators	—
FEFFFF 0F0000	Overlaid memory (reserved for future devices); locations *x*F0000–*x*F03FFH are reserved for in-circuit emulators	—
0EFFFF 010000	External device (memory or I/O) connected to address/data bus	Extended
00FFFF 00F800	Internal code RAM (code or data); can be windowed by WSR1. In 64-Kbyte mode, code RAM is identically mapped into page FFH.	Indirect, indexed, extended, windowed direct
00F7FF 00F000	External device (memory or I/O) connected to address/data bus; can be windowed by WSR1	Indirect, indexed, extended, windowed direct
00EFFF 002000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
001FFF 001F00	Internal peripheral special-function registers (SFRs); can be windowed by WSR or WSR1	Indirect, indexed, extended, windowed direct
001EFF 001C00	Reserved (future SFR expansion)	—
001BFF 000400	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
0003FF 000200	Reserved (future register file expansion)	—
0001FF 000100	Upper register file (general-purpose register RAM) can be windowed by WSR or WSR1	Indirect, indexed, extended windowed direct
0000FF 00001A	Lower register file (general-purpose register RAM)	Direct, indirect, indexed, extended
000019 000000	Lower register file (stack pointer and CPU SFRs)	Direct

NOTES:
1. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
2. The contents or functions of reserved locations may change in future device revisions, in which case a program that relies on one or more of these locations might not function properly.
3. External memory occupies the boot memory partition, FF2080–FF7FFH. After reset, the default chip-select line (CS0#) is active; the first instruction fetch is from FF2080H.

6.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... –60°C to +150°C
Supply Voltage with Respect to V_{SS} ..... –0.5 V to +7.0 V
Power Dissipation ..... 1.5 W

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
F_{XTAL1} (Input frequency for V_{CC} = 4.5 V – 5.5 V)
(Note 1, 2, 3) ..... 16 MHz to 50 MHz

NOTES:
1. This device is static and should operate below 1 Hz, but has been tested only down to 16 MHz.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. Assumes an external clock. The maximum frequency for an external crystal oscillator is 25 MHz.

NOTICE: This datasheet contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

***WARNING**: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 DC Characteristics

Table 6. DC Characteristics Over Specified Operating Conditions

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		90	150	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V Device in Reset
I_{IDLE}	Idle Mode Current		45	60	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

5. For all pins that were weakly pulled high during reset. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
6. Pin capacitance is not tested. This value is based on design simulations.

Table 6. DC Characteristics Over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{PD}	Powerdown Mode Current		20	50	µA	V_{CC} = 5.5 V (Note 2)
I_{STDBY}	Standby Mode		8	15	mA	V_{CC} = 5.5 V
I_{LI}	Input Leakage Current (Standard Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	–0.5		0.8	V	
V_{IL1}	Input Low Voltage XTAL1	–0.5		0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.2 V_{CC} +1		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (output configured as complementary) (Note 3, 4)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OL1}	Output Low Voltage on P4.3:0 (output configured as complementary) (Note 4)			0.45 0.6	V V	I_{OL} = 8 mA I_{OL} = 15 mA
V_{OL2}	Output Low Voltage in Reset on ALE, INST, and NMI			0.45	V	I_{OL} = 3 µA
V_{OL3}	Output Low Voltage in Reset on ONCE pin			0.45	V	I_{OL} = 30 µA
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45 1.5	V V V	I_{OL} = 100 µA I_{OL} = 700 µA I_{OL} = 3 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 4)	V_{CC} – 0.5 V_{CC} – 0.9 V_{CC} – 1.5			V V V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
V_{OH1}	Output High Voltage in Reset (Note 5)	V_{CC} – 0.7			V	I_{OH} = –3 µA

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

5. For all pins that were weakly pulled high during reset. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
6. Pin capacitance is not tested. This value is based on design simulations.

Table 6. DC Characteristics Over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
V_{OH2}	Output High Voltage on XTAL2	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –100 µA I_{OH} = –700 µA I_{OH} = –3 mA
V_{OH3}	Output High Voltage on READY in Reset	V_{CC} –1.1			V	
V_{TH+} – $V_{TH–}$	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 6)			10	pF	
R_{RST}	Reset Pull-up Resistor	50		150	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0 V

NOTES:

1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

5. For all pins that were weakly pulled high during reset. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
6. Pin capacitance is not tested. This value is based on design simulations.

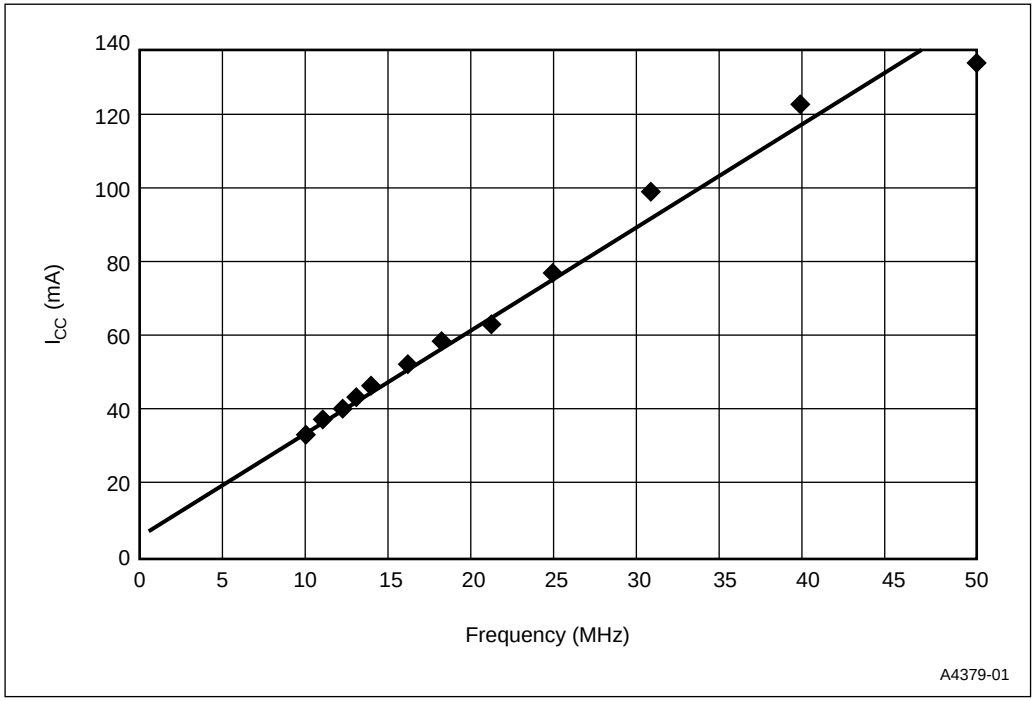


Figure 4. I_{cc} versus Frequency in Reset

6.2 AC Characteristics

6.2.1 RELATIONSHIP OF XTAL1 TO CLKOUT

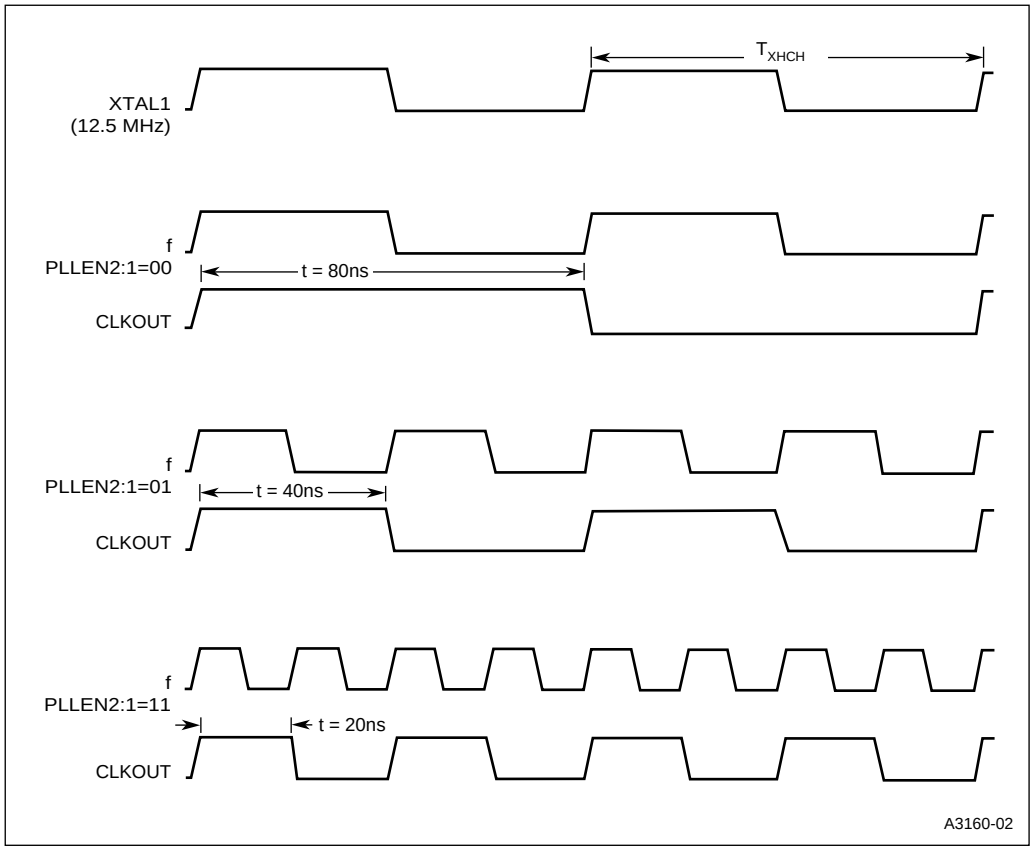


Figure 5. Effect of Clock Mode on CLKOUT

6.2.2 EXPLANATION OF AC SYMBOLS

Each AC timing symbol is two pairs of letters prefixed by “T” for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Table 7. AC Timing Symbol Definitions

Character	Signal(s)
A	AD15:0, A19:0
B	BHE#
BR	BREQ#
C	CLKOUT
D	AD15:0, AD7:0, RXD (SIO mode 0 input data)
H	HOLD#
HA	HLDA#
L	ALE
Q	AD15:0, AD7:0, RXD (SIO mode 0 output data)
R	RD#
S	CS*x*#
W	WR#, WRH#,WRL#
X	XTAL1, TXD (SIO clock)
Y	READY

Character	Condition
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating (low impedance)

6.2.3 AC CHARACTERISTICS — MULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 8. AC Characteristics the 80C296SA Will Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{XHCH}	XTAL1 Rising Edge to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{AVWL}	Address Valid to WR# Falling Edge	2t – 25		ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	–13	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	–15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{AVLL}	Address Valid to ALE Falling Edge	t – 15		ns
T_{LLAX}	Address Hold after ALE Falling Edge	1		ns
T_{LLRL}	ALE Falling Edge to RD# Falling Edge	3		ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	–10	20	ns
T_{RLRH}	RD# Low Period	2t – 25		ns (3)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 5	t + 15	ns (4)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Falling Edge to WR# Falling Edge	4		ns
T_{QVWH}	Data Stable to WR# Rising Edge	2t – 27		ns (3)
T_{CHWH}	CLKOUT High to WR# Rising Edge	–15	5	ns
T_{WLWH}	WR# Low Period	2t – 25		ns (3)

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 8. AC Characteristics the 80C296SA Will Meet, Multiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHQX}	Data Hold after WR# Rising Edge	t – 7		ns
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 15	t + 20	ns
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge	0		ns
T_{WHAX}	AD15:8 Hold after WR# Rising Edge	t – 4		ns (5)
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge	0		ns
T_{RHAX}	AD15:8 Hold after RD# Rising Edge	t – 4		ns (5)
T_{WHSH}	A19:16, CS# Hold after WR# Rising Edge	0		ns
T_{RHSH}	A19:16, CS# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 9. AC Characteristics the External Memory System Must Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	AD15:0 Valid to Input Data Valid		3t – 32	ns (1, 2)
T_{RLDV}	RD# Active to Input Data Valid		2t – 40	ns (1, 2)
T_{SLDV}	Chip Select Low to Data Valid		4t – 28	ns (1, 2)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t – 3	ns (2)
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{AVYV}	AD15:0 Valid to READY (Inactive) Setup		2t – 42	ns (3)
T_{CH1YX}	First READY Hold (active) after CLKOUT High	t – 4	2t – 21	ns (4, 5)
T_{CH2YX}	Non-first READY Hold (active) after CLKOUT High	0	2t – 21	ns (4)
T_{YLYH}	Non-READY (Inactive) Time	2t	No Upper Limit	ns

NOTES:
1. If using the READY signal to insert wait states, you must program at least one wait state in the BUSCON*x* register because the first falling edge of READY is not synchronized with a CLKOUT edge.
2. If using the BUSCON*x* register **without** the READY signal to insert wait states, add $2t \times n$, where n = number of wait states.
3. If using the BUSCON*x* register to insert wait states, add $2t \times (n–1)$, where n = number of wait states.
4. Exceeding the maximum specification causes additional wait states.
5. If you program two or more wait states in the BUSCON*x* register, the T_{CH1YX} minimum does **not** apply.

6.2.3.1 System Bus Timings, Multiplexed Bus

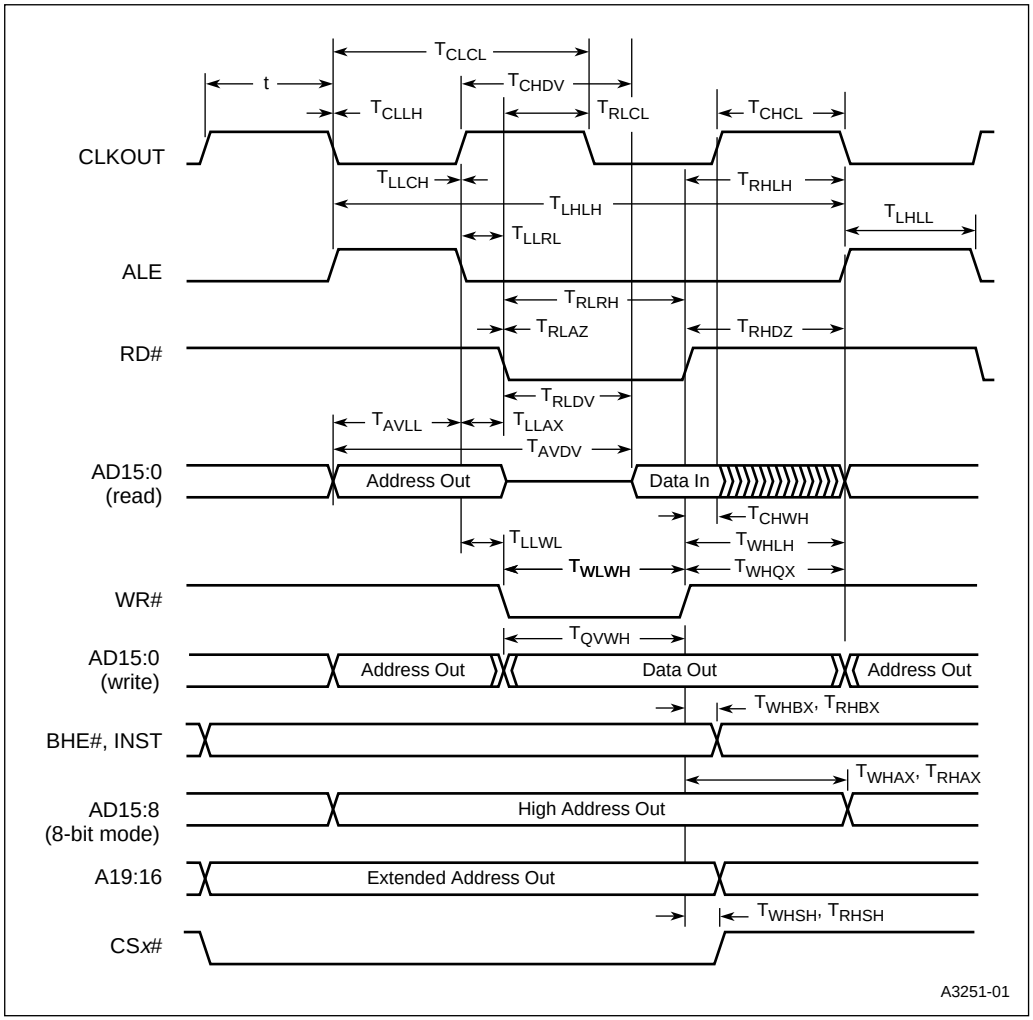


Figure 6. System Bus Timings, Multiplexed Bus Mode

6.2.3.2 READY Timing, Multiplexed Bus

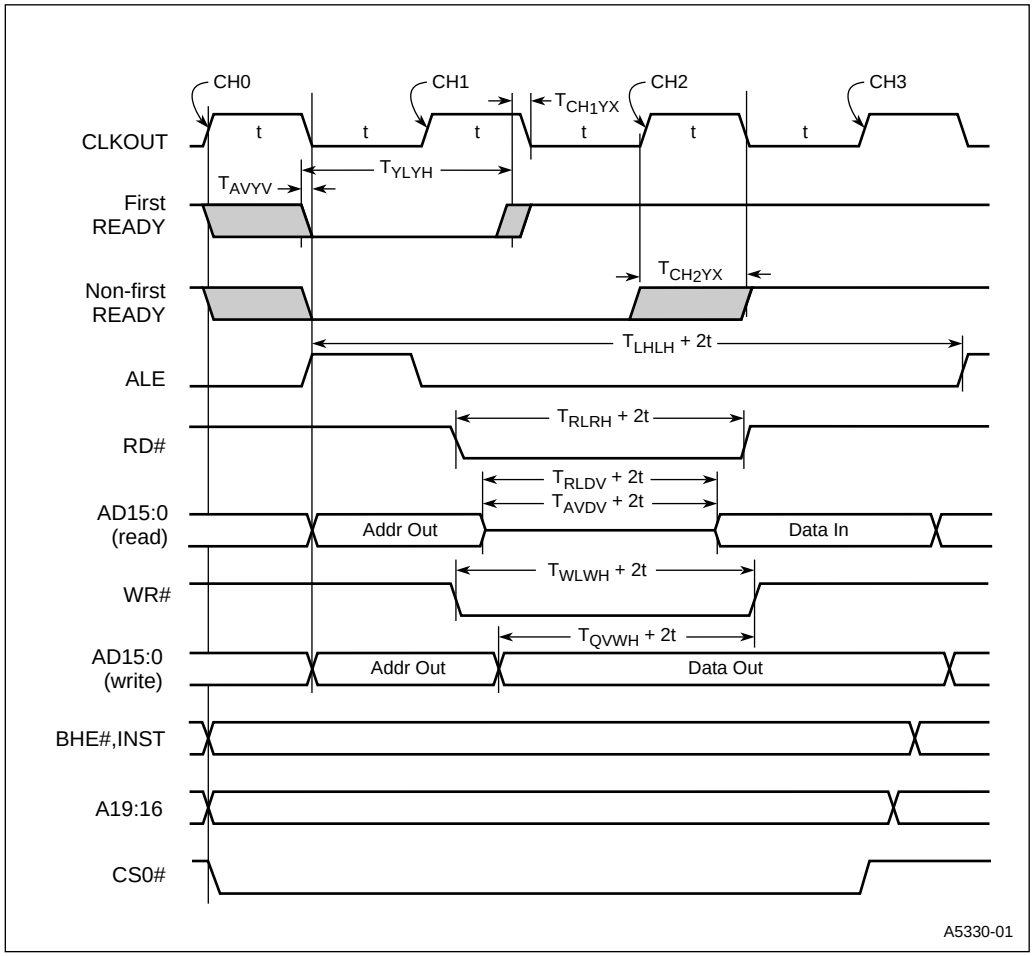


Figure 7. Example READY Timings at 50 MHz, Multiplexed Bus, BUSCON*x* = 1 Wait State

6.2.4 AC CHARACTERISTICS — DEMULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 10. AC Characteristics the 80C296SA Will Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{AVWL}	Address Valid to WR# Falling Edge	t – 10		ns
T_{AVRL}	Address Valid to RD# Falling Edge	t – 10		ns
T_{RHRL}	Read High to Next Read Low	t – 5		ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	–13	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	–15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3,4)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	–5	11	ns
T_{RLRH}	RD# Low Period	3t – 18		ns (3)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 4	t + 15	ns (4)
T_{WLCL}	WR# Low to CLKOUT Falling Edge	–8	9	ns
T_{QVWH}	Data Stable to WR# Rising Edge	3t – 10		ns (4)
T_{CHWH}	CLKOUT High to WR# Rising Edge	–11	10	ns
T_{WLWH}	WR# Low Period	3t – 10		ns (3)
T_{WHQX}	Data Hold after WR# Rising Edge	t – 5	t + 20	ns
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 5	t + 10	ns (3)

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If using either READY or BUSCON*x* to insert wait states, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.

Table 10. AC Characteristics the 80C296SA Will Meet, Demultiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge	0		ns
T_{WHAX}	A19:0, CS*x*# Hold after WR# Rising Edge	0		ns
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge	0		ns
T_{RHAX}	A19:0, CS*x*# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If using either READY or BUSCON*x* to insert wait states, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.

Table 11. AC Characteristics the External Memory System Must Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	A19:0 Valid to Input Data Valid		4t – 28	ns (1, 2, 3)
T_{RLDV}	RD# Active to Input Data Valid		3t – 25	ns (1, 2)
T_{SLDV}	Chip Select Low to Data Valid		4t – 28	ns (1, 2, 3)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t	ns (2, 3)
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{AVYV}	A19:0 Valid to READY Setup		3t – 45	ns (4)
T_{CH1YX}	First READY Hold (active) after CLKOUT High	t – 4	2t – 21	ns (5, 6)
T_{CH2YX}	Non-first READY Hold (active) after CLKOUT High	0	2t – 21	ns (5)
T_{YLYH}	Non READY (inactive) Time	2t	No Upper Limit	ns

NOTES:
1. If using the READY signal to insert wait states, you must program at least one wait state in the BUSCON*x* register because the first falling edge of READY is not synchronized with a CLKOUT edge.
2. If using the BUSCON*x* register **without** the READY signal to insert wait states, add $2t \times n$, where n = number of wait states.
3. If CS*x*# changes or if a write cycle follows a read cycle, add 2t (1 state).
4. If using the BUSCON*x* register to insert wait states, add $(2t \times n–1)$, where n = number of wait states.
5. Exceeding the maximum specification causes additional wait states.
6. If you program two or more wait states in the BUSCON*x* register, the T_{CH1YX} minimum does not apply.

6.2.4.1 System Bus Timings, Demultiplexed Bus

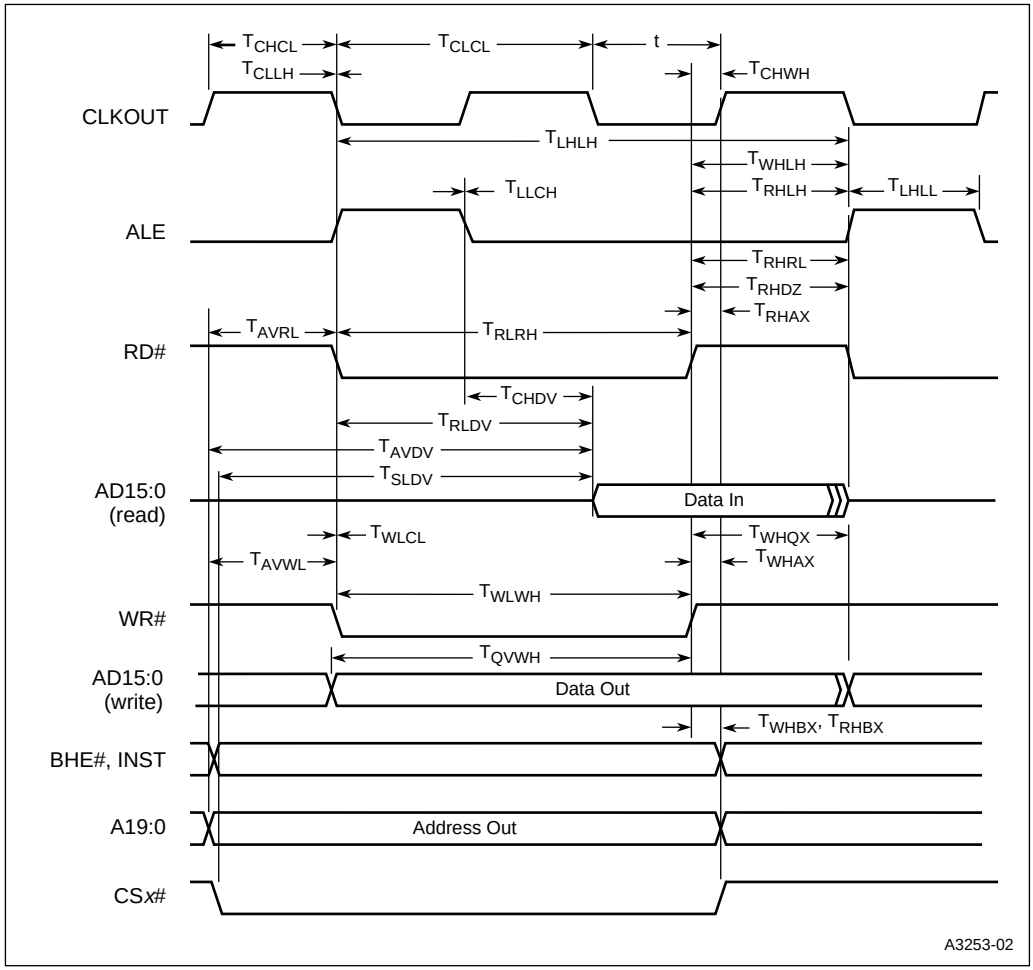


Figure 8. System Bus Timings, Demultiplexed Bus Mode

6.2.4.2 READY Timing, Demultiplexed Bus

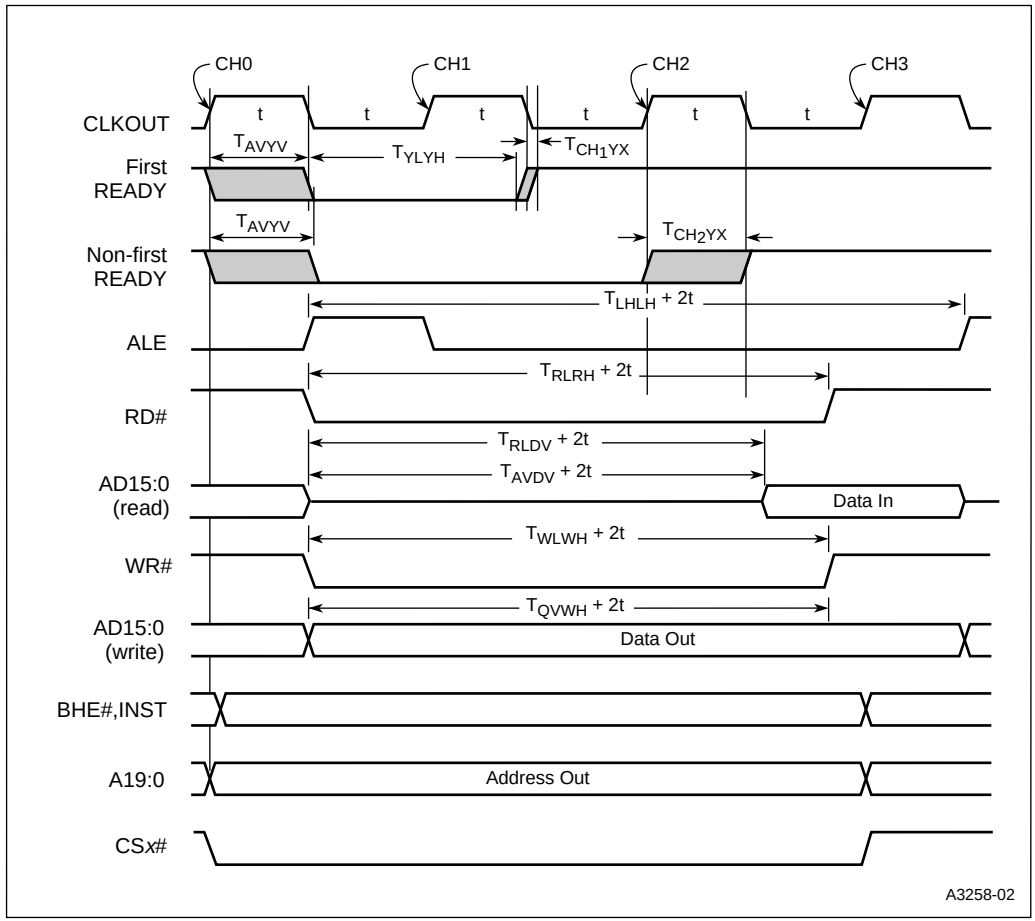


Figure 9. Example READY Timings at 50 MHz, Demultiplexed Bus, BUSCON*x* = 1 Wait State

6.2.4.3 80296SA Deferred Bus Timing Mode

The deferred bus cycle mode is designed to reduce bus contention when using the 80296SA in demultiplexed mode with slow memory devices. Unlike the 8XC196NU, in which this bus mode has to be enabled through the CCR to take advantage of the feature, the 80296SA **automatically invokes this mode** whenever the appropriate conditions occur. In the deferred mode, a delay of the WR# signal and the next bus cycle will occur in the first bus cycle following a chip-select change and in the first write cycle following a read cycle. This mode will work in parallel with wait states. Refer to Figure 11 to determine which control signals are affected.

Cycle 1 is a normal 4t read cycle. Cycle 2 is a write cycle that follows a read cycle, so a 2t delay of the next bus cycle is inserted. Notice that the chip-select change at the beginning of cycle 2 did not cause a double delay (4t). The chip-select change in cycle 3, a read cycle, causes a 2t delay.

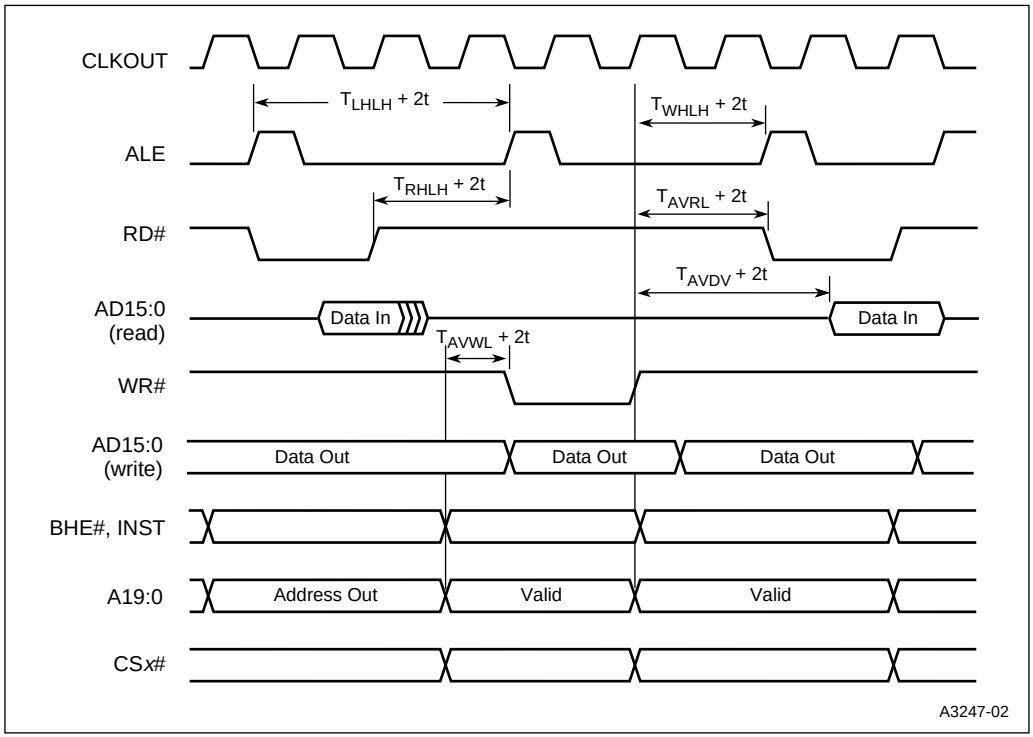


Figure 10. Deferred Bus Mode Timing Diagram

6.2.5 HOLD#, HLDA# TIMINGS

Table 12. HOLD#, HLDA# Timings

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD# Setup time (to guarantee recognition at next clock)	30		ns
T_{CLHAL}	CLKOUT Low to HLDA# Low	–15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	–15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	–25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	–25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	–20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	–20		ns

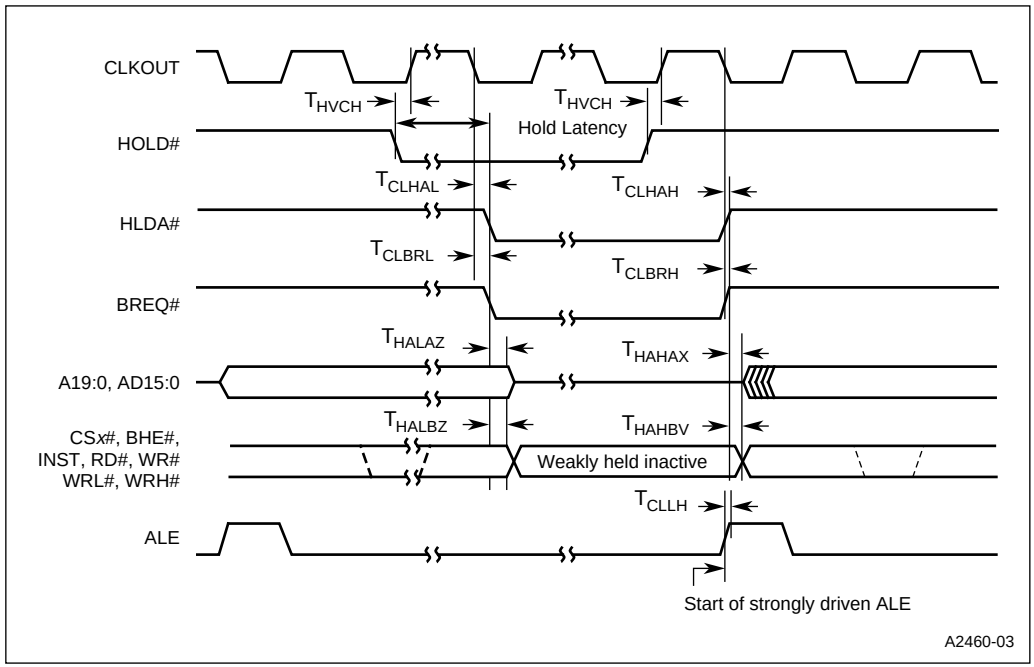


Figure 11. HOLD#, HLDA# Timing Diagram

6.2.6 AC CHARACTERISTICS — SERIAL PORT, SYNCHRONOUS MODE 0

Table 13. Serial Port Timing — Synchronous Mode 0

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock period† SP_BAUD ≥ *x*002H SP_BAUD = *x*001H	 6t 4t		 ns ns
T_{XLXH}	Serial Port Clock falling edge to rising edge † SP_BAUD ≥ *x*002H SP_BAUD = *x*001H	 4t – 15 2t – 15	 4t + 15 2t + 15	 ns ns
T_{QVXH}	Output data setup to clock high (see Note) SP_BAUD ≥ *x*002H SP_BAUD = *x*001H	 4t – 15 2t – 15	 4t + 15 2t + 15	 ns
T_{XHQX}	Output data hold after clock high	2t – 20		ns
T_{XHQV}	Next output data valid after clock high		2t + 20	ns
T_{DVXH}	Input data setup to clock high (see Note) SP_BAUD ≥ *x*002H SP_BAUD = *x*001H	 2t + 10 t + 10		 ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		2t + 15	ns

† The minimum baud-rate (SP_BAUD) register value is x002H for receptions and x001H for transmissions.

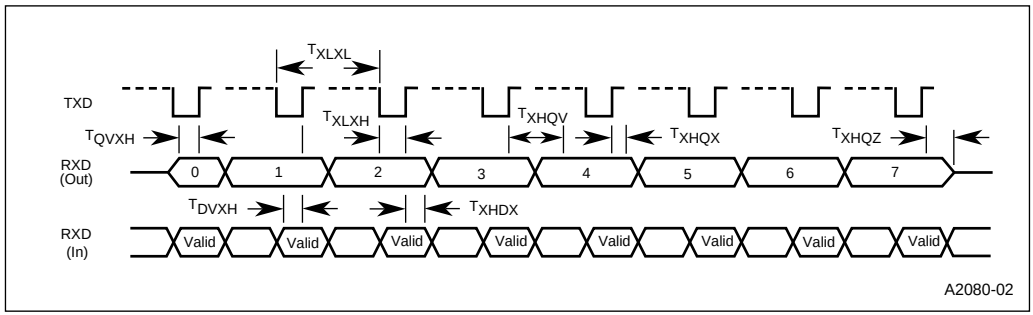


Figure 12. Serial Port Waveform — Synchronous Mode 0

6.2.7 EXTERNAL CLOCK DRIVE

Table 14. External Clock Drive

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	External Input Frequency ($1/T_{XLXL}$), PLL disabled	16	50†	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 2x mode	8	25	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 4x mode	8	12.5	MHz
T_{XTAL1}	Oscillator Period (T_{XLXL}), PLL disabled	20	62.5	ns
	Oscillator Period (T_{XLXL}), PLL in 2x mode	40	125	ns
	Oscillator Period (T_{XLXL}), PLL in 4x mode	80	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

† Assumes an external clock; the maximum input frequency for an external crystal oscillator is 25 MHz.

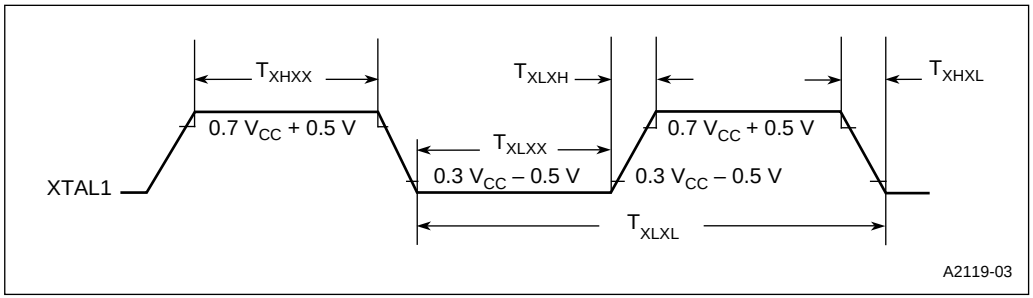
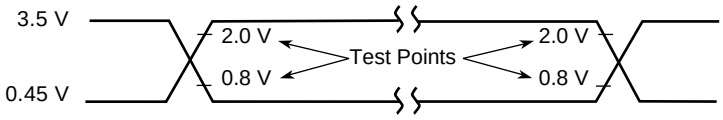


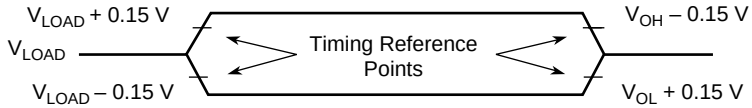
Figure 13. External Clock Drive Waveforms



Note:
AC testing inputs are driven at 3.5 V for a logic " 1" and 0.45 V for a logic " 0" . Timing measurements are made at 2.0 V for a logic " 1" and 0.8 V for a logic " 0".

A2120-04

Figure 14. AC Testing Input and Output Waveforms During 5.0 Volt Testing



Note:
For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2121-03

Figure 15. Float Waveforms During 5.0 Volt Testing

7.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 15. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin QFP	50°C/W	16°C/W

8.0 80296SA ERRATA

The 80296SA may contain design defects or errors known as errata. Characterized errata that may cause the 80296SA's behavior to deviate from published specifications are documented in a specification update. Specification updates can be obtained from your local Intel sales office or from the World Wide Web (*www.intel.com*).

9.0 DATASHEET REVISION HISTORY

This datasheet is valid for devices with an "A" at the end of the topside tracking number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This is the -003 version of the datasheet. The following changes were made in this version:

1. All references to SQFP package were deleted.
2. Reference to ROM option was removed from Table 1.
3. The speed designation for 40 MHz was changed from "no mark" to "40" in Table 1.
4. The T_{RXDX} specification was changed to 0 ns (from 2 ns) in Table 11 and Table 13.
5. The T_{CHYX} specification was replaced by T_{CH1YX} and T_{CH2YX}.
6. The READY timing diagrams (Figures 8 and 10) were replaced by examples that reflect the new T_{CH1YX} and T_{CH2YX} specifications.

This is the -002 version of the datasheet. The following changes were made in this version:

1. The "Intel Confidential" designation was removed for publication.
2. A heading was added for Section 1.0, "Product Overview," and the remaining sections were renumbered.
3. The errata list was replaced with a reference to the specification update document.

The following changes were made in the -001 version of the datasheet:

1. Throughout the datasheet, the product name was changed to read "80296SA" instead of "80C296SA."
2. The feature list was clarified.
3. A table of contents was added.
4. The block diagram was changed.
5. Several sections were rearranged and section numbers were assigned. "Thermal Characteristics" was moved to Section 7.0; a section heading was added for "Nomenclature Overview," Section 2.0; a section heading was added for "Address Map" and it was moved to Section 5.0; a section heading was added for "Pinout," and it was moved to Section 3.0; the section heading "Pin Descriptions" was changed to "Signals," Section 4.0. The remaining sections were assigned section numbers: "Electrical Characteris-

tics" is Section 6.0; "Errata" is Section 8.0, and "Datasheet Revision History" is Section 9.0.

6. Table 2 was changed to Table 1 and the "process information" was corrected to show that "no mark" signifies a CHMOS process.
7. Table 3 was changed to Table 7 and several clarifications were made.
8. Figure 3 was changed to correct the product name. Pin assignments did **not** change.
9. Table 4 was changed to Table 2 and pin 3 was changed from "no connection" to "tie to V_{CC}."
10. Figure 4 was changed to correct the product name. Pin assignments did **not** change.
11. Figure 5, "I_{CC} versus Frequency in Reset," was added. Remaining figure numbers were incremented.
12. Table 6 was changed to Table 4 and a note for handling the "no connection" pins was added.
13. Table 8 was changed to Table 6. The descriptions of BREQ#, HLDA#, and HOLD# were changed to reflect their operation during hold. The description of the ONCE signal was changed to reflect the correct states of READY, RESET#, and NMI during ONCE mode. The description of PLLEN2:1 was changed to show the correct pin states to achieve each phase-locked loop (PLL) clock multiplier mode. The descriptions of RPD and RESET# were changed to reflect system requirements when using the PLL.
14. Two notes were added to clarify the "Operating Conditions" in the "Electrical Characteristics" section.
15. Table 9 was changed to Table 8, the notes were re-ordered, and the following specifications were changed:
    - I_{CC} max was changed to 150 mA (from 120 mA).
    - V_{OH} min was changed to V_{CC}–0.5 V (from V_{CC}–0.3 V) at I_{OH} = –200µA.
    - V_{OH} min was changed to V_{CC}–0.9 V (from V_{CC}–0.7V) at I_{OH} = –3.2 mA.
    - Test condition for V_{OL1} max = 0.45 V was changed to I_{OL} = 8 mA (from I_{OL} = 10 mA).
    - R_{RST} min and max were changed to 50 kΩ and 150 kΩ (from 9 kΩ and 95 kΩ).
    - V_{OH3} min specification was added.
16. Table 10 was divided into two tables: timing specifications that the microcontroller will meet (Table 10) and those that the external memory system must meet (Table 11). Note 7 was deleted and the remaining notes were re-ordered. The following specifications were changed or added in Table 10:
    - F_{XTAL1} min for the PLL in 4x mode was changed to 8 MHz (from 4 MHz); a clarifying note was added.
    - T_{XHCH} min was changed to 3 ns (from TBD).
    - T_{LLAX} min was changed to 1 ns (from TBD).
    - T_{LLRL} min was changed to 3 ns (from TBD)
    - T_{RHAX} min was changed to t – 4 ns (from t).
    - T_{AVWL} min (2t – 25) was added to Table 10.
    - T_{SLDV} min (4t – 28) was added to Table 11.
17. Table 11 was divided into two tables: timing specifications that the microcontroller will meet (Table 12) and those that the external memory system must meet (Table 13). Note 7 was deleted and the remaining notes were re-ordered. The following specifications were changed:
    - F_{XTAL1} min for the PLL in 4x mode was changed to 8 MHz (from 4 MHz); a clarifying note was added.
    - T_{WHQX} min was changed to t – 5 ns (from t – 2 ns).
18. Figure 6 was changed to show the correct PLLEN2:1 values to select the 2x clock multiplier mode.
19. Table 13 was changed to Table 15 and a note was added.
20. Table 14 was changed to Table 16, $1/T_{XLXL}$ specifications for each phase-locked loop (PLL) mode were added, and Note 2 was deleted.

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