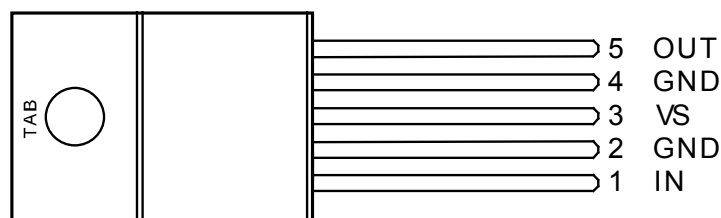
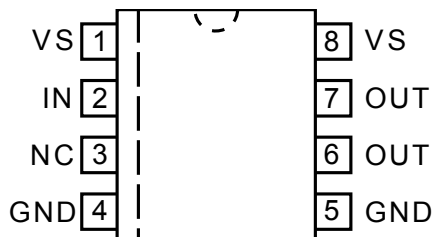


Ordering Information

Part Number		Temperature Range	Package	Configuration
Standard	Pb-Free			
-	MIC4451YN	-40°C to +85°C	8-Pin Plastic DIP	Inverting
MIC4451BM	MIC4451YM	-40°C to +85°C	8- Pin SOIC	Inverting
-	MIC4451ZT	0°C to +70°C	5- Pin TO-220	Inverting
-	MIC4452YN	-40°C to +85°C	8- Pin Plastic DIP	Non-Inverting
MIC4452BM	MIC4452YM	-40°C to +85°C	8- Pin SOIC	Non-Inverting
-	MIC4452ZT	0°C to +70°C	5- Pin TO-220	Non-Inverting
-	MIC4452VM	-40°C to +125°C	8- Pin SOIC	Non-Inverting

Pin Configurations



Pin Description

Pin Number T0-220-5	Pin Number DIP, SOIC	Pin Name	Pin Function
1	2	IN	Control Input.
2, 4	4, 5	GND	Ground: Duplicate Pins must be externally connected together.
3, TAB	1, 8	V _s	Supply Input: Duplicate pins must be externally connected together.
5	6, 7	OUT	Output: Duplicate pins must be externally connected together.
	3	NC	Not Connected.

Absolute Maximum Ratings^(1, 2)

Supply Voltage	20V
Input Voltage	$V_S + 0.3V$ to GND $-5V$
Input Current ($V_{IN} > V_S$)	5mA
Power Dissipation, $T_{AMBIENT} \leq 25^\circ C$	
PDIP	960mW
SOIC	1040mW
5-Pin TO-220	2W
Power Dissipation, $T_{CASE} \leq 25^\circ C$	
5-Pin TO-220	12.5W
Derating Factors (to Ambient)	
PDIP	7.7mW/ $^\circ C$
SOIC	8.3mW/ $^\circ C$
5-Pin TO-220	17mW/ $^\circ C$
Storage Temperature	$-65^\circ C$ to $+150^\circ C$
Lead Temperature(10s)	300 $^\circ C$

Operating Ratings

Operating Temperature (Chip)	150 $^\circ C$
Operating Temperature (Ambient)	
Z Version	0 $^\circ C$ to $+70^\circ C$
Y Version	$-40^\circ C$ to $+85^\circ C$
V Version	$-40^\circ C$ to $+125^\circ C$
Thermal Impedances (To Case)	
5-Pin TO-220(θJC)	10 $^\circ C/W$

Electrical Characteristics⁽³⁾

($T_A = 25^\circ C$, with $4.5V \leq V_S \leq 18V$ unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Input						
V_{IH}	Logic 1 Input Voltage		2.4	1.3		V
V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
V_{IN}	Input Voltage Range		-5		$V_S + .3$	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA
Output						
V_{OH}	High Output Voltage	See Figure 1	$V_S - .025$			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output High	$I_{OUT} = 10mA, V_S = 18V$		0.6	1.5	Ω
R_O	Output Resistance, Output Low	$I_{OUT} = 10mA, V_S = 18V$		0.8	1.5	Ω
I_{PK}	Peak Output Current	$V_S = 18V$ (See Figure 6)		12		A
I_{DC}	Continuous Output Current		2			A
I_R	Latch-up Protection Withstand Reverse Current	Duty Cycle $\leq 2\%$ $t \leq 300\mu s$	>1500			mA
Switching Time⁽³⁾						
t_R	Rise Time	Test Figure 1, $C_L = 15,000pF$		20	40	ns
t_F	Fall Time	Test Figure 1, $C_L = 15,000pF$		24	50	ns
t_{D1}	Delay Time	Test Figure 1		25	50	ns
t_{D2}	Delay Time	Test Figure 1		40	60	ns
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ $V_{IN} = 0V$		0.4 80	1.5 150	mA μA
V_S	Operating Input Voltage		4.5			V

Electrical Characteristics

(Over operating temperature range with $4.5V \leq V_S \leq 18V$ unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Input						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
V_{IN}	Input Voltage Range		-5		$V_S + .3$	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA
Output						
V_{OH}	High Output Voltage	See Figure 1	$V_S - .025$			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output High	$I_{OUT} = 10mA, V_S = 18V$			2.2	Ω
R_O	Output Resistance, Output Low	$I_{OUT} = 10mA, V_S = 18V$			2.2	Ω
Switching Time ⁽³⁾						
t_R	Rise Time	Test Figure 1, $C_L = 15,000pF$			50	ns
t_F	Fall Time	Test Figure 1, $C_L = 15,000pF$			60	ns
t_{D1}	Delay Time	Test Figure 1			65	ns
t_{D2}	Delay Time	Test Figure 1			80	ns
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ $V_{IN} = 0V$			3 0.4	mA
V_S	Operating Input Voltage		4.5		18	V

Notes:

1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
3. Specification for packaged product only.

Test Circuits

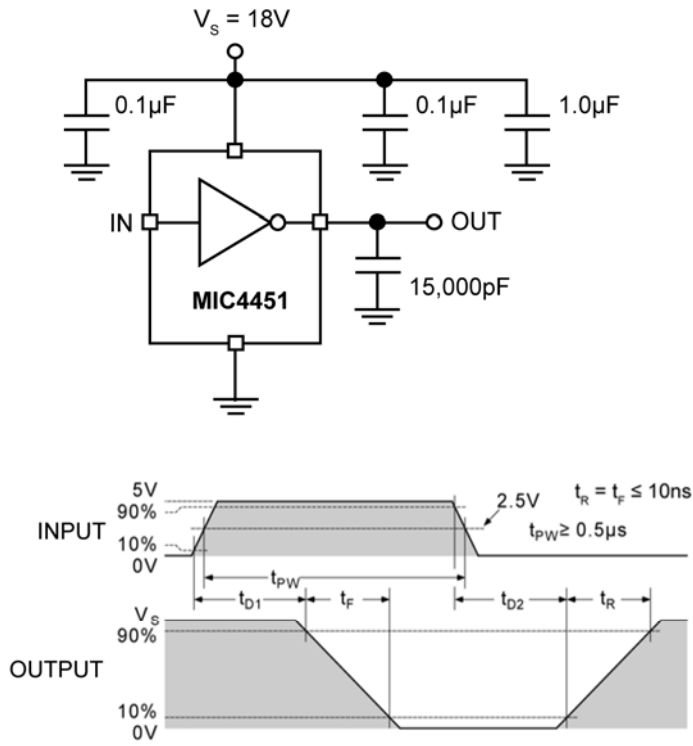


Figure 1. Inverting Driver Switching Time

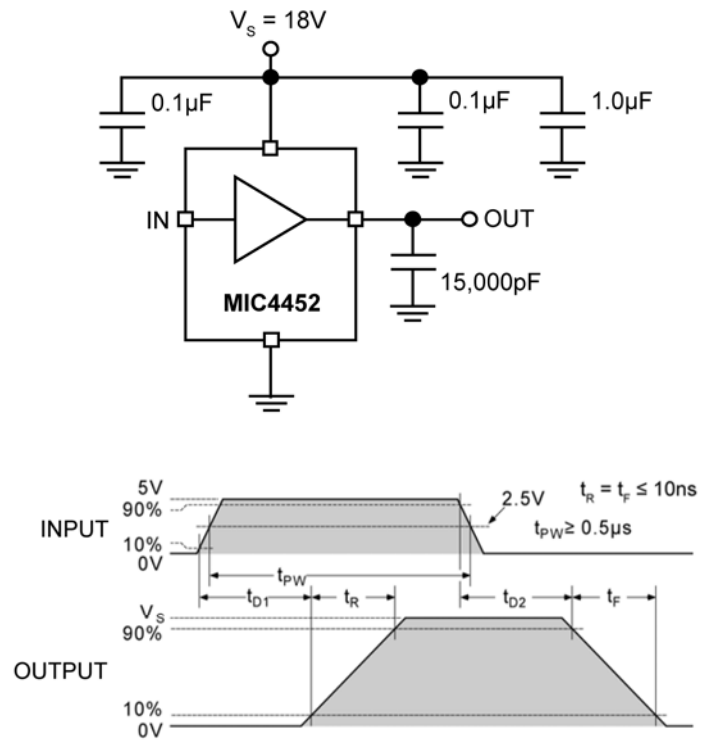


Figure 2. Noninverting Driver Switching Time

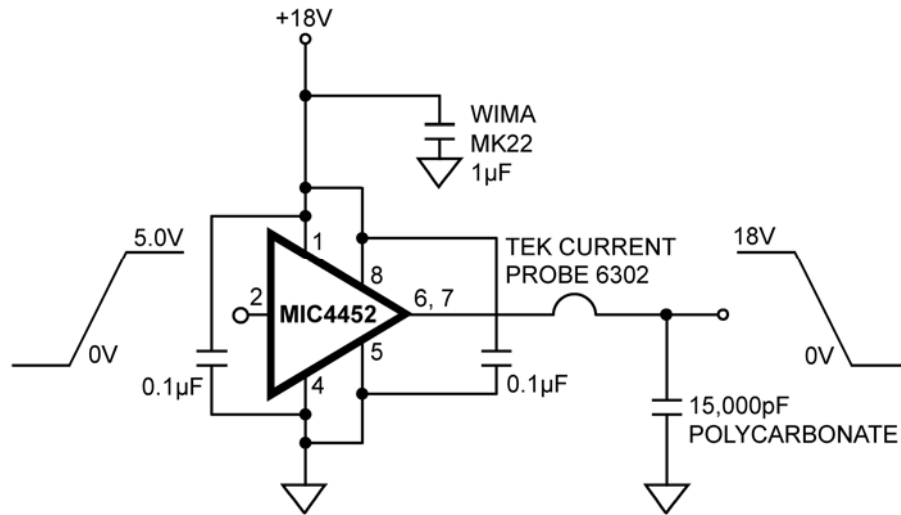
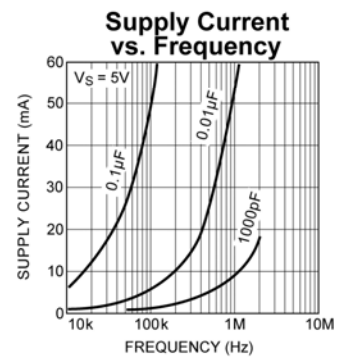
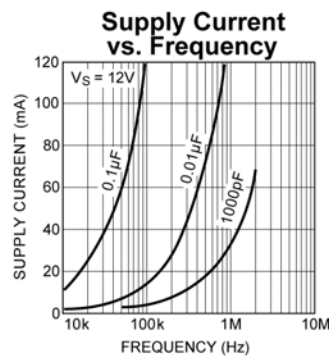
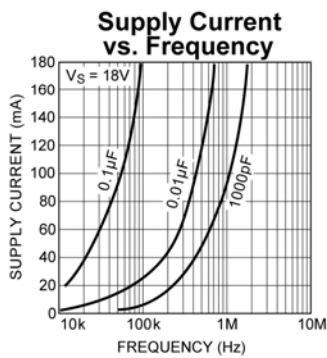
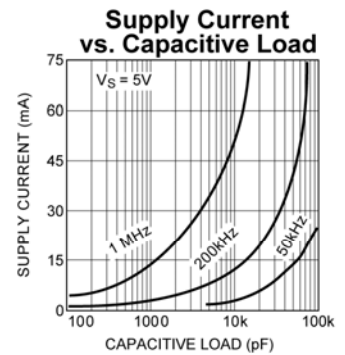
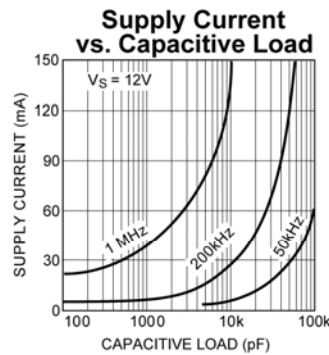
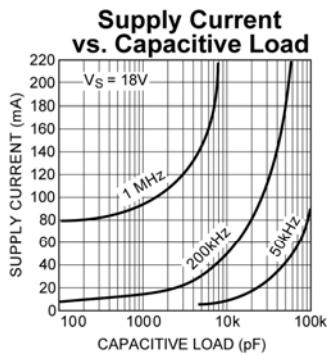
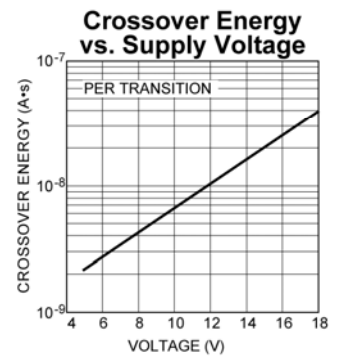
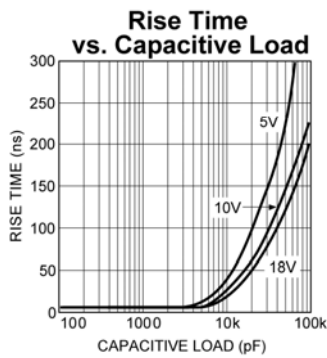
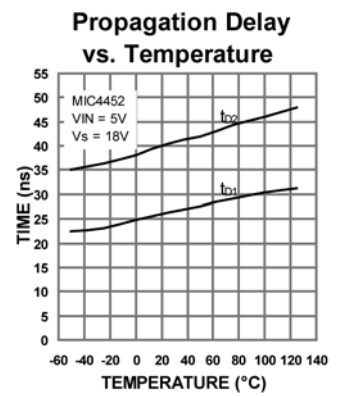
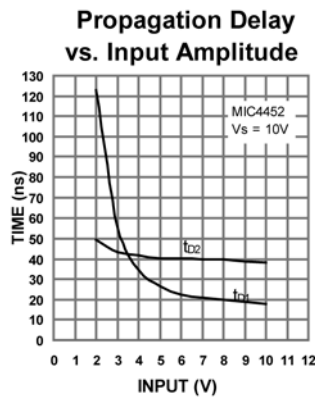
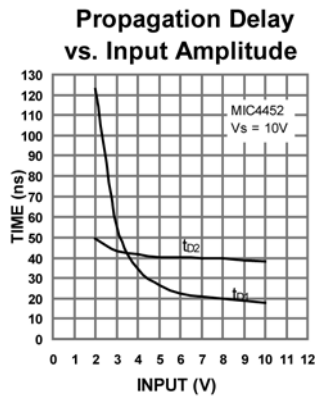
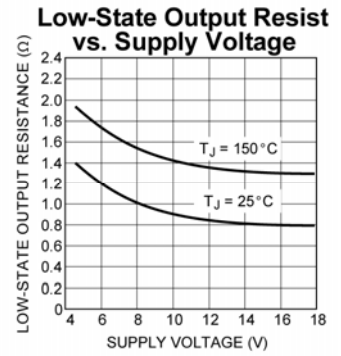
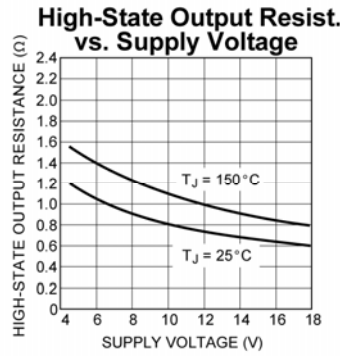
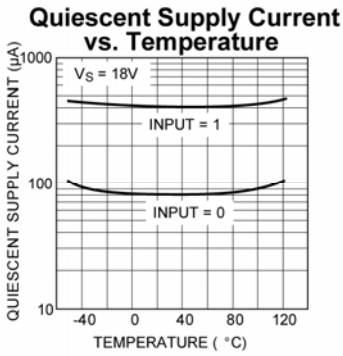


Figure 3. Peak Output Current Test Circuit

Typical Characteristics



Typical Characteristics Curves (Continued)



Applications Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 10,000pF load to 18V in 50ns requires 3.6A.

The MIC4451/4452 has double bonding on the supply pins, the ground pins and output pins. This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1 μ F low ESR film capacitor in parallel with two 0.1 μ F low ESR ceramic capacitors, (such as AVX RAM GUARD[®]), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4451/4452 demands careful PC board layout for best performance. Since the MIC4451 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4451 input structure includes 200mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 4 shows the feedback effect in detail. As the MIC4451 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05 Ω of PC trace resistance can produce hundreds of millivolts at the MIC4451 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4451 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4451 GND pins should, however, still be connected to power ground.

Input Stage

The input voltage level of the MIC4451 changes the quiescent supply current. The N channel MOSFET input stage transistor drives a 320 μ A current source load. With a logic "1" input, the maximum quiescent supply current is 400 μ A. Logic "0" input level signals reduce quiescent current to 80 μ A typical.

The MIC4451/4452 input is designed to provide 200mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the full temperature and operating supply voltage ranges. Input current is less than $\pm 10\mu$ A.

The MIC4451 can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38C42, and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the MIC4451/4452, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the V_S supply, however, current will flow into the input lead. The input currents can be as high as 30mA p-p (6.4mA_{RMS}) with the input. No damage will occur to MIC4451/4452 however, and it will not latch.

The input appears as a 7pF capacitance and does not change even if the input is driven from an AC source. While the device will operate and no damage will occur up to 25V below the negative rail, input current will increase up to 1mA/V due to the clamping action of the input, ESD diode, and 1k Ω resistor.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4451/4452 on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

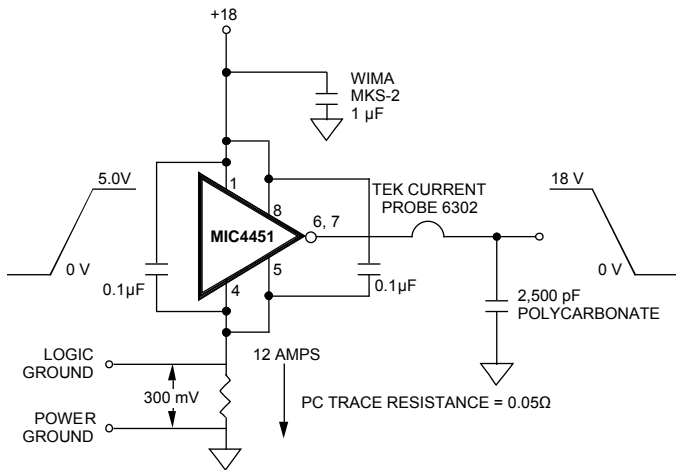


Figure 4. Switching Time Degradation Due to Negative Feedback

The supply current vs. frequency and supply current vs capacitive load characteristic curves aid in determining power dissipation calculations. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 10,000pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin plastic DIP package, from the data sheet, is 130°C/W. In a 25°C ambient, then, using a maximum junction temperature of 125°C, this package will dissipate 960mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load

R_O = the output resistance of the driver when the output is high, at the power supply voltage used. (See data sheet)

D = fraction of time the load is conducting (duty cycle)

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2 C V^2$$

VS	Max. Frequency
18V	220kHz
15V	300kHz
10V	640kHz
5V	2MHz

Table 1: MIC4451 Maximum Operating Frequency

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = f C (V_S)^2$$

where:

f = Operating Frequency

C = Load Capacitance

V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

$$P_{L2} = I V_D (1 - D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L :

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q , as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of $\leq 0.2\text{mA}$; a logic high will result in a current drain of $\leq 3.0\text{mA}$. Quiescent power can therefore be found from:

$$P_Q = V_S [D I_H + (1 - D) I_L]$$

where:

I_H = quiescent current with input high

I_L = quiescent current with input low

D = fraction of time input is high (duty cycle)

V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = 2 f V_S (A \times s)$$

where ($A \times s$) is a time-current factor derived from the typical characteristic curve "Crossover Energy vs. Supply Voltage." Total power (P_D) then, as previously described is:

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

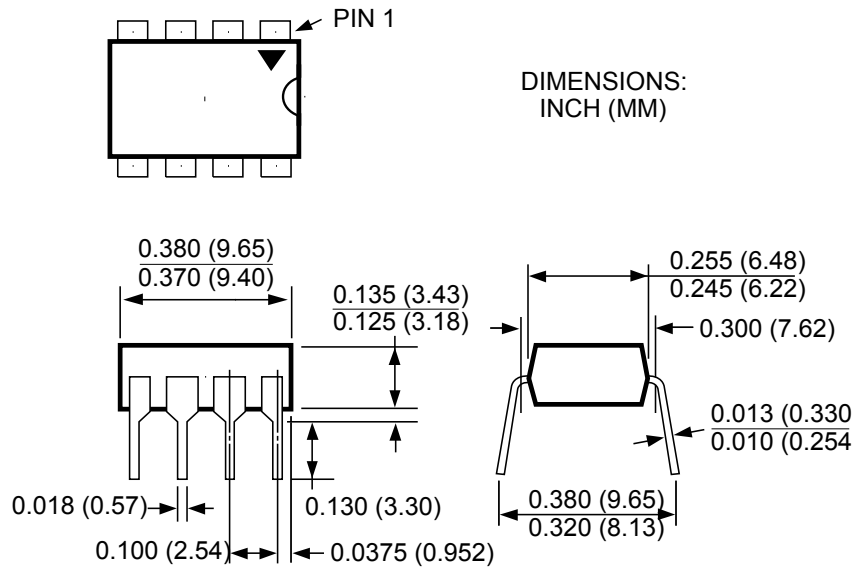
P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in watts.

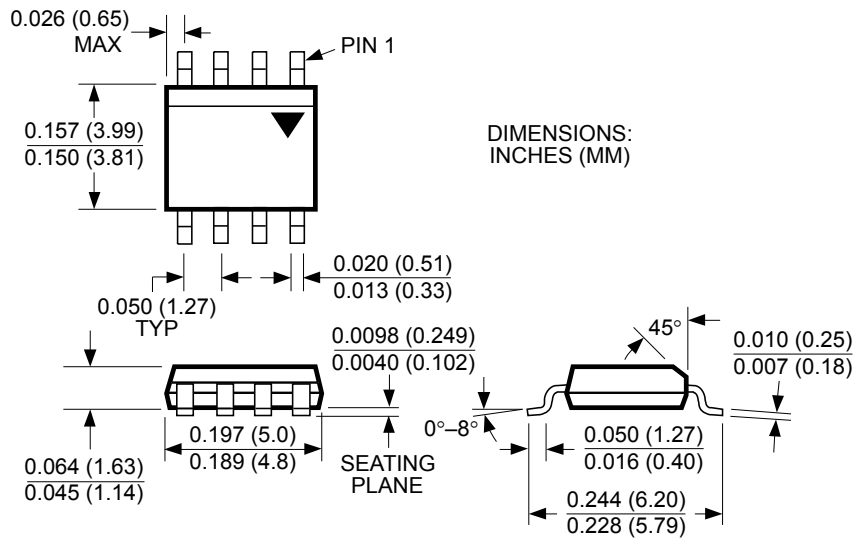
R_O = Output resistance of a driver in Ω s.

V_S = Power supply voltage to the IC in volts.

Package Information

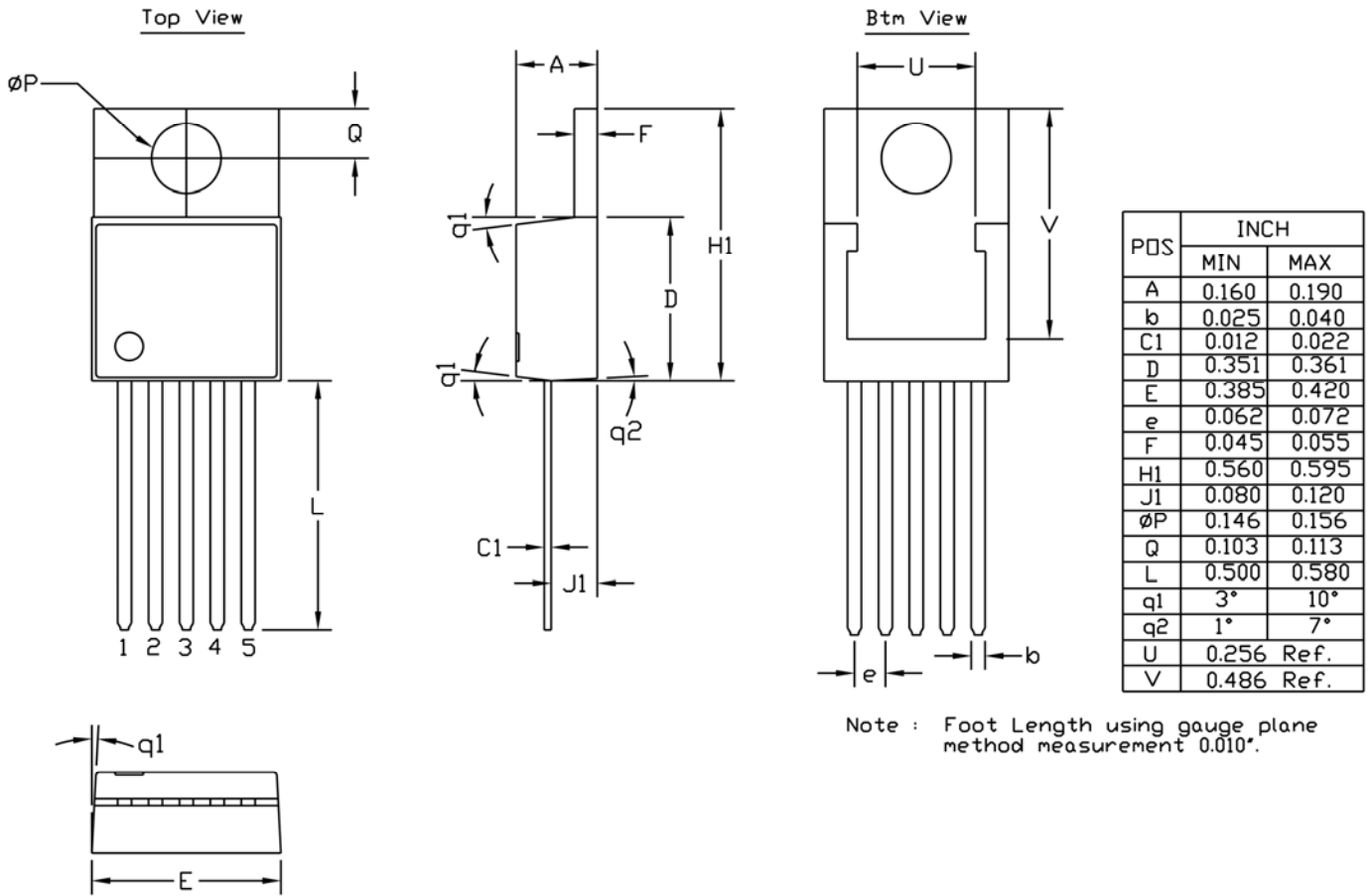


8-Pin Plastic DIP (N)



8-Pin SOIC (M)

Package Information (Continued)



5-Pin TO-220 (T)

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