

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers including microcontrollers.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- Good immunity to false turn-on by  $dV/dt$
- High commutation capability with sensitive gate
- High voltage capability
- Isolated mounting base package
- Planar technology for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

## 3. Applications

- General purpose motor controls
- Large and small appliances (White Goods)
- Loads such as contactors, circuit breakers, valves, dispensers and door locks
- Lower-power highly inductive, resistive and safety loads

## 4. Quick reference data

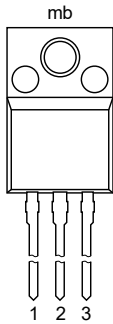
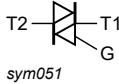
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 110\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	2	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	14	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	-	15.4	A
$T_j$	junction temperature		-	-	125	°C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	0.5	-	10	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ \text{ G-}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	0.5	-	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- \text{ G-}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 7}$	0.5	-	10	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	12	mA
$V_T$	on-state voltage	$I_T = 3\text{ A}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 10}$	-	1.63	2	V
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{exponential waveform}; R_{GT1(\text{ext})} = 220\text{ }\Omega$	-	500	-	V/ $\mu\text{s}$
$di_{\text{com}}/dt$	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(\text{RMS})} = 2\text{ A}; dV_{\text{com}}/dt = 20\text{ V}/\mu\text{s}; (\text{snubberless condition}); \text{gate open circuit}$	2	-	-	A/ms
		$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(\text{RMS})} = 2\text{ A}; dV_{\text{com}}/dt = 10\text{ V}/\mu\text{s}; \text{gate open circuit}$	2.3	-	-	A/ms

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220F (SOT186A)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

## 6. Ordering information

Table 3. Ordering information

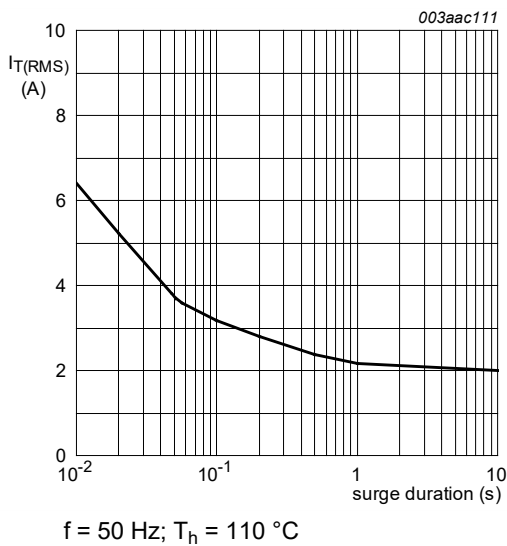
Type number	Package		Version
	Name	Description	
BTA202X-800E	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

## 7. Limiting values

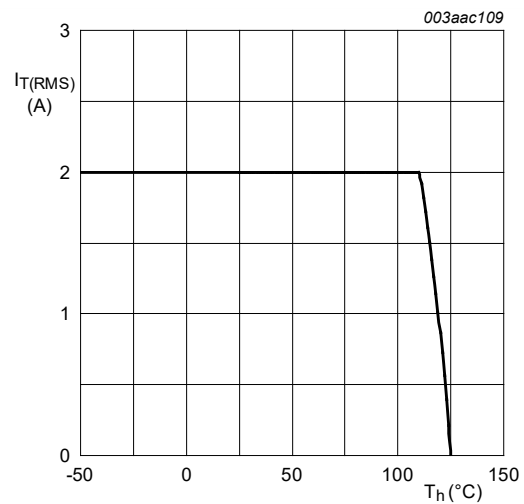
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 110\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	2	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	14	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 16.7\text{ ms}$	-	15.4	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sine-wave pulse	-	0.98	$\text{A}^2\text{s}$
$di_T/dt$	rate of rise of on-state current	$I_G = 0.2\text{ A}$	-	100	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		-	2	A
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	$^\circ\text{C}$
$T_j$	junction temperature		-	125	$^\circ\text{C}$



**Fig. 1. RMS on-state current as a function of surge duration; maximum values**



**Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values**

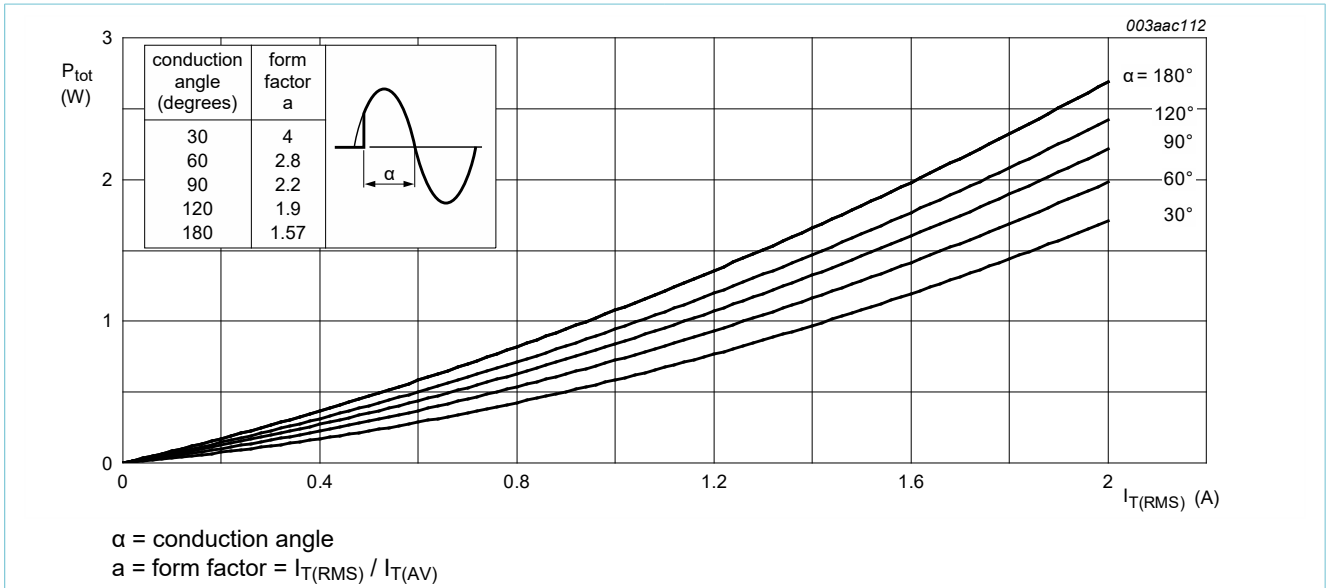


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

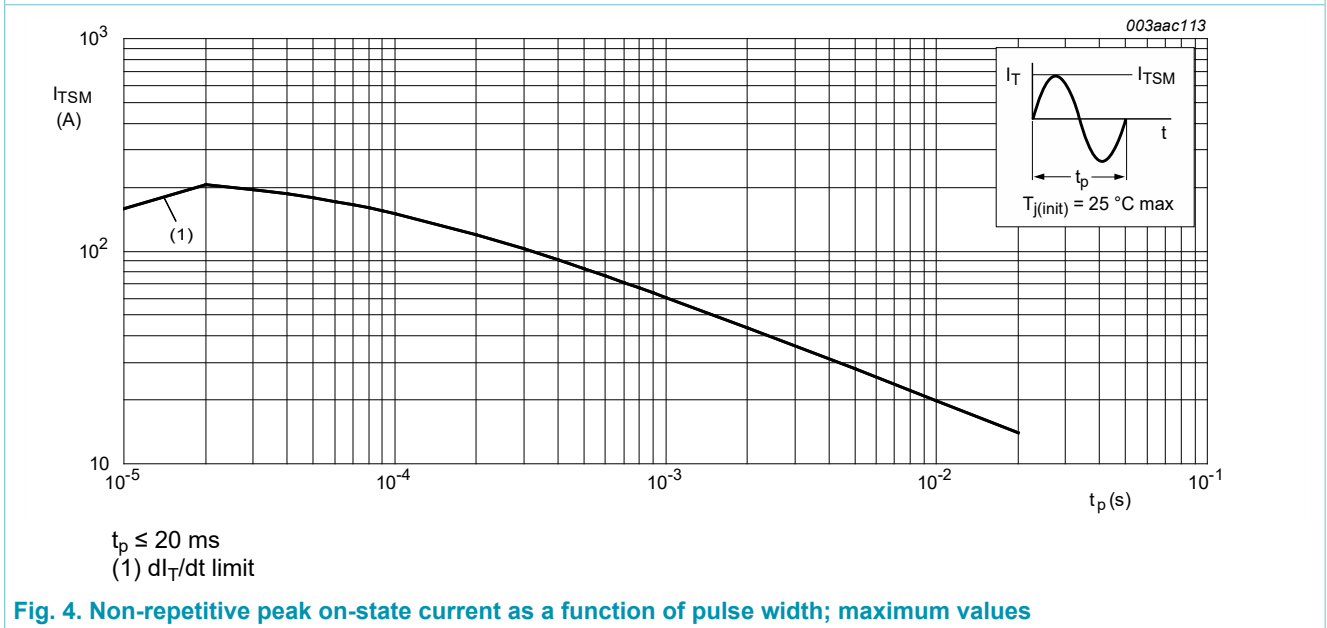


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

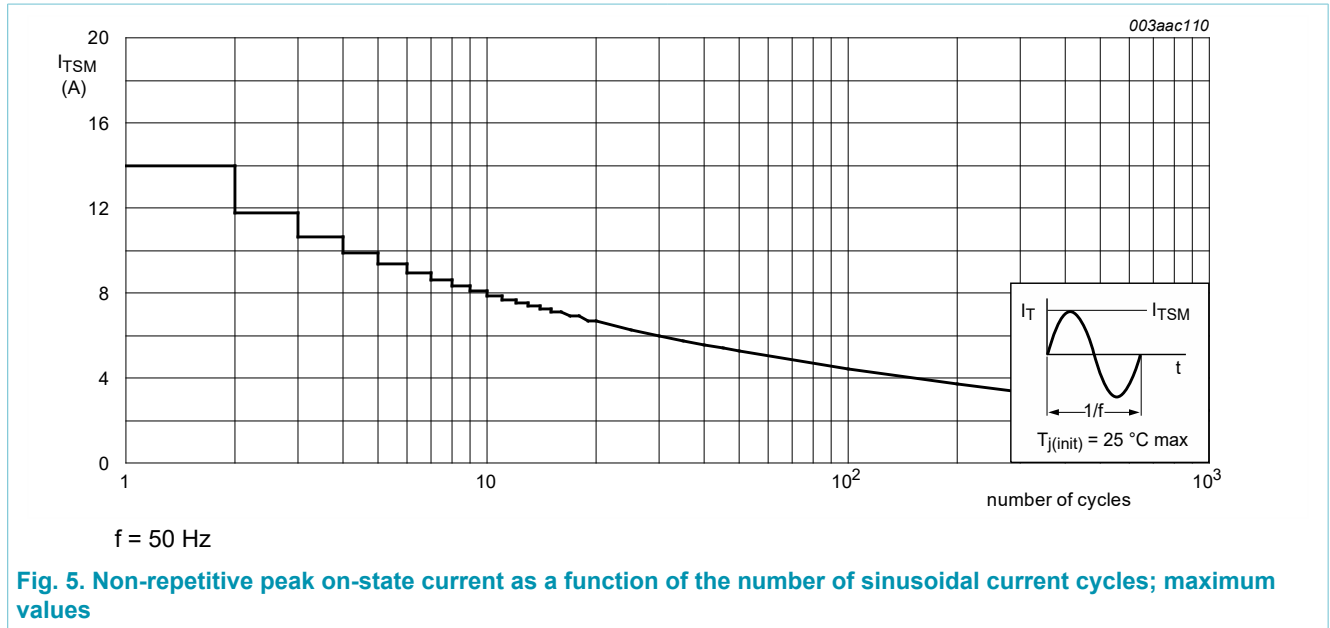


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle; with heatsink compound; <a href="#">Fig. 6</a>	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W

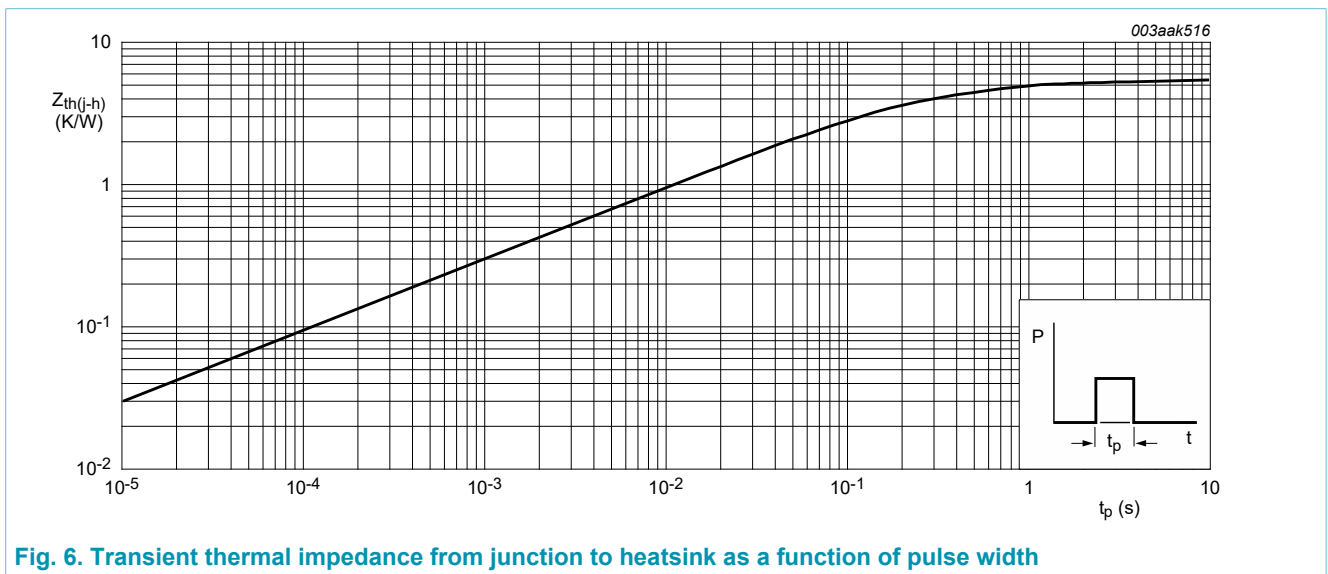


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

## 9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$ ; $RH \leq 65\%$ ; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
$C_{isol}$	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$	-	10	-	pF

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	0.5	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	0.5	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	0.5	-	10	mA
I <sub>L</sub>	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	12	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	20	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	12	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a>	-	-	12	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 3 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	1.63	2	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	-	0.7	1	V
		V <sub>D</sub> = 400 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 11</a>	0.2	0.3	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 800 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 536 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; R <sub>GT1(ext)</sub> = 220 Ω	-	500	-	V/μs
dI <sub>com</sub> /dt	rate of change of commutating current	V <sub>D</sub> = 400 V; T <sub>j</sub> = 125 °C; I <sub>T(RMS)</sub> = 2 A; dV <sub>com</sub> /dt = 20 V/μs; (snubberless condition); gate open circuit	2	-	-	A/ms
		V <sub>D</sub> = 400 V; T <sub>j</sub> = 125 °C; I <sub>T(RMS)</sub> = 2 A; dV <sub>com</sub> /dt = 10 V/μs; gate open circuit	2.3	-	-	A/ms

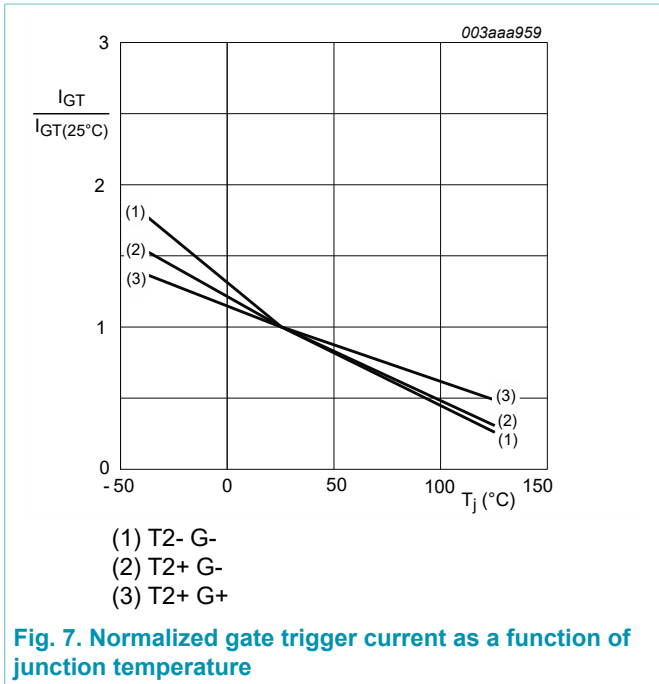


Fig. 7. Normalized gate trigger current as a function of junction temperature

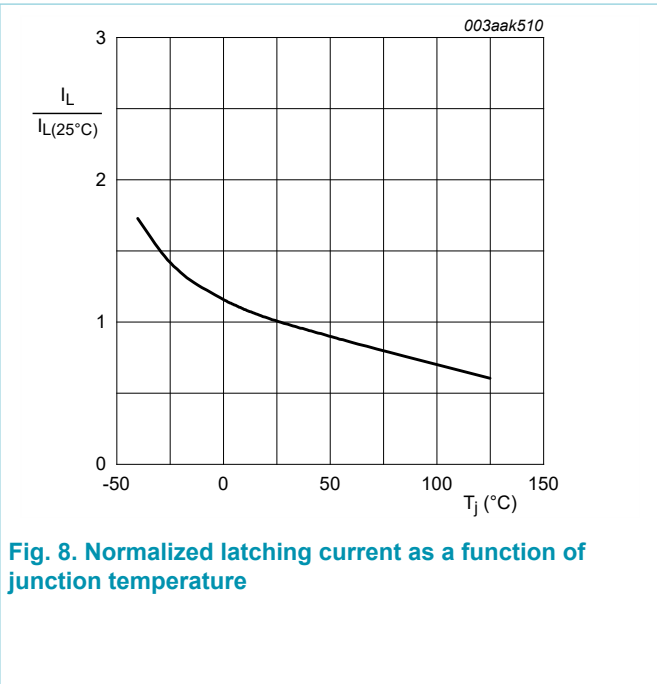


Fig. 8. Normalized latching current as a function of junction temperature

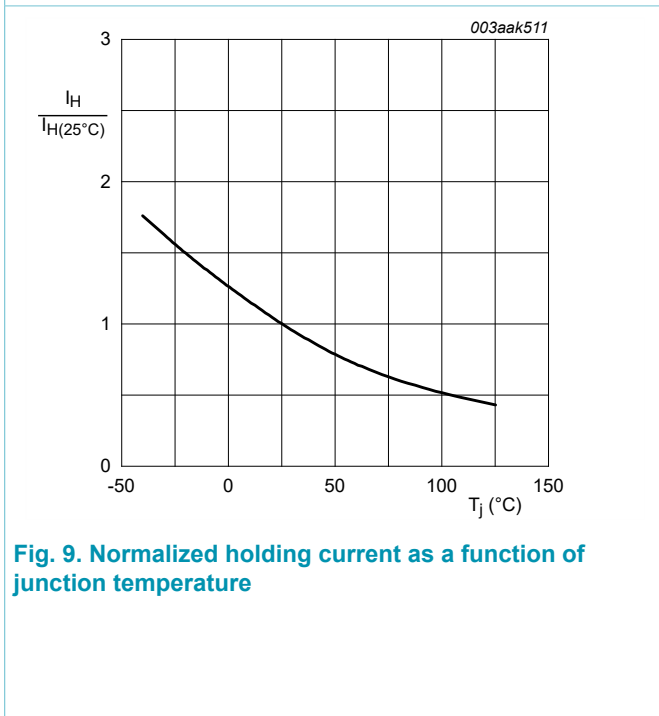


Fig. 9. Normalized holding current as a function of junction temperature

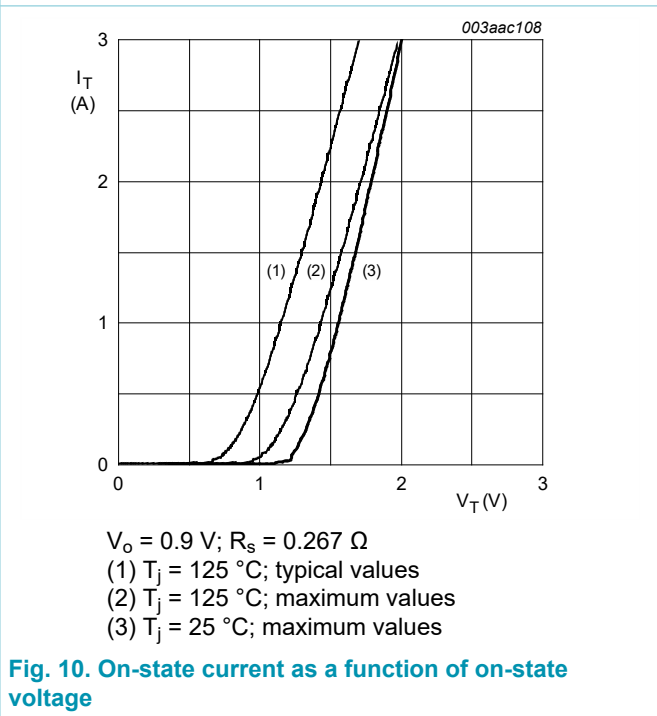


Fig. 10. On-state current as a function of on-state voltage





Fig. 11. Normalized gate trigger voltage as a function of junction temperature

### 11. Package outline



Fig. 12. Package outline TO-220F (SOT186A)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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