



# AD5544-EP

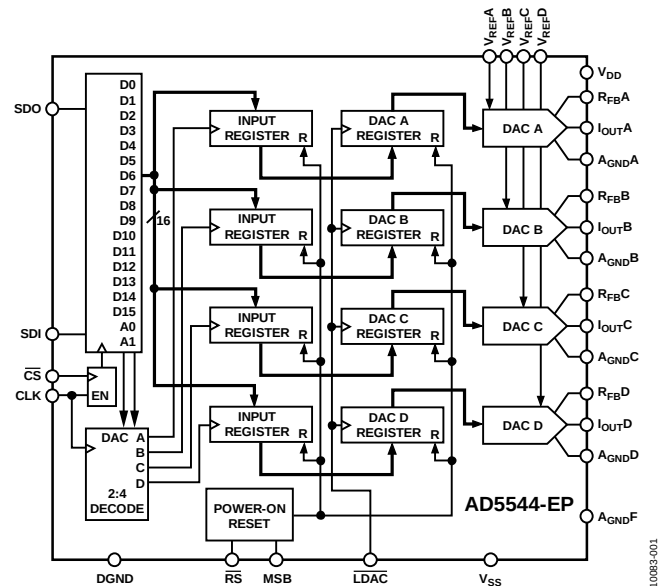


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REVISION HISTORY

4/12—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $I_{OUTX} = \text{virtual GND}$ ,  $A_{GNDX} = 0 \text{ V}$ ,  $V_{REFA} = V_{REFB} = V_{REFC} = V_{REFD} = 10 \text{ V}$ ,  $T_A = \text{full operating temperature range of } -55^\circ\text{C to } +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                             | Symbol                 | Test Condition/Comments                                                            | Min  | Typ        | Max       | Unit                  |
|---------------------------------------|------------------------|------------------------------------------------------------------------------------|------|------------|-----------|-----------------------|
| STATIC PERFORMANCE <sup>1</sup>       |                        |                                                                                    |      |            |           |                       |
| Resolution                            | N                      | 1 LSB = $V_{REFX}/2^{16} = 153 \mu\text{V}$ when $V_{REF} = 10 \text{ V}$          |      |            | 16        | Bits                  |
| Relative Accuracy                     | INL                    |                                                                                    |      |            | $\pm 1.5$ | LSB                   |
| Differential Nonlinearity             | DNL                    |                                                                                    |      |            | $\pm 1.5$ | LSB                   |
| Output Leakage Current                | $I_{OUTX}$             | Data = 0x0000, $T_A = 25^\circ\text{C}$<br>Data = 0x0000, $T_A = 85^\circ\text{C}$ |      |            | 10<br>20  | nA<br>nA              |
| Full-Scale Gain Error                 | $G_{FSE}$              | Data = 0xFFFF                                                                      |      | $\pm 0.75$ | $\pm 4$   | mV                    |
| Full-Scale Tempco <sup>2</sup>        | $TCV_{FS}$             |                                                                                    |      | 1          |           | ppm/ $^\circ\text{C}$ |
| Feedback Resistor                     | $R_{FBX}$              | $V_{DD} = 5 \text{ V}$                                                             | 4    | 6          | 8         | k $\Omega$            |
| REFERENCE INPUT                       |                        |                                                                                    |      |            |           |                       |
| $V_{REFX}$ Range                      | $V_{REFX}$             |                                                                                    | -15  |            | +15       | V                     |
| Input Resistance                      | $R_{REFX}$             |                                                                                    | 4    | 6          | 8         | k $\Omega$            |
| Input Resistance Match                | $R_{REFX}$             | Channel-to-channel                                                                 |      | 0.35       |           | %                     |
| Input Capacitance <sup>2</sup>        | $C_{REFX}$             |                                                                                    |      | 5          |           | pF                    |
| ANALOG OUTPUT                         |                        |                                                                                    |      |            |           |                       |
| Output Current                        | $I_{OUTX}$             | Data = 0xFFFF                                                                      | 1.25 |            | 2.5       | mA                    |
| Output Capacitance <sup>2</sup>       | $C_{OUTX}$             | Code dependent                                                                     |      | 35         |           | pF                    |
| LOGIC INPUT AND OUTPUT                |                        |                                                                                    |      |            |           |                       |
| Logic Input Low Voltage               | $V_{IL}$               |                                                                                    |      |            | 0.8       | V                     |
| Logic Input High Voltage              | $V_{IH}$               |                                                                                    | 2.4  |            |           | V                     |
| Input Leakage Current                 | $I_{IL}$               |                                                                                    |      |            | 1         | $\mu\text{A}$         |
| Input Capacitance <sup>2</sup>        | $C_{IL}$               |                                                                                    |      |            | 10        | pF                    |
| Logic Output Low Voltage              | $V_{OL}$               | $I_{OL} = 1.6 \text{ mA}$                                                          |      |            | 0.4       | V                     |
| Logic Output High Voltage             | $V_{OH}$               | $I_{OH} = 100 \mu\text{A}$                                                         | 4    |            |           | V                     |
| INTERFACE TIMING <sup>2, 3</sup>      |                        |                                                                                    |      |            |           |                       |
| Clock Width High                      | $t_{CH}$               |                                                                                    | 25   |            |           | ns                    |
| Clock Width Low                       | $t_{CL}$               |                                                                                    | 25   |            |           | ns                    |
| $\overline{\text{CS}}$ to Clock Setup | $t_{CSS}$              |                                                                                    | 0    |            |           | ns                    |
| Clock to $\overline{\text{CS}}$ Hold  | $t_{CSH}$              |                                                                                    | 25   |            |           | ns                    |
| Clock to SDO Propagation Delay        | $t_{PD}$               |                                                                                    | 2    |            | 20        | ns                    |
| Load DAC Pulse Width                  | $t_{LDAC}$             |                                                                                    | 25   |            |           | ns                    |
| Data Setup                            | $t_{DS}$               |                                                                                    | 20   |            |           | ns                    |
| Data Hold                             | $t_{DH}$               |                                                                                    | 20   |            |           | ns                    |
| Load Setup                            | $t_{LDS}$              |                                                                                    | 5    |            |           | ns                    |
| Load Hold                             | $t_{LDH}$              |                                                                                    | 25   |            |           | ns                    |
| SUPPLY CHARACTERISTICS                |                        |                                                                                    |      |            |           |                       |
| Power Supply Range                    | $V_{DD \text{ RANGE}}$ |                                                                                    | 2.7  |            | 5.5       | V                     |
| Positive Supply Current               | $I_{DD}$               | Logic inputs = 0 V                                                                 |      |            | 5         | $\mu\text{A}$         |
| Negative Supply Current               | $I_{SS}$               | Logic inputs = 0 V, $V_{SS} = -5 \text{ V}$                                        |      | 0.001      | 9         | $\mu\text{A}$         |
| Power Dissipation                     | $P_{DISS}$             | Logic inputs = 0 V                                                                 |      |            | 1.25      | mW                    |
| Power Supply Sensitivity              | PSS                    | $\Delta V_{DD} = \pm 5\%$                                                          |      |            | 0.006     | %/%                   |

| Parameter                            | Symbol                            | Test Condition/Comments                                                                       | Min | Typ | Max | Unit                         |
|--------------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------|-----|-----|-----|------------------------------|
| AC CHARACTERISTICS <sup>4</sup>      |                                   |                                                                                               |     |     |     |                              |
| Output Voltage Settling Time         | $t_s$                             | To $\pm 0.1\%$ of full scale, data = 0x0000 to 0xFFFF to 0x0000                               |     | 0.9 |     | $\mu\text{s}$                |
| Reference Multiplying Bandwidth (BW) | BW – 3 dB                         | $V_{\text{REF}X} = 5\text{ V p-p}$ , data = 0xFFFF, $C_{\text{FB}} = 2.0\text{ pF}$ ,         |     | 12  |     | MHz                          |
| DAC Glitch Impulse                   | Q                                 | $V_{\text{REF}X} = 8\text{ V}$ , data = 0x0000 to 0x8000 to 0x0000                            |     | –1  |     | nV-sec                       |
| Feedthrough Error                    | $V_{\text{OUT}X}/V_{\text{REF}X}$ | Data = 0x0000, $V_{\text{REF}X} = 100\text{ mV rms}$ , $f = 100\text{ kHz}$                   |     | –65 |     | dB                           |
| Crosstalk Error                      | $V_{\text{OUT}A}/V_{\text{REF}B}$ | Data = 0x0000, $V_{\text{REF}B} = 100\text{ mV rms}$ , adjacent channel, $f = 100\text{ kHz}$ |     | –90 |     | dB                           |
| Digital Feedthrough                  | Q                                 | $\overline{\text{CS}} = 1$ , $f_{\text{CLK}} = 1\text{ MHz}$                                  |     | 0.6 |     | nV-sec                       |
| Total Harmonic Distortion            | THD                               | $V_{\text{REF}X} = 5\text{ V p-p}$ , data = 0xFFFF, $f = 1\text{ kHz}$                        |     | –98 |     | dB                           |
| Output Spot Noise Voltage            | $e_N$                             | $f = 1\text{ kHz}$ , BW = 1 Hz                                                                |     | 7   |     | $\text{nV}/\sqrt{\text{Hz}}$ |

<sup>1</sup> All static performance tests (except  $I_{\text{OUT}X}$ ) are performed in a closed-loop system using an external precision [OP177](#) I-to-V converter amplifier. The AD5544  $R_{\text{FB}}$  terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.

<sup>2</sup> These parameters are guaranteed by design and not subject to production testing.

<sup>3</sup> All input control signals are specified with  $t_{\text{R}} = t_{\text{F}} = 2.5\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

<sup>4</sup> All ac characteristic tests are performed in a closed-loop system using an [AD8038](#) I-to-V converter amplifier.

## TIMING DIAGRAMS

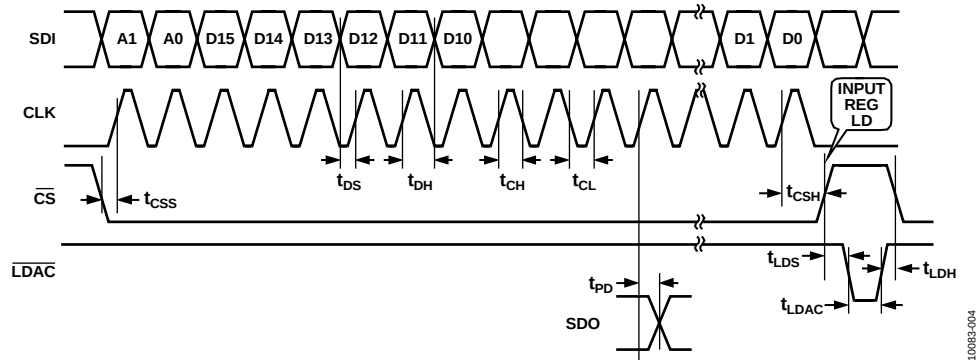


Figure 2. Timing Diagram

10083-004

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter                                                  | Rating                                |
|------------------------------------------------------------|---------------------------------------|
| $V_{DD}$ to GND                                            | −0.3 V, +8 V                          |
| $V_{SS}$ to GND                                            | +0.3 V, −7 V                          |
| $V_{REFX}$ to GND                                          | −18 V, +18 V                          |
| Logic Input and Output to GND                              | −0.3 V, +8 V                          |
| $V(I_{OUTX})$ to GND                                       | −0.3 V, $V_{DD} + 0.3$ V              |
| $A_{GNDX}$ to DGND                                         | −0.3 V, +0.3 V                        |
| Input Current to Any Pin Except Supplies                   | ±50 mA                                |
| Package Power Dissipation                                  | $(T_J \text{ max} - T_A)/\theta_{JA}$ |
| Thermal Resistance                                         | $\theta_{JA}$                         |
| 28-Lead SSOP                                               | 100°C/W                               |
| 32-Lead LFCSP                                              | 32.5°C/W                              |
| Maximum Junction Temperature ( $T_J$ Max)                  | 150°C                                 |
| Operating Temperature Range, Enhanced Product (EP Version) | −55°C to +125°C                       |
| Storage Temperature Range                                  | −65°C to +150°C                       |
| Lead Temperature                                           |                                       |
| Vapor Phase, 60 Sec                                        | 215°C                                 |
| Infrared, 15 Sec                                           | 220°C                                 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

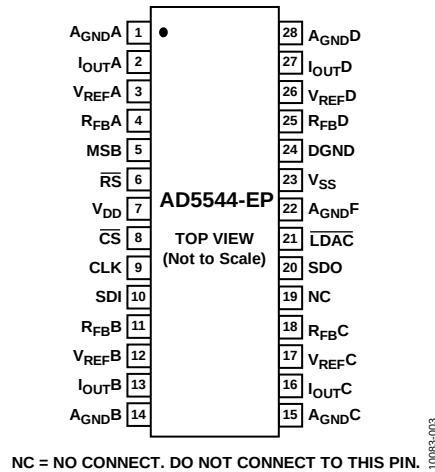


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic          | Description                                                                                                                                                                                            |
|---------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | $A_{GND}A$        | DAC A Analog Ground.                                                                                                                                                                                   |
| 2       | $I_{OUT}A$        | DAC A Current Output.                                                                                                                                                                                  |
| 3       | $V_{REF}A$        | DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. This pin can be tied to the $V_{DD}$ pin.                                                                         |
| 4       | $R_{FB}A$         | Establish the voltage output for DAC A by connecting to an external amplifier output.                                                                                                                  |
| 5       | MSB               | MSB Pin. Set pin during a reset pulse ( $\overline{RS}$ ) or at system power-on if tied to ground or $V_{DD}$ .                                                                                        |
| 6       | $\overline{RS}$   | Reset Pin, Active Low Input. Input registers and DAC registers are set to all 0s or half-scale code, determined by the voltage on the MSB pin. Register data = 0x0000 when MSB = 0.                    |
| 7       | $V_{DD}$          | Positive Power Supply Input. Specified range of operation: $5V \pm 10\%$ .                                                                                                                             |
| 8       | $\overline{CS}$   | Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}/LDAC$ returns high. Does not affect LDAC operation. |
| 9       | CLK               | Clock Input. Positive edge clocks data into the shift register.                                                                                                                                        |
| 10      | SDI               | Serial Data Input. Input data loads directly into the shift register.                                                                                                                                  |
| 11      | $R_{FB}B$         | Establish the voltage output for DAC B by connecting to an external amplifier output.                                                                                                                  |
| 12      | $V_{REF}B$        | DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. This pin can be tied to the $V_{DD}$ pin.                                                                         |
| 13      | $I_{OUT}B$        | DAC B Current Output.                                                                                                                                                                                  |
| 14      | $A_{GND}B$        | DAC B Analog Ground.                                                                                                                                                                                   |
| 15      | $A_{GND}C$        | DAC C Analog Ground.                                                                                                                                                                                   |
| 16      | $I_{OUT}C$        | DAC C Current Output.                                                                                                                                                                                  |
| 17      | $V_{REF}C$        | DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. This pin can be tied to the $V_{DD}$ pin.                                                                         |
| 18      | $R_{FB}C$         | Establish the voltage output for DAC C by connecting to an external amplifier output.                                                                                                                  |
| 19      | NC                | No Connect. Do not connect to this pin.                                                                                                                                                                |
| 20      | SDO               | Serial Data Output. Input data loads directly into the shift register. Data appears at SDO at 19 clock pulses for the AD5544-EP after input at the SDI pin.                                            |
| 21      | $\overline{LDAC}$ | Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input.                                                               |
| 22      | $A_{GND}F$        | High Current Analog Force Ground.                                                                                                                                                                      |
| 23      | $V_{SS}$          | Negative Bias Power Supply Input. Specified range of operation: $-5.5V$ to $+0.3V$ .                                                                                                                   |
| 24      | DGND              | Digital Ground Pin.                                                                                                                                                                                    |
| 25      | $R_{FB}D$         | Establish the voltage output for DAC D by connecting to an external amplifier output.                                                                                                                  |

| Pin No. | Mnemonic   | Description                                                                                                                    |
|---------|------------|--------------------------------------------------------------------------------------------------------------------------------|
| 26      | $V_{REF}D$ | DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. This pin can be tied to the $V_{DD}$ pin. |
| 27      | $I_{OUT}D$ | DAC D Current Output.                                                                                                          |
| 28      | $A_{GND}D$ | DAC D Analog Ground.                                                                                                           |

## TYPICAL PERFORMANCE CHARACTERISTICS

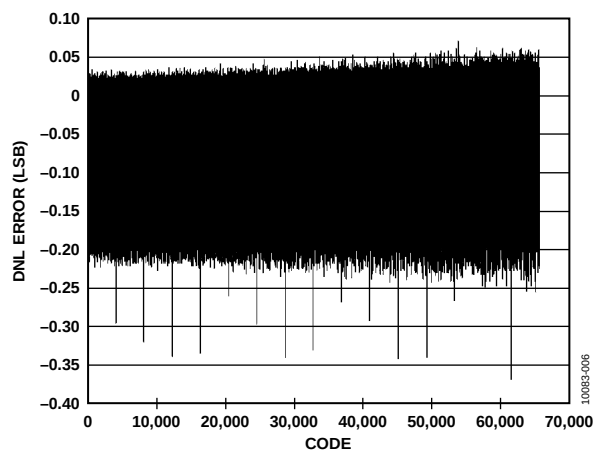
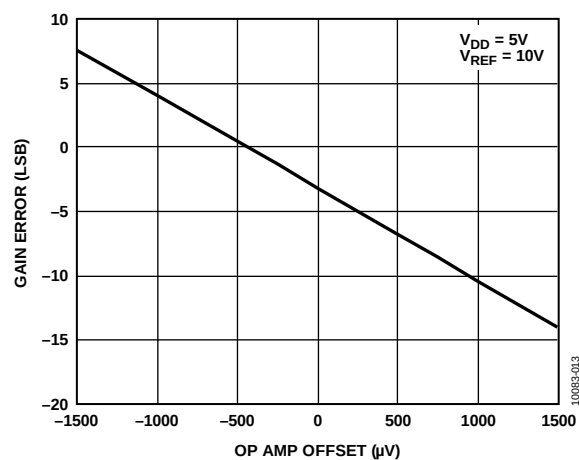
Figure 4. DNL Error vs. Code,  $T_A = 25^\circ\text{C}$ 

Figure 7. Gain Error vs. Op Amp Offset

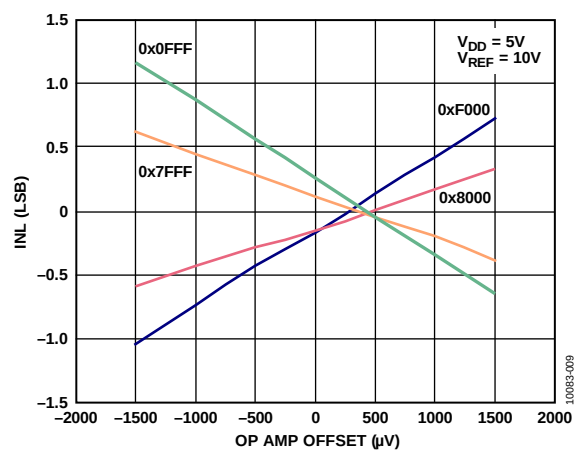


Figure 5. INL Error vs. Op Amp Offset

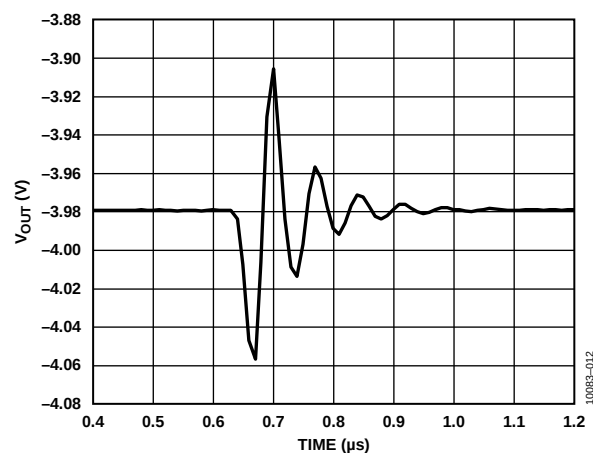


Figure 8. Midscale Transition

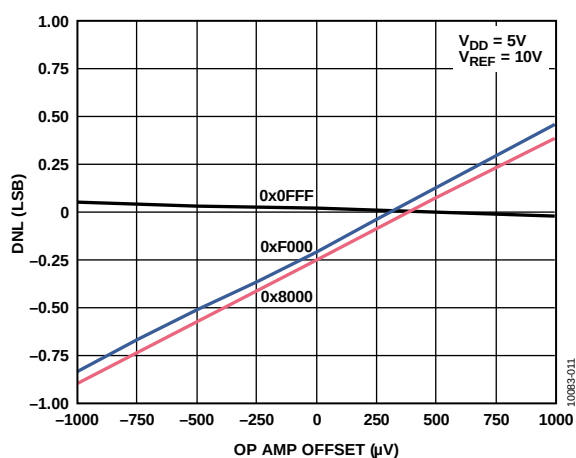


Figure 6. DNL Error vs. Op Amp Offset

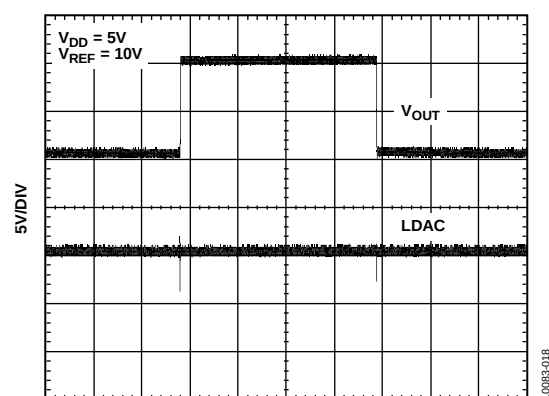


Figure 9. Large Signal Settling Time

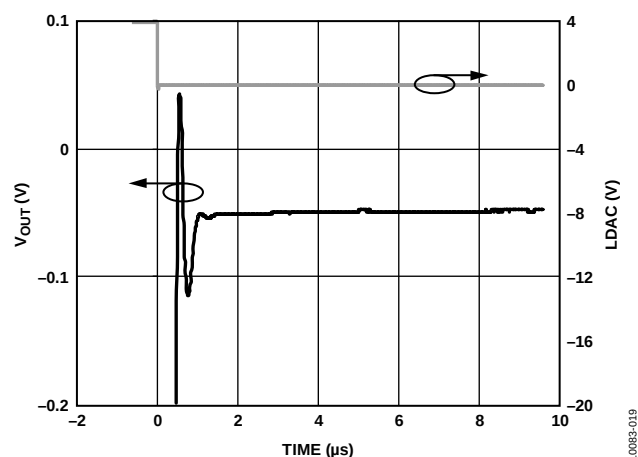


Figure 10. Small Signal Settling Time

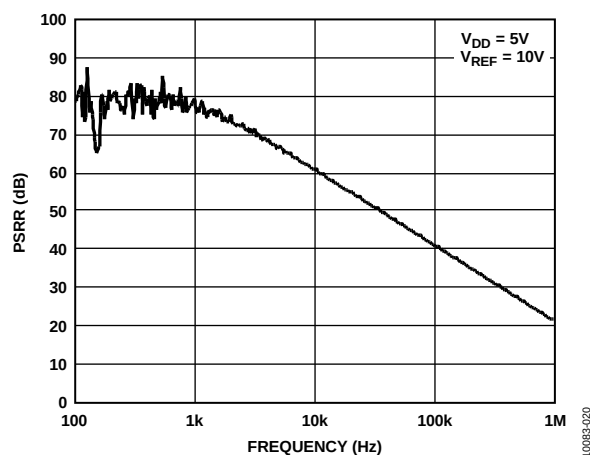


Figure 12. Power Supply Rejection vs. Frequency

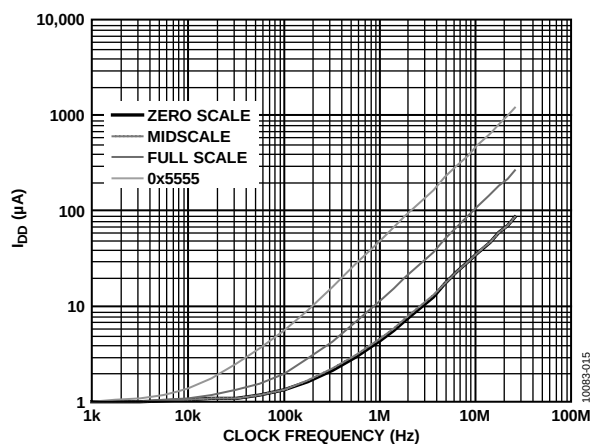


Figure 11. Power Supply Current vs. Clock Frequency

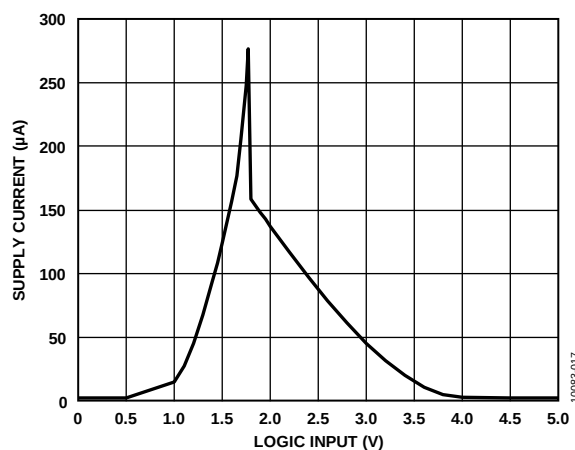


Figure 13. Power Supply Current vs. Logic Input Voltage

OUTLINE DIMENSIONS

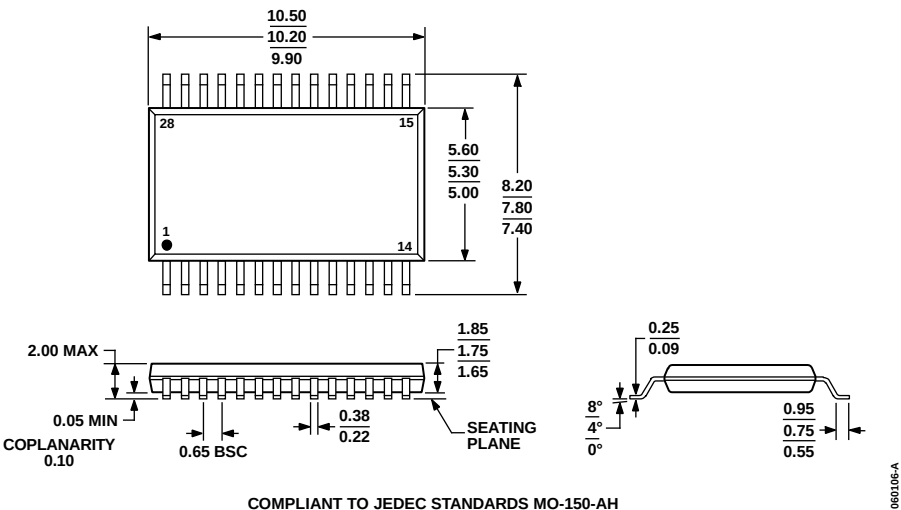


Figure 4. 28-Lead Shrink Small Outline Package [SSOP]  
(RS-28)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model        | Resolution (Bits) | INL LSB | DNL LSB | Temperature Range | Package Description                         | Package Option |
|--------------|-------------------|---------|---------|-------------------|---------------------------------------------|----------------|
| AD5544SRS-EP | 16                | ±1.5    | ±1.5    | −55°C to +125°C   | 28-Lead Shrink Small Outline Package [SSOP] | RS-28          |

## NOTES

## NOTES

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Наши преимущества:

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- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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кабельные сборки и микроволновые компоненты:

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