Matched Monolithic Quad Transistor

MAT14

FEATURES

Low offset voltage: 400 µV maximum
High current gain: 300 minimum
Excellent current gain match: 4% maximum
Low voltage noise density at 100 Hz, 1 mA
3 nV/√Hz maximum
Excellent log conformance
Bulk resistance (r_{BE}) = 0.6 Ω maximum
Guaranteed matching for all transistors

APPLICATIONS

Low noise op amp front end
Current mirror and current sink/source
Low noise instrumentation amplifiers
Voltage controlled attenuators
Log amplifiers

PIN CONFIGURATION

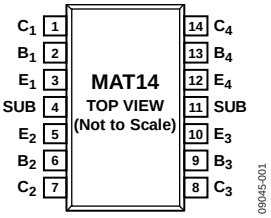

Figure 1.

GENERAL DESCRIPTION

The MAT14 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and nonlinear circuit applications. Performance characteristics of the MAT14 include high gain (300 minimum) over a wide range of collector current, low noise (3 nV/√Hz maximum at 100 Hz, I_C = 1 mA), and excellent logarithmic conformance. The MAT14 also features a low offset voltage of 100 µV typical and tight current gain matching to within 4%. Each transistor of the MAT14 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at an ambient temperature of 25°C and over the industrial temperature range.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias, base emitter current. The superior logarithmic conformance and accurate matching characteristics of the MAT14 make it an excellent choice for use in log and antilog circuits. The MAT14 is an ideal choice in applications where low noise and high gain are required.

Rev. A
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113
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REVISION HISTORY

12/10—Rev. 0 to Rev. A

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10/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC AND AC CHARACTERISTICS						
Current Gain	h_{FE}	10 µA ≤ I_C ≤ 1 mA				
		0 V ≤ V_{CB} ≤ 30 V[1]	300	600		
		−40°C ≤ T_A ≤ +85°C	200	500		
Current Gain Match	Δh_{FE}	I_C = 100 µA[2]		1	4	%
		0 V ≤ V_{CB} ≤ 30 V				
Noise Voltage Density	e_N	I_C = 1 mA, V_{CB} = 0[3]				
		f_O = 10 Hz		2	4	nV/√Hz
		f_O = 100 Hz		1.8	3	nV/√Hz
		f_O = 1 kHz		1.8	3	nV/√Hz
Offset Voltage	V_{OS}	10 µA ≤ I_C ≤ 1 mA[4]				
		0 V ≤ V_{CB} ≤ 30 V		100	400	µV
		−40°C ≤ T_A ≤ +85°C		120	520	µV
Offset Voltage Change vs. V_{CB} Change	$\Delta V_{OS}/\Delta V_{CB}$	0 V ≤ V_{CB} ≤ 30 V[4]				
		10 µA ≤ I_C ≤ 1 mA		100	200	µV
Offset Voltage Change vs. I_C Change	$\Delta V_{OS}/\Delta I_C$	10 µA ≤ I_C ≤ 1 mA[4], V_{CB} = 0 V		10	50	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C				
		I_C = 100 µA, V_{CB} = 0 V		0.4	2	µV/°C
Breakdown Voltage	BV_{CEO}	I_C = 10 µA	40			V
		−40°C ≤ T_A ≤ +85°C	40			V
Gain-Bandwidth Product	f_T	I_C = 1 mA, V_{CE} = 10 V		300		MHz
Collector Leakage Current						
Base	I_{CBO}	V_{CB} = 40 V		5		pA
		−40°C ≤T_A ≤ +85°C		0.5		nA
Substrate	I_{CS}	V_{CS} = 40 V		0.5		nA
		−40°C ≤ T_A ≤ +85°C		0.7		nA
Emitter	I_{CES}	V_{CE} = 40 V		3		nA
		−40°C ≤ T_A ≤ +85°C		5		nA
Input Current						
Bias	I_B	I_C = 100 µA, 0 V ≤ V_{CB} ≤ 30 V		165	330	nA
		−40°C ≤ T_A ≤ +85°C		200	500	nA
Offset	I_{OS}	I_C = 100 µA, V_{CB} = 0 V		2	13	nA
		−40°C ≤ T_A ≤ +85°C		8	40	nA
Offset Drift	$\Delta I_{OS}/\Delta T$	I_C = 100 µA				
		−40°C ≤ T_A ≤ +85°C		100		pA/°C
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA		0.03	0.06	V
Output Capacitance	C_{OBO}	V_{CB} = 15 V, I_E[5] = 0, f = 1 MHz		10		pF
Bulk Resistance	r_{BE}	10 µA ≤ I_C ≤ 10 mA,V_{CB} = 0 V[6]		0.4	0.6	Ω
Input Capacitance	C_{EBO}	V_{CB} = 15 V, I_E = 0, f = 1 MHz		40		pF

[1] Current gain measured at I_C = 10 µA, 100 µA, and 1 mA.
[2] Current gain match (Δh_{FE}) defined as: $\Delta h_{FE} = (100(\Delta I_B)(h_{FE\,min})/I_C)$.
[3] Sample tested.
[4] Measured at I_C = 10 µA and guaranteed by design over the specified range of I_C.
[5] See Table 2 for the emitter current rating.
[6] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Collector-to-Base Voltage (BV_{CBO})	40 V
Collector-to-Emitter Voltage (BV_{CEO})	40 V
Collector-to-Collector Voltage (BV_{CC})	40 V
Emitter-to-Emitter Voltage (BV_{EE})	40 V
Current	
Collector Current (I_C)	30 mA
Emitter Current (I_E)	30 mA
Temperature	
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC	115	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

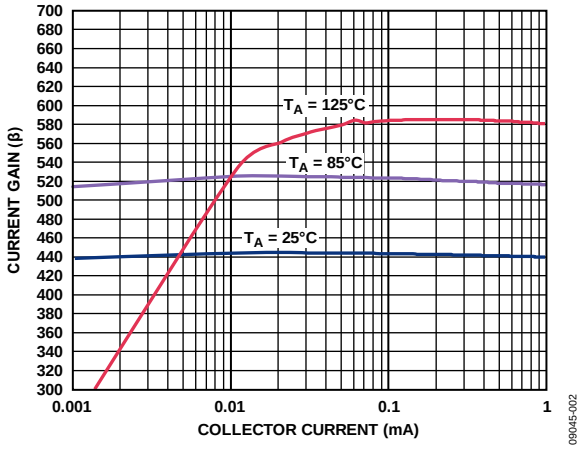


Figure 2. Current Gain vs. Collector Current

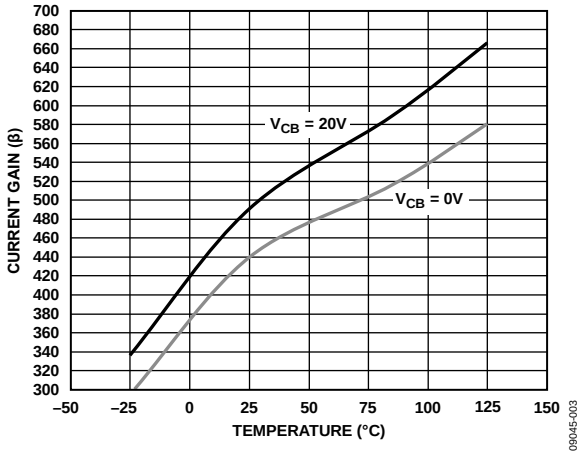


Figure 3. Current Gain vs. Temperature

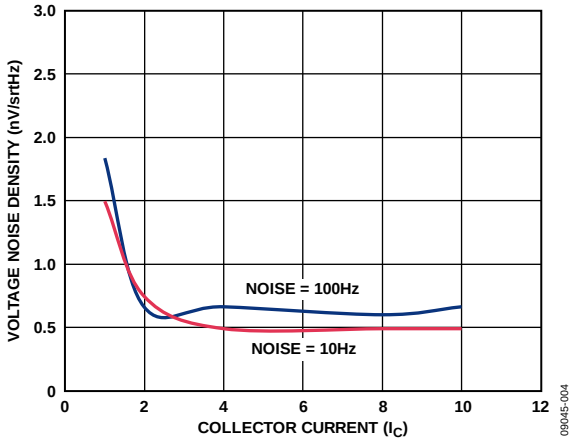


Figure 4. Voltage Noise Density vs. Collector Current

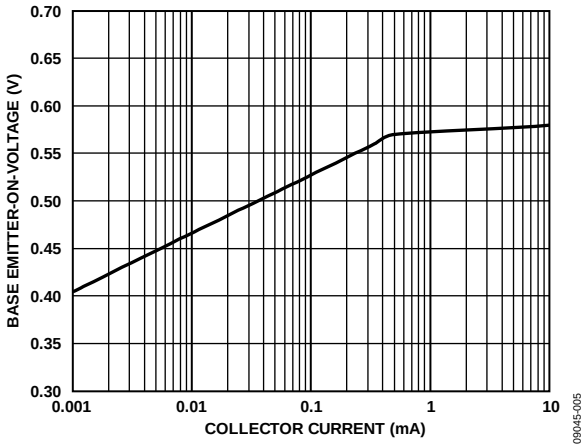


Figure 5. Base Emitter-On-Voltage vs. Collector Current

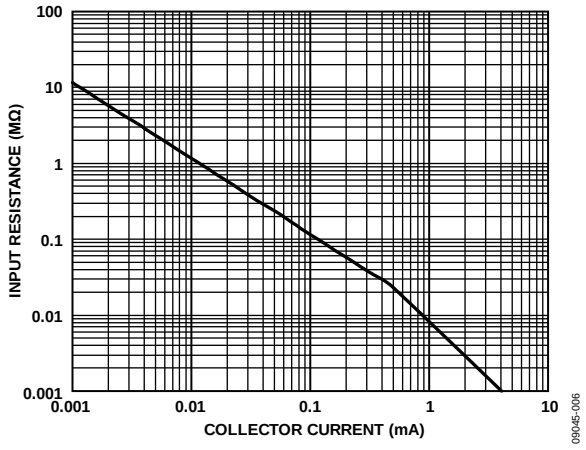


Figure 6. Small Signal Input Resistance vs. Collector Current

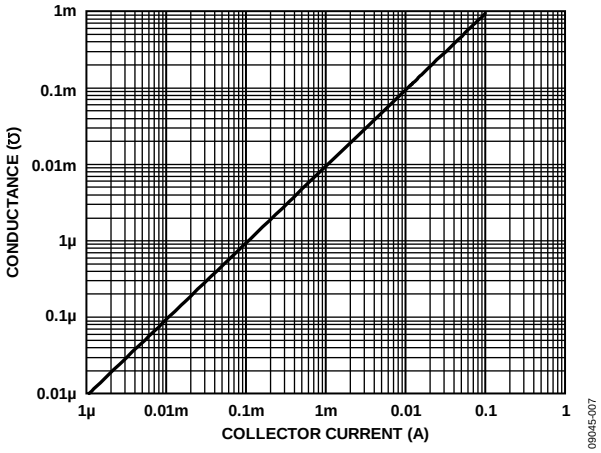


Figure 7. Small Signal Output Conductance vs. Collector Current

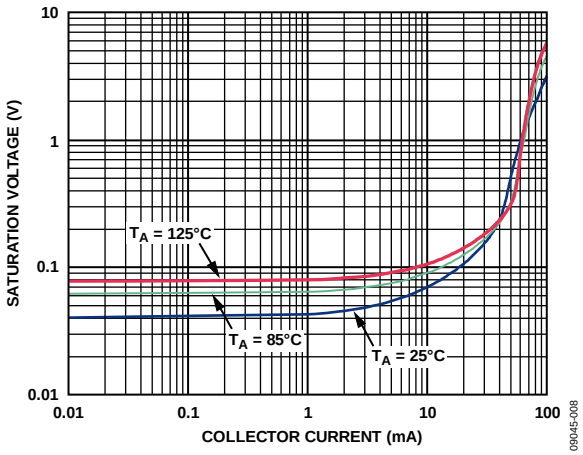


Figure 8. Saturation Voltage vs. Collector Current

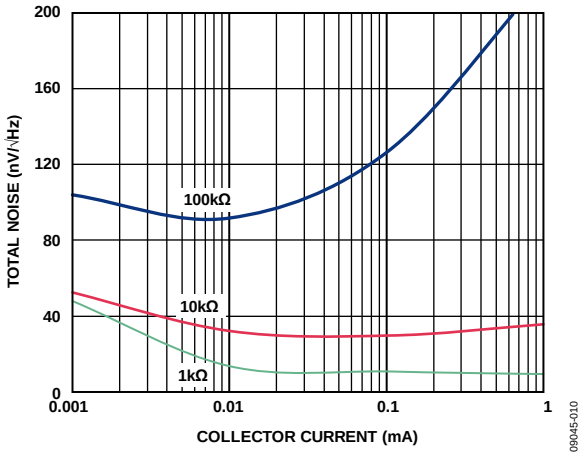


Figure 10. Total Noise vs. Collector Current

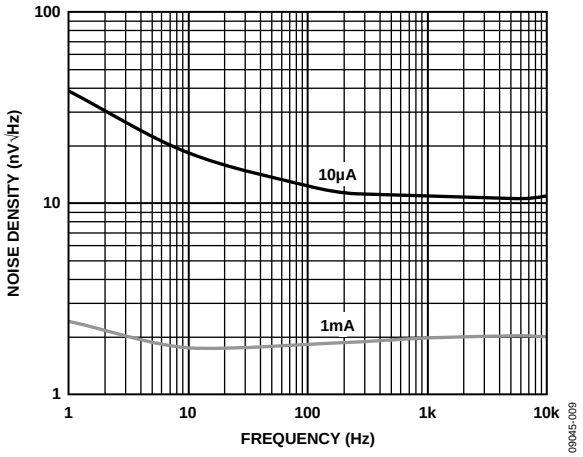


Figure 9. Noise Voltage Density vs. Frequency

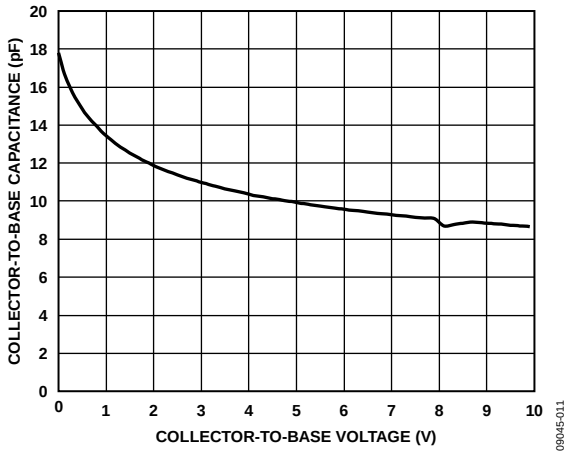


Figure 11. Collector-to-Base Capacitance vs. Collector-to-Base Voltage

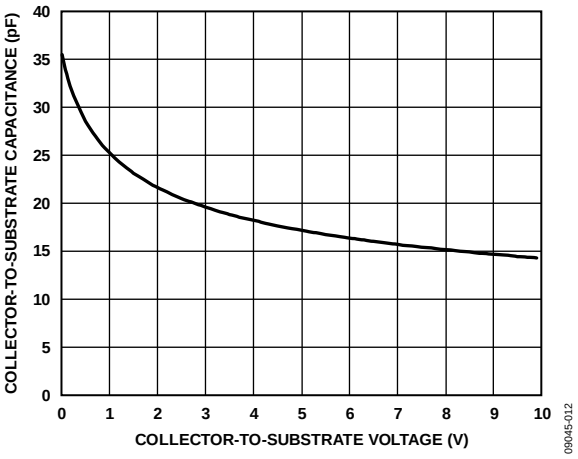


Figure 12. Collector-to-Substrate Capacitance vs. Collector-to-Substrate Voltage

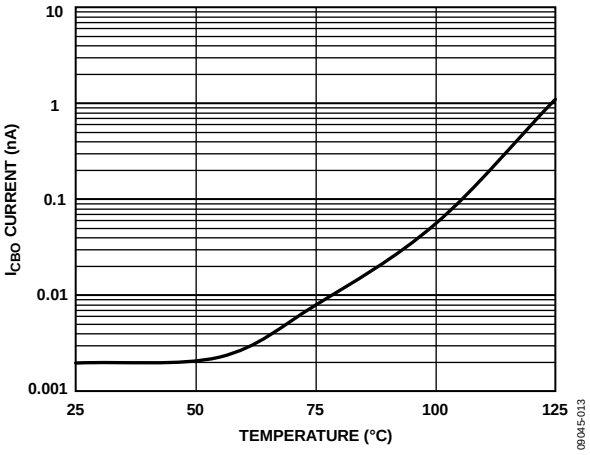


Figure 13. Collector-to-Base Leakage vs. Temperature

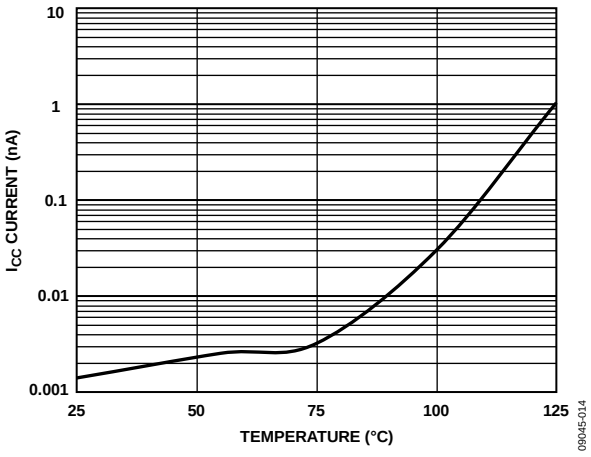


Figure 14. Collector-to-Collector Leakage vs. Temperature

THEORY OF OPERATION

APPLICATIONS INFORMATION

To minimize coupling between devices, tie one of the substrate pins (Pin 4 or Pin 11) to the most negative circuit potential. Note that Pin 4 and Pin 11 are internally connected.

Applications Current Sources

MAT14 can be used to implement a variety of high impedance current mirrors as shown in Figure 15, Figure 16, and Figure 17. These current mirrors can be used as biasing elements and load devices for amplifier stages.

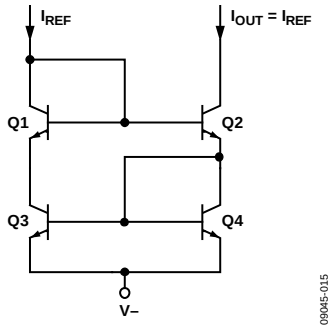


Figure 15. Unity-Gain Current Mirror, $I_{OUT} = I_{REF}$

The unity-gain current mirror shown in Figure 15 has an accuracy of better than 1% and an output impedance of more than 100 MΩ at 100 µA.

Figure 16 and Figure 17 each show a modified current mirror; Figure 16 is designed for a current gain of two (2), and Figure 17 is designed for a current gain of one-half (½). The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but remains better than 2%.

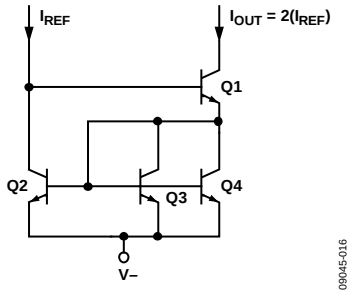


Figure 16. Current Mirror, $I_{OUT} = 2(I_{REF})$

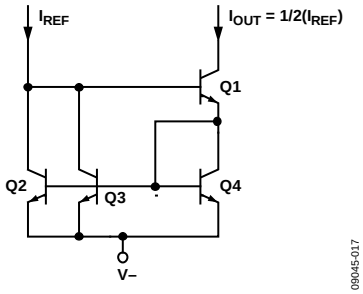


Figure 17. Current Mirror, $I_{OUT} = ½(I_{REF})$

Figure 18 is a temperature independent current sink that has an accuracy of better than 1% at an output current of 100 µA to 1 mA. A Schottky diode acts as a clamp to ensure correct circuit startup at power-on. Use 1% metal film type resistors in this circuit.

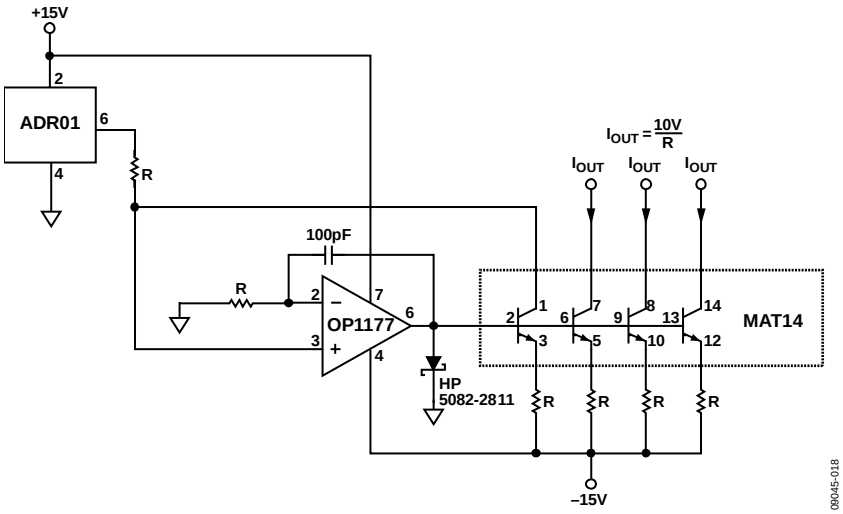
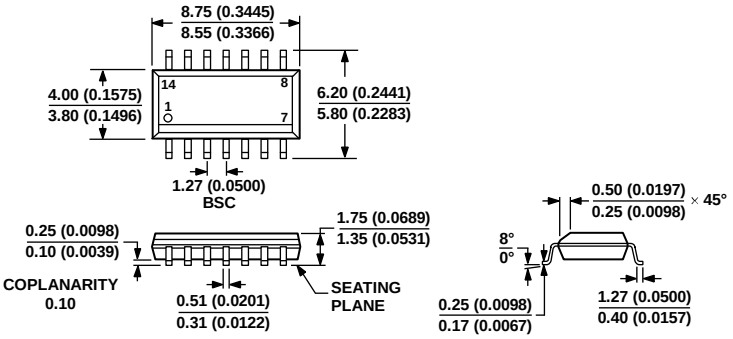


Figure 18. Temperature Independent Current Sink, $I_{OUT} = 10\ V/R$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 19. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
MAT14ARZ	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
MAT14ARZ-R7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
MAT14ARZ-RL	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14

[1] Z = RoHS Compliant Part.

NOTES

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NOTES

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А