



# PRMD3

## 50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

14 September 2018

Product data sheet

### 1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) in a leadless ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PRMH11; PNP/PNP complement: PRMB11.

### 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

### 3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

### 4. Quick reference data

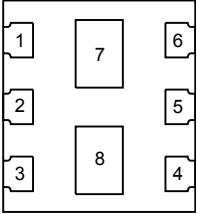
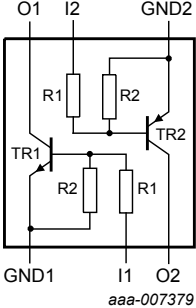
Table 1. Quick reference data

| Symbol                                                               | Parameter                 | Conditions                                                                     | Min | Typ | Max | Unit          |
|----------------------------------------------------------------------|---------------------------|--------------------------------------------------------------------------------|-----|-----|-----|---------------|
| <b>Per transistor, for the PNP transistor with negative polarity</b> |                           |                                                                                |     |     |     |               |
| $V_{CEO}$                                                            | collector-emitter voltage | open base                                                                      | -   | -   | 50  | V             |
| $I_O$                                                                | output current            |                                                                                | -   | -   | 100 | mA            |
| $h_{FE}$                                                             | DC current gain           | $V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | 30  | -   | -   |               |
| R1                                                                   | bias resistor 1           | $T_{amb} = 25\text{ }^{\circ}\text{C}$                                         | [1] | 7   | 10  | 13 k $\Omega$ |
| R2/R1                                                                | bias resistor ratio       |                                                                                | [1] | 0.8 | 1   | 1.2           |

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description            | Simplified outline                                                                                                                        | Graphic symbol                                                                                        |
|-----|--------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| 1   | GND1   | GND (emitter) TR1      |  <p>Transparent top view<br/>DFN1412-6<br/>(SOT1268)</p> |  <p>aaa-007379</p> |
| 2   | I1     | input (base) TR1       |                                                                                                                                           |                                                                                                       |
| 3   | O2     | output (collector) TR2 |                                                                                                                                           |                                                                                                       |
| 4   | GND2   | GND (emitter) TR2      |                                                                                                                                           |                                                                                                       |
| 5   | I2     | input (base) TR2       |                                                                                                                                           |                                                                                                       |
| 6   | O1     | output (collector) TR1 |                                                                                                                                           |                                                                                                       |
| 7   | O1     | output (collector) TR1 |                                                                                                                                           |                                                                                                       |
| 8   | O2     | output (collector) TR2 |                                                                                                                                           |                                                                                                       |

6. Ordering information

Table 3. Ordering information

| Type number | Package   |                                                                                                                   |         |
|-------------|-----------|-------------------------------------------------------------------------------------------------------------------|---------|
|             | Name      | Description                                                                                                       | Version |
| PRMD3       | DFN1412-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm | SOT1268 |

7. Marking

Table 4. Marking codes

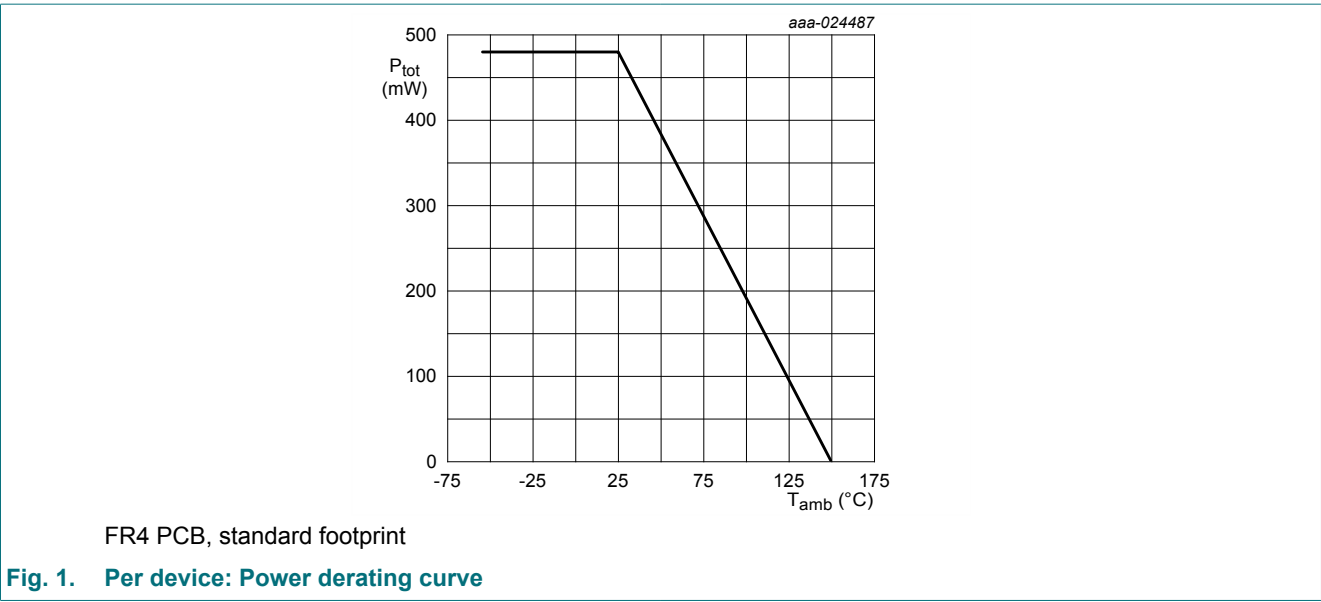
| Type number | Marking code |
|-------------|--------------|
| PRMD3       | B3           |

8. Limiting values

Table 5. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                                                               | Parameter                 | Conditions               |     | Min | Max | Unit |
|----------------------------------------------------------------------|---------------------------|--------------------------|-----|-----|-----|------|
| <b>Per transistor, for the PNP transistor with negative polarity</b> |                           |                          |     |     |     |      |
| V <sub>CBO</sub>                                                     | collector-base voltage    | open emitter             |     | -   | 50  | V    |
| V <sub>CEO</sub>                                                     | collector-emitter voltage | open base                |     | -   | 50  | V    |
| V <sub>EBO</sub>                                                     | emitter-base voltage      | open collector           |     | -   | 10  | V    |
| V <sub>I</sub>                                                       | input voltage             | positive                 |     | -   | 40  | V    |
|                                                                      |                           | negative                 |     | -   | -10 | V    |
| I <sub>O</sub>                                                       | output current            |                          |     | -   | 100 | mA   |
| P <sub>tot</sub>                                                     | total power dissipation   | T <sub>amb</sub> ≤ 25 °C | [1] | -   | 325 | mW   |
| <b>Per device</b>                                                    |                           |                          |     |     |     |      |
| P <sub>tot</sub>                                                     | total power dissipation   | T <sub>amb</sub> ≤ 25 °C | [1] | -   | 480 | mW   |
| T <sub>j</sub>                                                       | junction temperature      |                          |     | -   | 150 | °C   |
| T <sub>amb</sub>                                                     | ambient temperature       |                          |     | -55 | 150 | °C   |
| T <sub>stg</sub>                                                     | storage temperature       |                          |     | -65 | 150 | °C   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

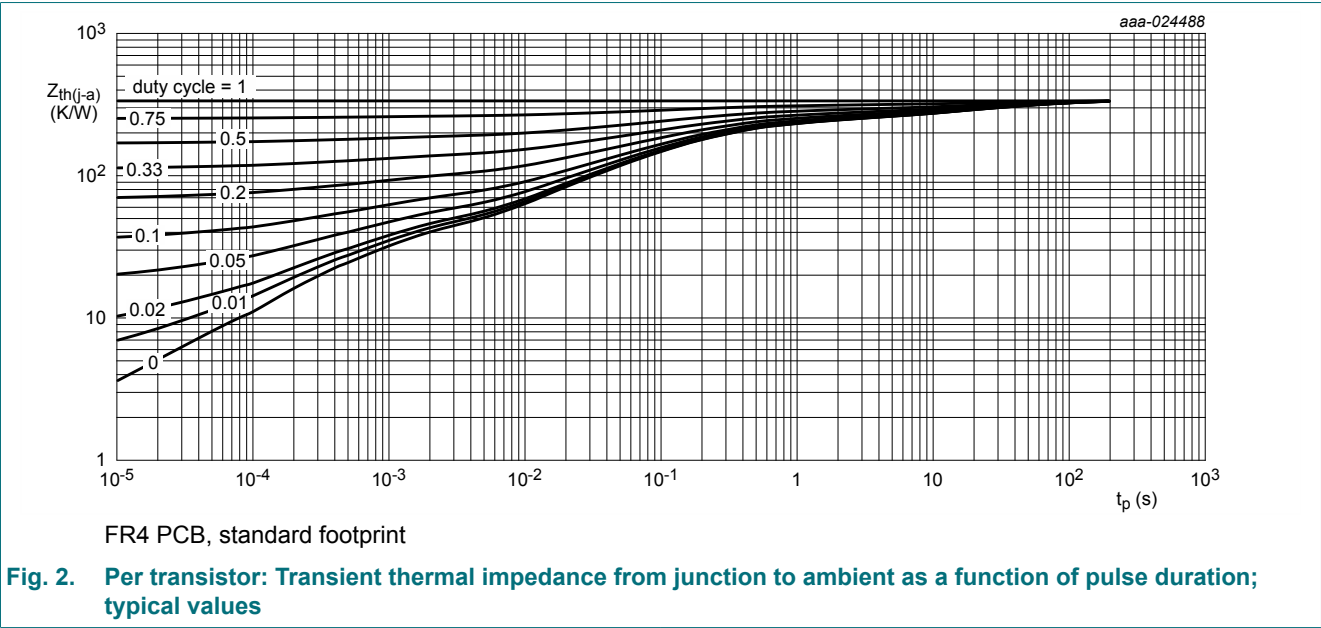


9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter                                   | Conditions  |     | Min | Typ | Max | Unit |
|----------------|---------------------------------------------|-------------|-----|-----|-----|-----|------|
| Per transistor |                                             |             |     |     |     |     |      |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient | in free air | [1] | -   | -   | 385 | K/W  |
| Per device     |                                             |             |     |     |     |     |      |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient | in free air | [1] | -   | -   | 261 | K/W  |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



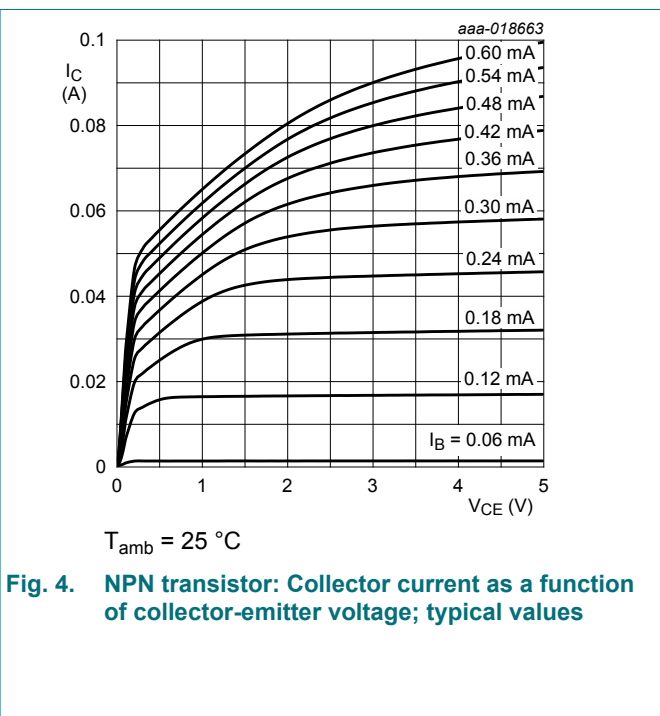
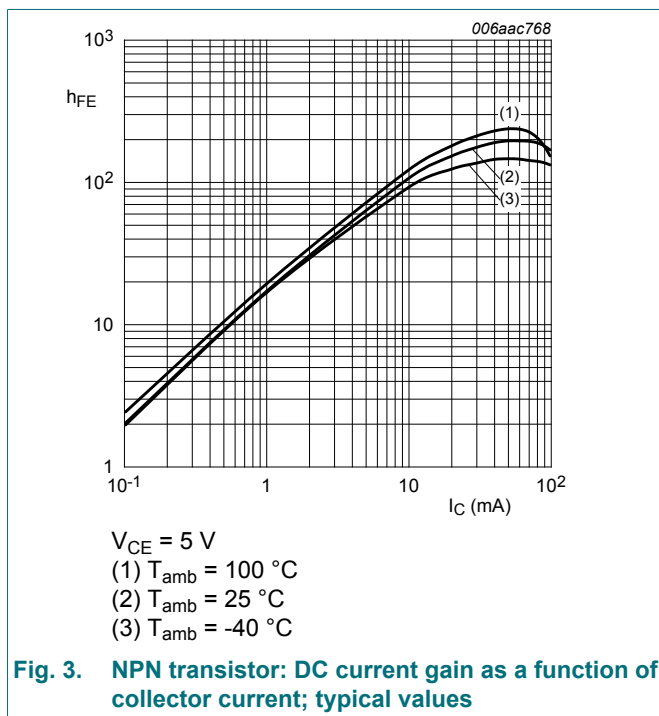
## 10. Characteristics

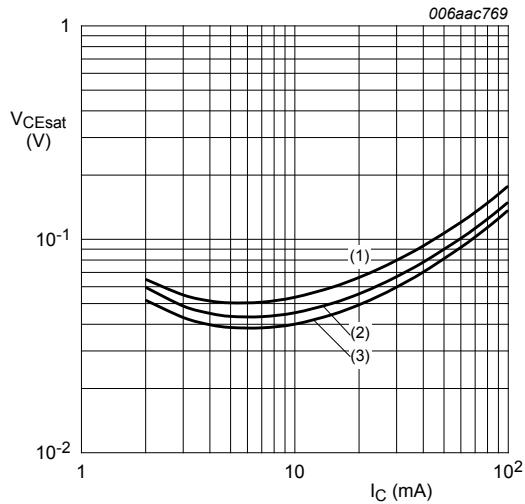
Table 7. Characteristics

| Symbol                                                               | Parameter                            | Conditions                                                                                            | Min | Typ | Max | Unit          |
|----------------------------------------------------------------------|--------------------------------------|-------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| <b>Per transistor, for the PNP transistor with negative polarity</b> |                                      |                                                                                                       |     |     |     |               |
| $I_{CEO}$                                                            | collector-emitter cut-off current    | $V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 25\text{ °C}$                                      | -   | -   | 1   | $\mu\text{A}$ |
|                                                                      |                                      | $V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 150\text{ °C}$                                     | -   | -   | 5   | $\mu\text{A}$ |
| $I_{CBO}$                                                            | collector-base cut-off current       | $V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$                                      | -   | -   | 100 | nA            |
| $I_{EBO}$                                                            | emitter-base cut-off current         | $V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$                                       | -   | -   | 400 | $\mu\text{A}$ |
| $h_{FE}$                                                             | DC current gain                      | $V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ °C}$                                      | 30  | -   | -   |               |
| $V_{CEsat}$                                                          | collector-emitter saturation voltage | $I_C = 10\text{ mA}; I_B = 0.5\text{ mA}; T_{amb} = 25\text{ °C}$                                     | -   | -   | 150 | mV            |
| $V_{I(off)}$                                                         | off-state input voltage              | $V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}; T_{amb} = 25\text{ °C}$                           | -   | 1.1 | 0.8 | V             |
| $V_{I(on)}$                                                          | on-state input voltage               | $V_{CE} = 0.3\text{ V}; I_C = 10\text{ mA}; T_{amb} = 25\text{ °C}$                                   | 2.5 | 1.8 | -   | V             |
| R1                                                                   | bias resistor 1                      | $T_{amb} = 25\text{ °C}$                                                                              | [1] | 7   | 10  | k $\Omega$    |
| R2/R1                                                                | bias resistor ratio                  |                                                                                                       | [1] | 0.8 | 1   |               |
| $C_C$                                                                | collector capacitance                | $V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$  | -   | -   | 2.5 | pF            |
|                                                                      |                                      | $V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$ | -   | -   | 3   | pF            |
| $f_T$                                                                | transition frequency                 | $V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}$                 | [2] | -   | 230 | MHz           |
|                                                                      |                                      | $V_{CE} = -5\text{ V}; I_C = -10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}$               | [2] | -   | 180 | MHz           |

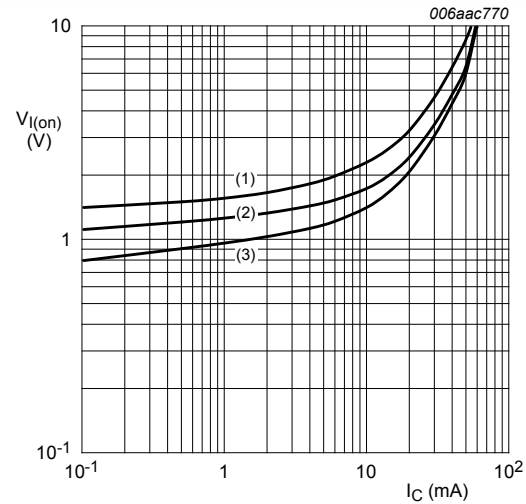
[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.

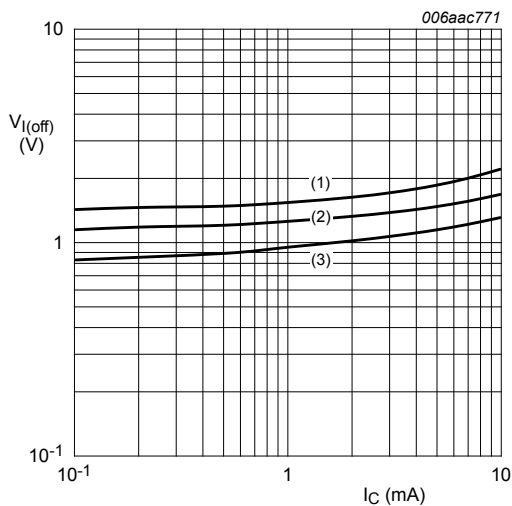




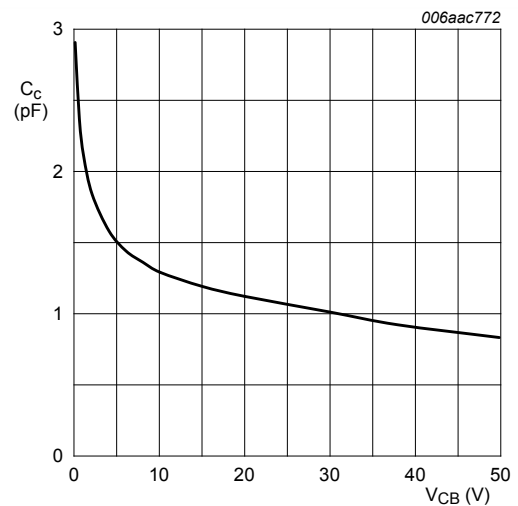
**Fig. 5. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values**



**Fig. 6. NPN transistor: On-state input voltage as a function of collector current; typical values**



**Fig. 7. NPN transistor: Off-state input voltage as a function of collector current; typical values**



**Fig. 8. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values**

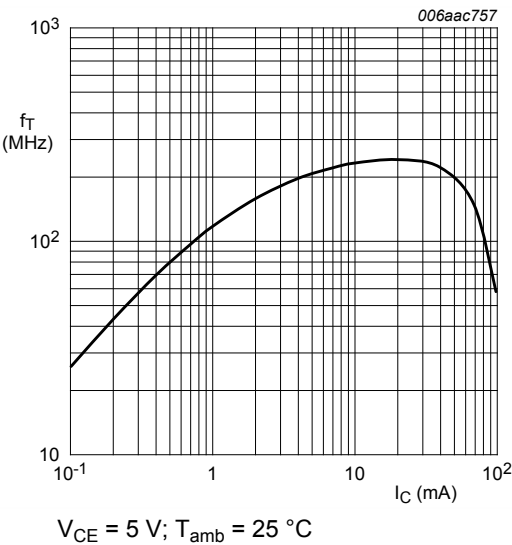


Fig. 9. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor

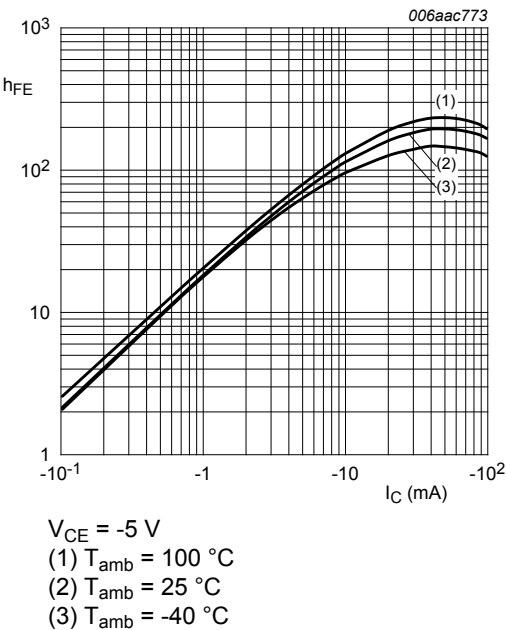


Fig. 10. PNP transistor: DC current gain as a function of collector current; typical values

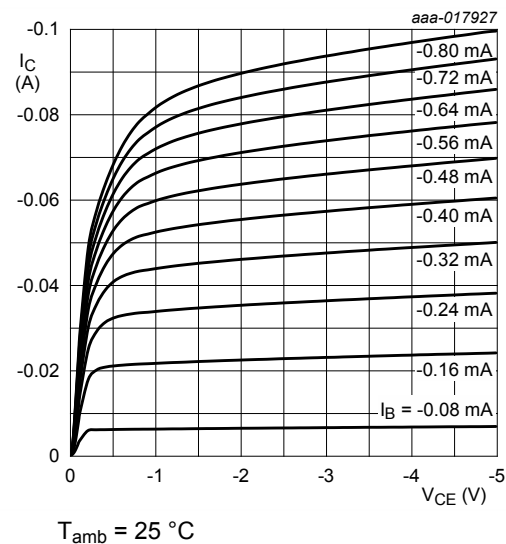


Fig. 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

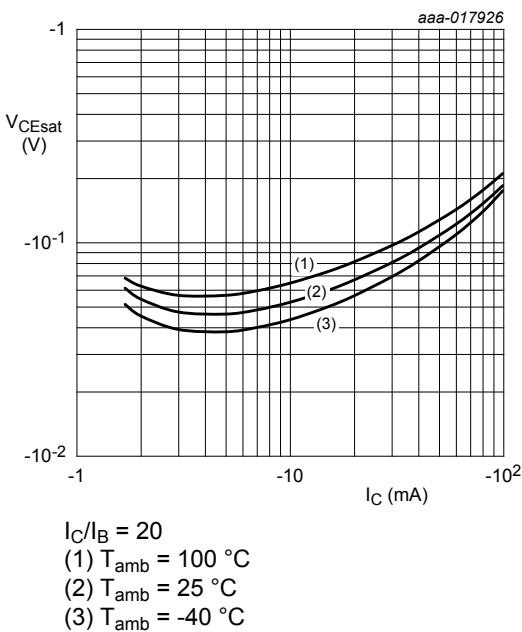


Fig. 12. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

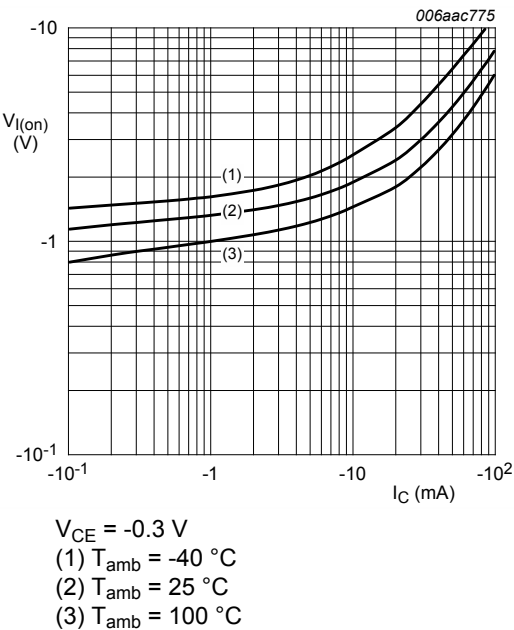


Fig. 13. PNP transistor: On-state input voltage as a function of collector current; typical values

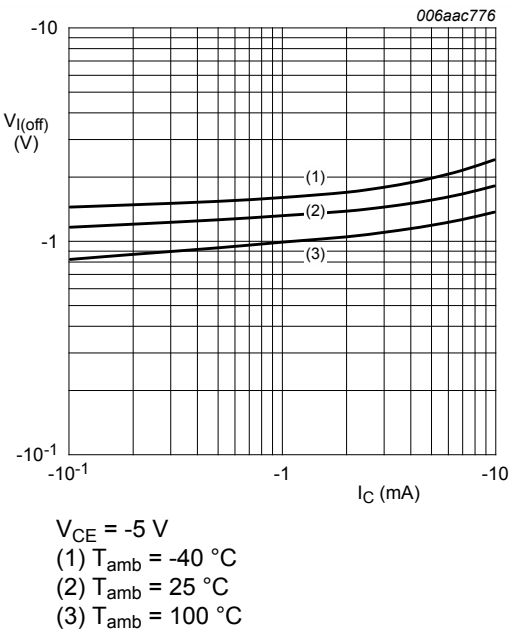


Fig. 14. PNP transistor: Off-state input voltage as a function of collector current; typical values

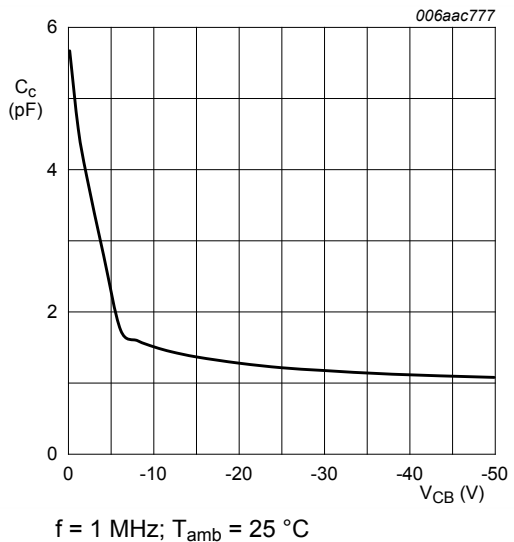


Fig. 15. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values

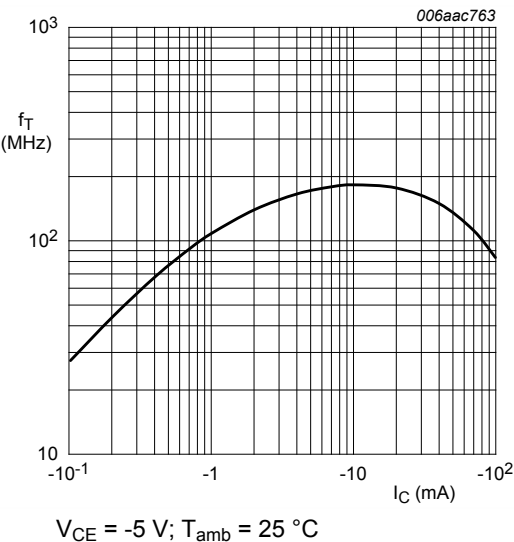


Fig. 16. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

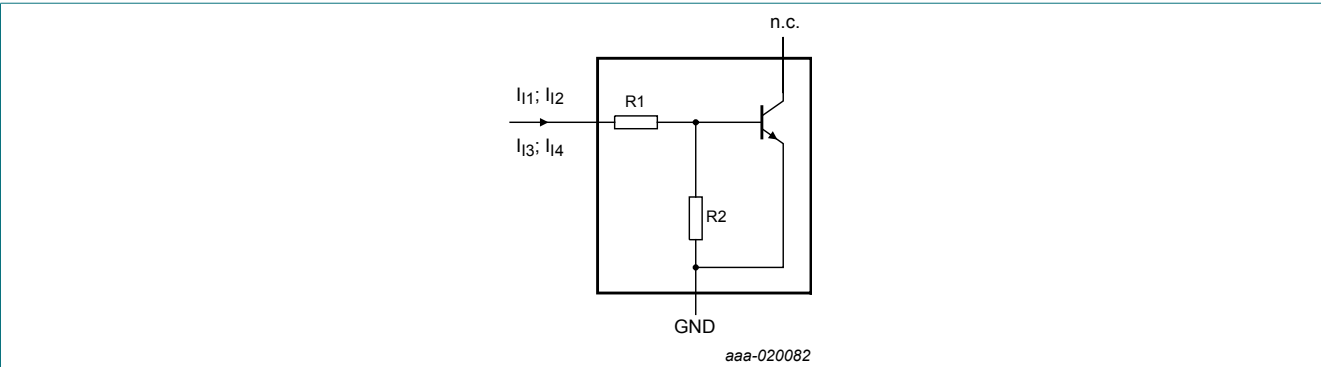


Fig. 17. NPN transistor: Resistor test circuit

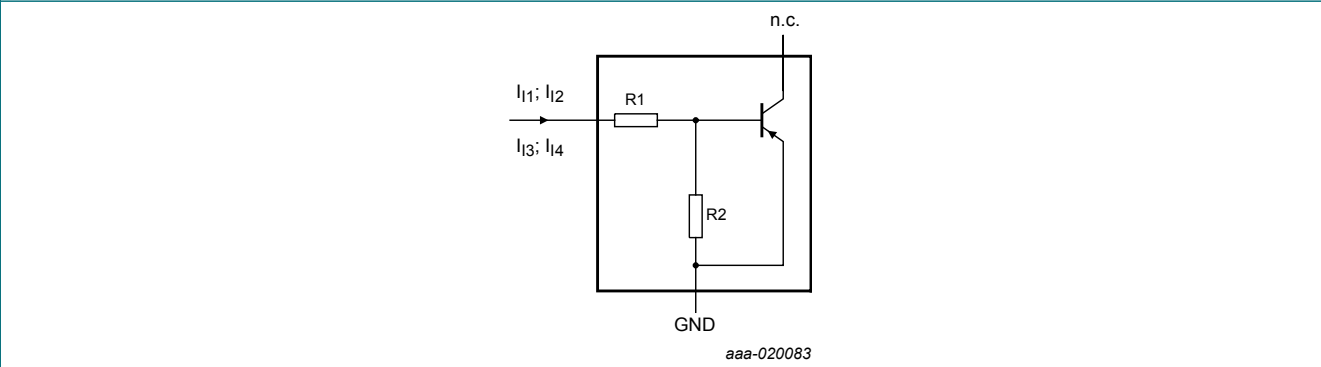


Fig. 18. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Per transistor; for the PNP transistor with negative polarity

| R1 (kΩ) | R2 (kΩ) | Test conditions |                 |                 |                 |
|---------|---------|-----------------|-----------------|-----------------|-----------------|
|         |         | I <sub>I1</sub> | I <sub>I2</sub> | I <sub>I3</sub> | I <sub>I4</sub> |
| 10      | 10      | 350 μA          | 450 μA          | -350 μA         | -450 μA         |

12. Package outline

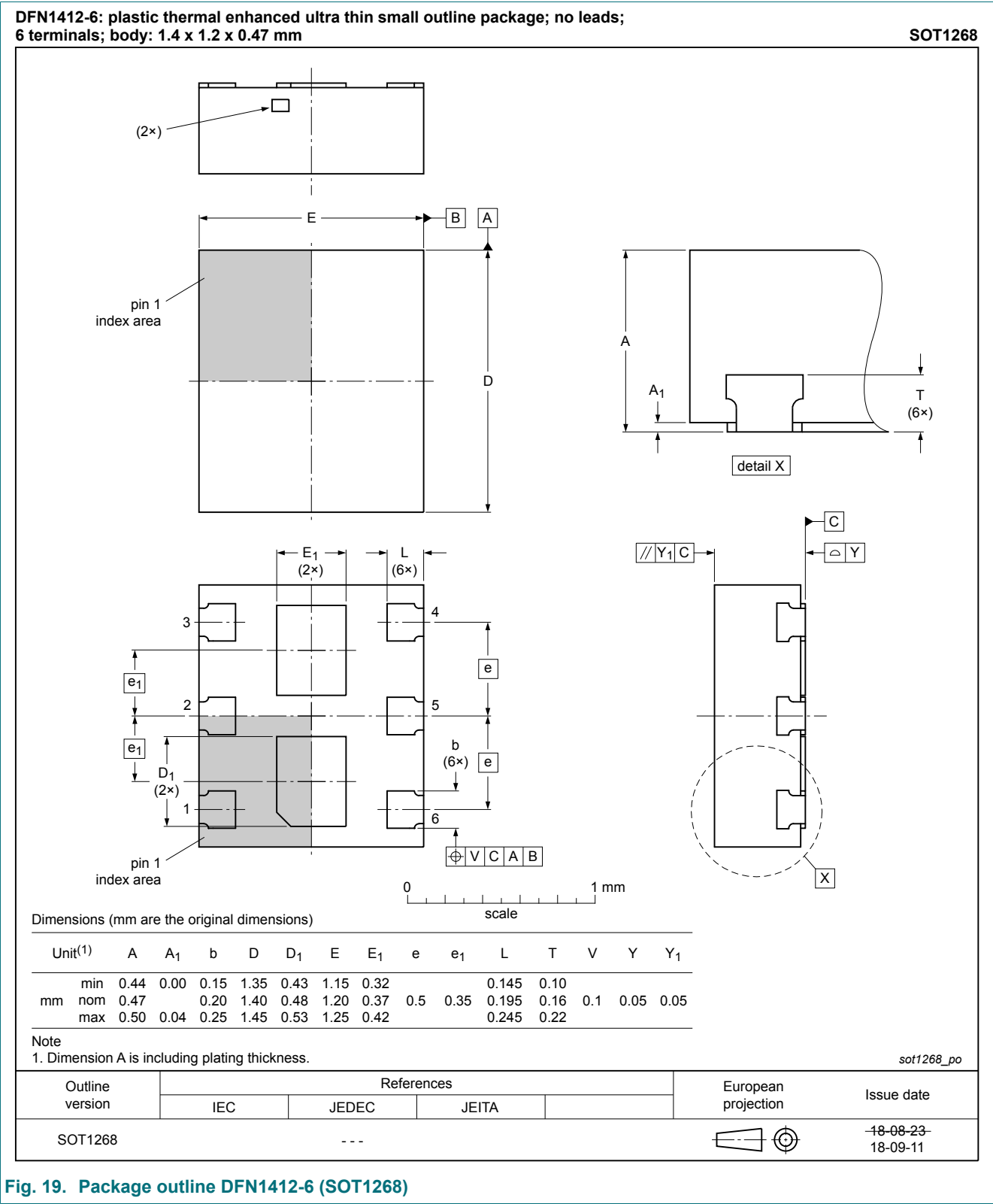


Fig. 19. Package outline DFN1412-6 (SOT1268)

13. Soldering

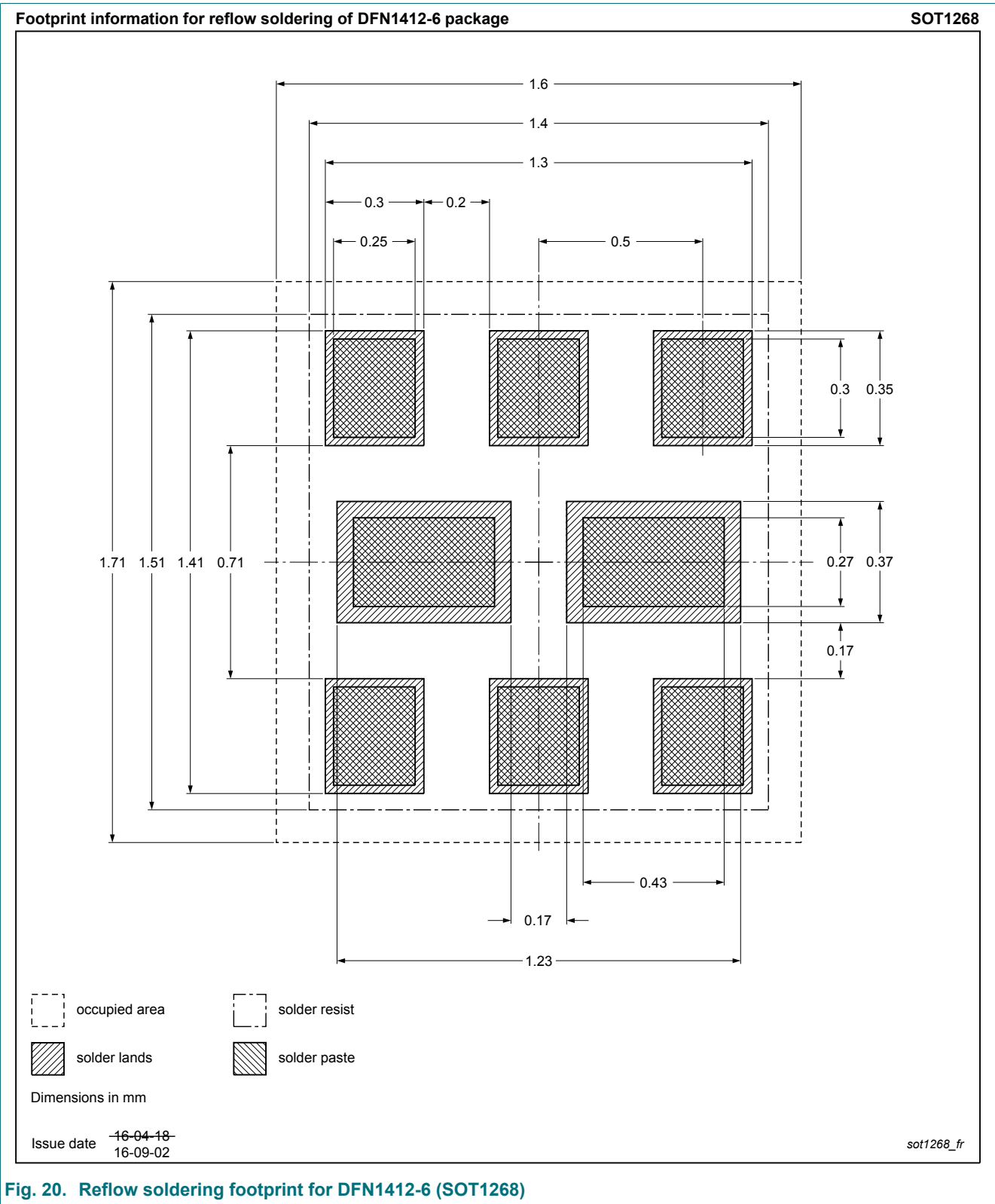


Fig. 20. Reflow soldering footprint for DFN1412-6 (SOT1268)

## 14. Revision history

**Table 9. Revision history**

| Data sheet ID  | Release date                                    | Data sheet status  | Change notice | Supersedes |
|----------------|-------------------------------------------------|--------------------|---------------|------------|
| PRMD3 v.2      | 20180914                                        | Product data sheet | -             | PRMD3 v.1  |
| Modifications: | • Package outline drawing updated: Unit T added |                    |               |            |
| PRMD3 v.1      | 20170615                                        | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 14 September 2018

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- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,  
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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