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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SK4151

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1901-0100

Rev.1.00

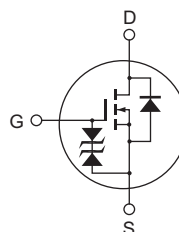
Mar 15, 2010

Features

- Capable of 2.5 V gate drive
- Low drive current
- Low on-resistance
 $R_{DS(on)} = 1.5 \Omega$ typ. (at $I_D = 0.5$ A, $V_{GS} = 4$ V, $T_a = 25^\circ\text{C}$)

Outline

RENESAS Package code: PRSS0003DA-A
(Package name: TO-92(1))



1. Source
2. Drain
3. Gate

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	150	V
Gate to source voltage	V_{GSS}	± 10	V
Drain current	I_D ^{Note1}	1	A
Drain peak current	$I_{D(pulse)}$ ^{Note2}	4	A
Body-drain diode reverse drain current	I_{DR} ^{Note1}	1	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note2}	4	A
Channel dissipation	P_{ch} ^{Note2}	0.75	W
Channel to ambient thermal impedance	θ_{ch-a}	166.7	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 30\%$

2. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	150	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 10	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 150 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.5	1.95	Ω	$I_D = 0.5 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	1.9	2.5	Ω	$I_D = 0.5 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	98	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	31	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	14	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	3.5	—	nC	$V_{DD} = 100 \text{ V}$
Gate to source charge	Q_{gs}	—	0.5	—	nC	$V_{GS} = 4 \text{ V}$
Gate to drain charge	Q_{gd}	—	1.8	—	nC	$I_D = 1 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	8	—	ns	$V_{GS} = 4 \text{ V}$
Rise time	t_r	—	12	—	ns	$I_D = 0.5 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	34	—	ns	$R_L = 60 \text{ }\Omega$
Fall time	t_f	—	19	—	ns	
Body-drain diode forward voltage	V_{DF}	—	1.0	1.5	V	$I_F = 1 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	60	—	ns	$I_F = 1 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

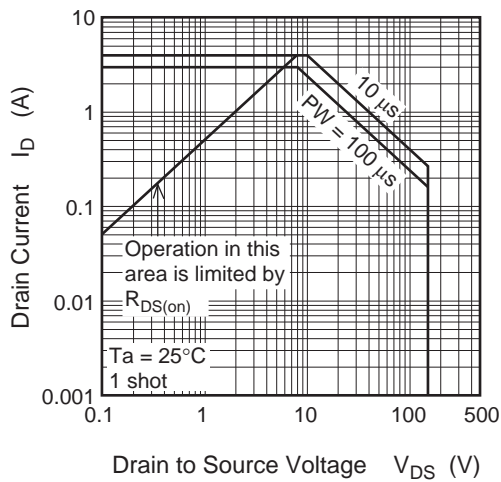
Notes: 3. Pulse test

4. This device is sensitive to electrostatic discharge.

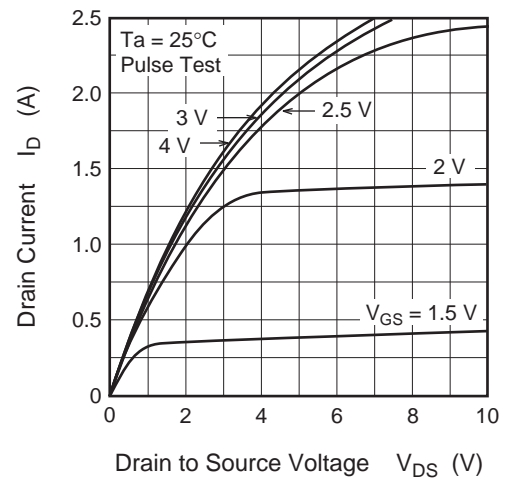
It is recommended to adopt appropriate cautions when handling this product.

Main Characteristics

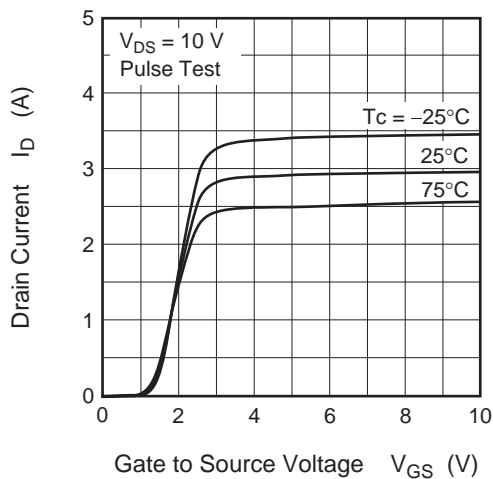
Maximum Safe Operation Area



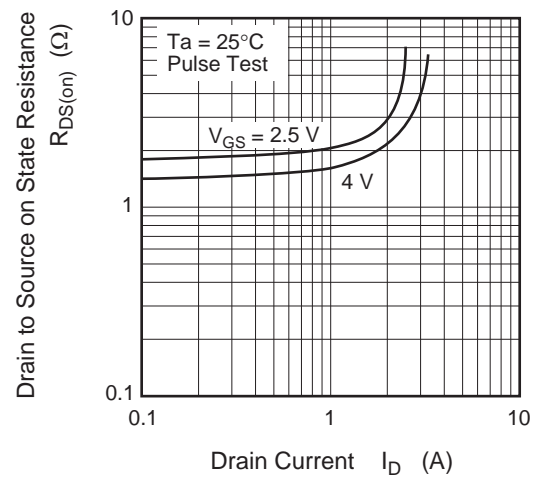
Typical Output Characteristics



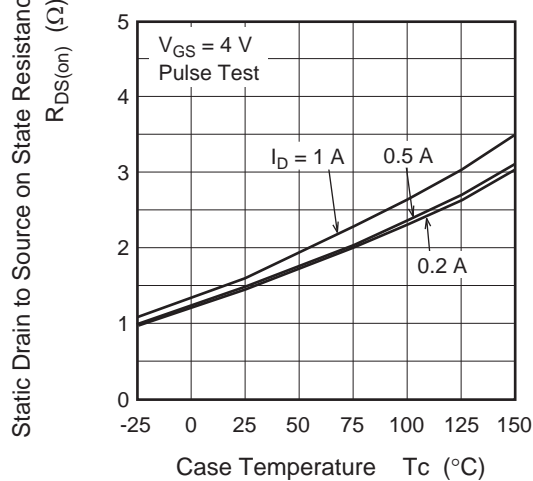
Typical Transfer Characteristics



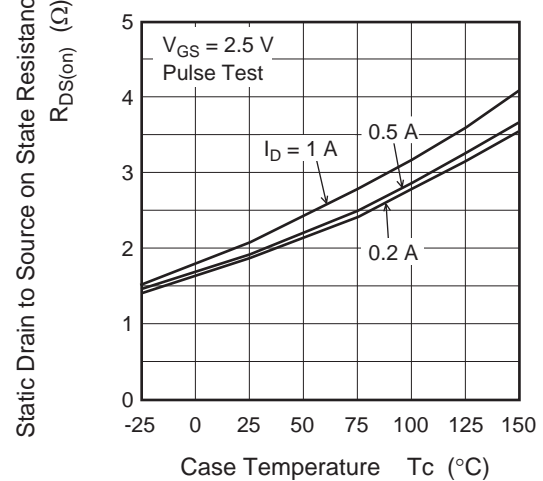
Static Drain to Source on State Resistance vs. Drain Current (Typical)



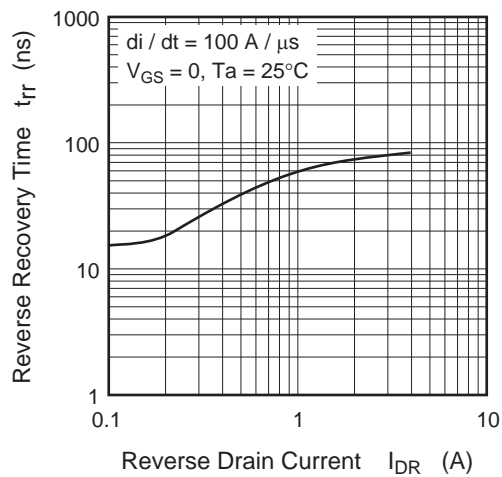
Static Drain to Source on State Resistance vs. Temperature (Typical) (1)



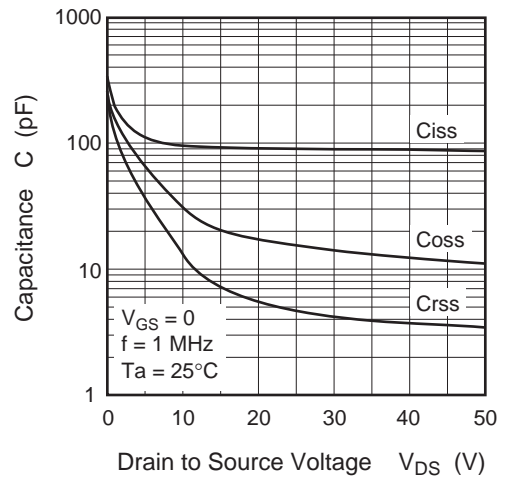
Static Drain to Source on State Resistance vs. Temperature (Typical) (2)



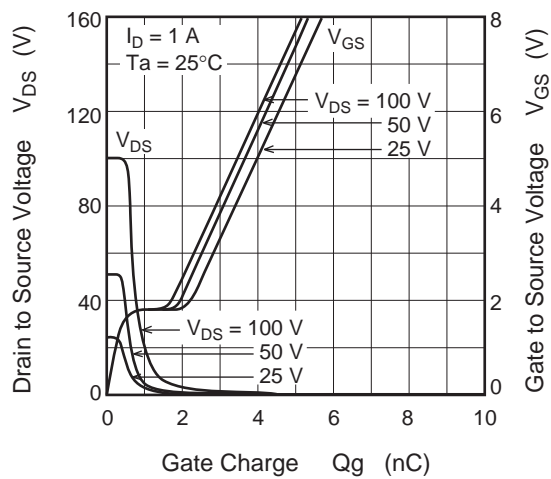
Body-Drain Diode Reverse Recovery Time (Typical)



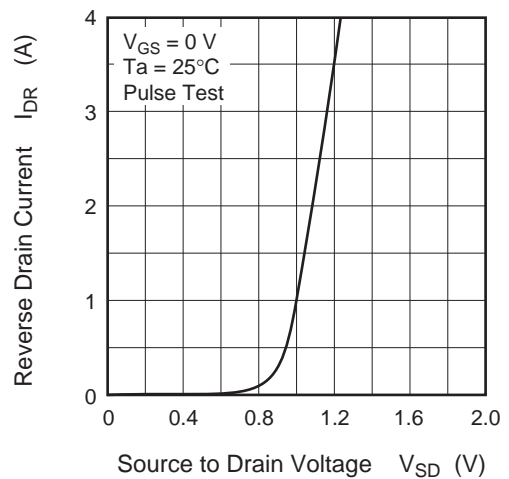
Typical Capacitance vs. Drain to Source Voltage



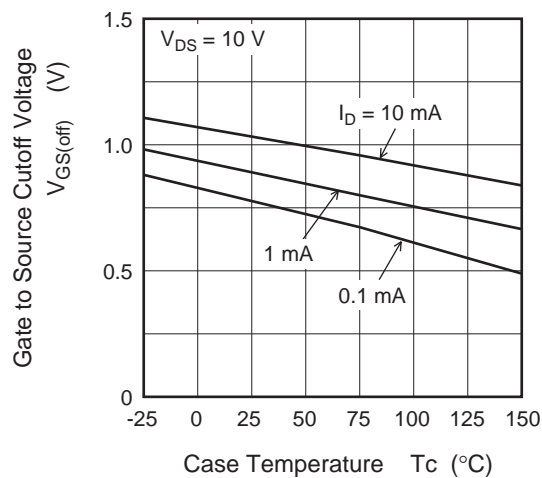
Dynamic Input Characteristics (Typical)

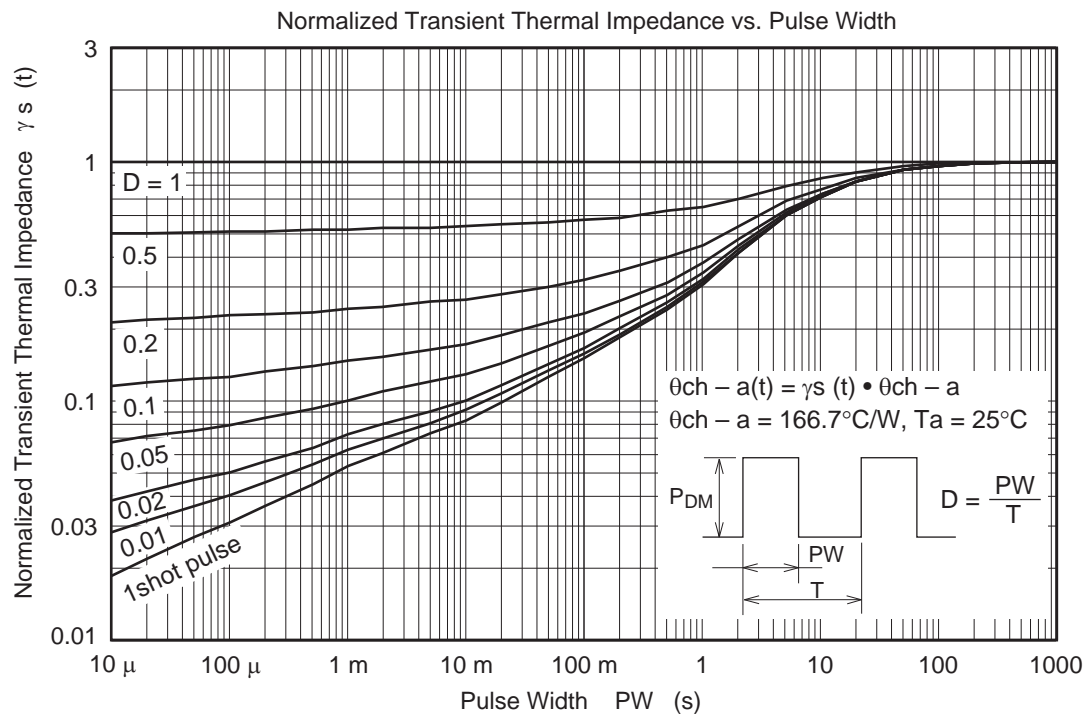


Reverse Drain Current vs. Source to Drain Voltage (Typical)

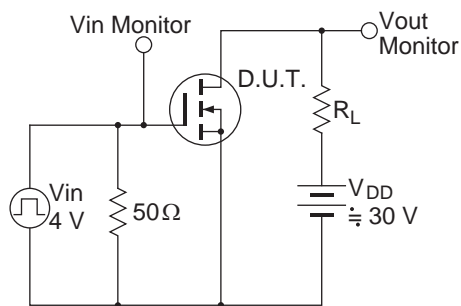


Gate to Source Cutoff Voltage vs. Case Temperature (Typical)

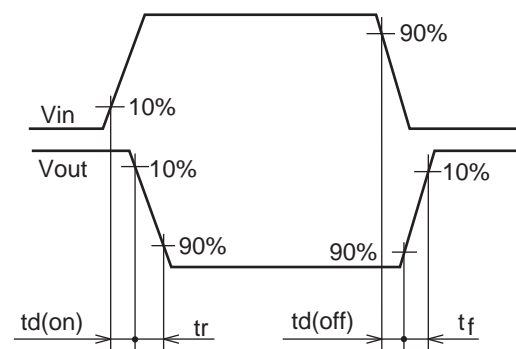




Switching Time Test Circuit



Waveform



Unit: mm

Note: Leads is forming applied as following figure.



Notes:

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