

PL602041



ClockWorks™ PCIe Quad Outputs Ultra-Low Jitter, HCSL Frequency Synthesizer

General Description

The PL602041 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for PCI Express clock signals.

The device operates from a 3.3V or 2.5V power supply and synthesizes four HCSL output clocks at 25MHz, 100MHz, 125MHz, and 200MHz. The PL602041 accepts a 25MHz crystal.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

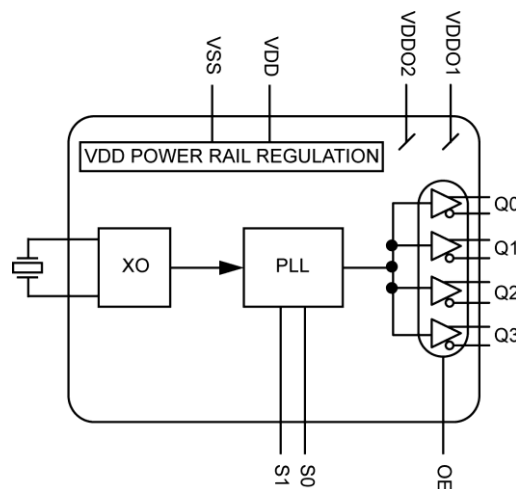
Features

- Input crystal frequency of 25MHz
- Generates four HCSL clock outputs at 25MHz, 100MHz, 125MHz, and 200MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 100MHz (1.875MHz to 20MHz): 105fs
- Compliant with PCI Express Gen1, Gen2, and Gen3
- Industrial temperature range (–40°C to +85°C)
- RoHS and PFOS compliant
- Available in 24-pin 4mm x 4mm QFN package

Applications

- Servers
- Storage systems
- Switches and routers
- Gigabit Ethernet
- Set-top boxes/DVRs

Block Diagram



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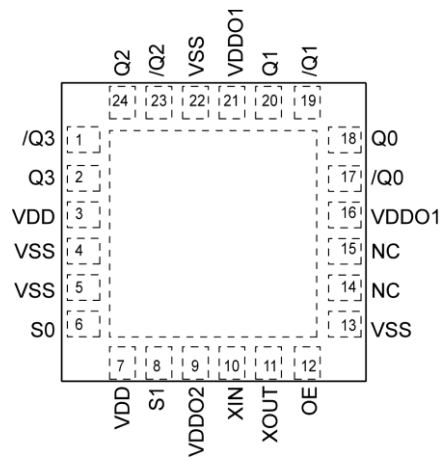
Ordering Information⁽¹⁾

| Part Number | Marking | Shipping | Junction Temperature Range | Package | Lead Finish |
|----------------|--------------|---------------|----------------------------|------------|-------------|
| PL602041UMG | PL602 041 | Tube | -40°C to +85°C | 24-Pin QFN | NiPdAu |
| PL602041UMG TR | PL602 041 | Tape and Reel | -40°C to +85°C | 24-Pin QFN | NiPdAu |

Note:

1. Devices are RoHS and PFOS compliant.

Pin Configuration



**24-Pin QFN
(Top View)**

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Function |
|------------------|--------------------|----------|-----------|--|
| 17, 18 19, 20 | /Q0, Q0 /Q1, Q1 | O, (DIF) | HCSL | Differential Clock Outputs Pairs. |
| 23, 24 1, 2 | /Q2, Q2 /Q3, Q3 | O, (DIF) | HCSL | Differential Clock Outputs Pairs. |
| 9 | VDDO2 | PWR | | Power Supply. |
| 16, 21 | VDDO1 | PWR | | Power Supply. |
| 3, 7 | VDD | PWR | | Core Power Supply. |
| 4, 5, 13, 22 | VSS | PWR | | Power Supply Ground. |
| 6, 8 | S0, S1 | I | LVC MOS | Frequency Select for 25MHz, 100MHZ, 125MHZ, and 200MHZ. Each pin has a 45KΩ pull-up. |
| 10 | XIN | I, (SE) | Crystal | Crystal Input, no load caps needed (see Figure 5). |
| 11 | XOUT | O, (SE) | Crystal | Crystal Output, no load caps needed (see Figure 5). |
| 12 | OE | I, (SE) | LVC MOS | Output Enable/Disable. |
| 14, 15 | NC | | | No Connect. |

Absolute Maximum Ratings⁽²⁾

| | |
|--|---------------------------|
| Supply Voltage (V_{DD} , $V_{DDO1/2}$) | +4.6V |
| Input Voltage (V_{IN}) | -0.50V to $V_{DD} + 0.5V$ |
| Lead Temperature (soldering, 20s) | 260°C |
| Case Temperature | 115°C |
| Storage Temperature (T_S) | -65°C to +150°C |

Operating Ratings⁽³⁾

| | |
|--|--------------------|
| Supply Voltage (V_{DD} , $V_{DDO1/2}$) | +2.375V to +3.465V |
| Ambient Temperature (T_A) | -40°C to +85°C |
| Junction Thermal Resistance ⁽⁴⁾ | |
| QFN (θ_{JA}) Still Air | 50°C/W |
| QFN (ψ_{JB}) Junction-to-Board | 30°C/W |

DC Electrical Characteristics⁽⁵⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------------------|--------------------------------------|-------------------------|-------|------|-------|-------|
| V_{DD} , $V_{DDO1/2}$ | 2.5V Operating Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DD} , $V_{DDO1/2}$ | 2.5V Operating Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Supply Current to $V_{DD} + V_{DDO}$ | Outputs 50Ω to V_{SS} | | 150 | 185 | mA |

HCSL DC Electrical Characteristics⁽⁵⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. $R_L = 50\Omega$ to V_{SS}

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------|------------------------|-----------|------|------|------|-------|
| V_{OH} | Output High Voltage | | 660 | 700 | 850 | mV |
| V_{OL} | Output Low Voltage | | -150 | 0 | 27 | mV |
| V_{CROSS} | Crossing Point Voltage | | 250 | 350 | 550 | mV |

LVC MOS (S0, S1) DC Electrical Characteristics⁽⁶⁾

$V_{DD} = 3.3V \pm 5\%$, or $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|-----------------------------------|------|------|----------------|-------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -150 | | | μA |

Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- The datasheet limits are not guaranteed if the device is operated beyond operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
- The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.
- All phase noise measurements were taken with an Agilent 5052B phase noise system.

Crystal Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------------------------|-----------------------|--------------------------------|------|------|----------|
| Mode of Oscillation | 10pF load capacitance | Fundamental, Parallel Resonant | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitor, C0 | | | 1 | 5 | pF |
| Correlation Drive Level | | | 10 | 100 | μ W |

AC Electrical Characteristics^(6, 7)

$$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\% \text{ or } 2.5V \pm 5\%$$

$$V_{DD} = 3.3V \pm 5\%, V_{DDO1/2} = 3.3V \pm 5\% \text{ or } 2.5V \pm 5\%$$

$$T_A = -40^\circ\text{C to } +85^\circ\text{C. } R_L = 50\Omega \text{ to } V_{SS}$$

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------------------------------|---------------------------------|---|------|----------------------------|------|-------|
| F _{OUT} | Output Frequency | | | 25, 100, 125, 200 | | MHz |
| F _{REF} | Crystal Input Frequency | | | 25 | | MHz |
| T _R /T _F | HCSL Output Rise/Fall Time | 20% – 80% | 150 | 300 | 450 | ps |
| ODC | Output Duty Cycle | | 48 | 50 | 52 | % |
| T _{SKEW} | Output-to-Output Skew | Note 7 | | | 45 | ps |
| T _{LOCK} | PLL Lock Time | | | | 20 | ms |
| T _{JIT} (\emptyset) | RMS Phase Jitter ⁽⁸⁾ | 100MHz Integration Range (1.875MHz–20MHz) Integration Range (12kHz–20MHz) | | 105 250 | | fs |

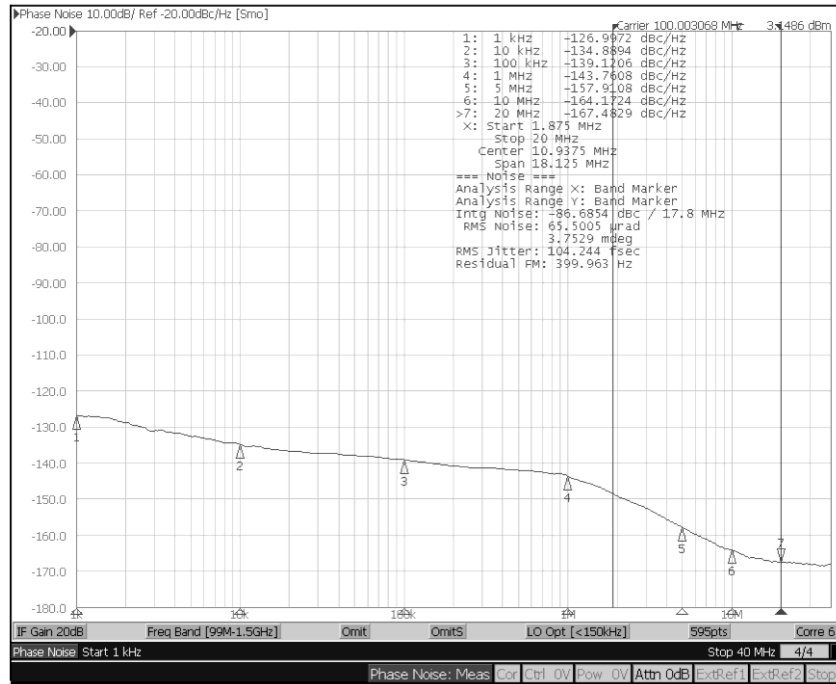
Notes:

7. Defined as skew between outputs at the same supply voltage and with equal load conditions; measured at the output differential crossing points.
8. Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

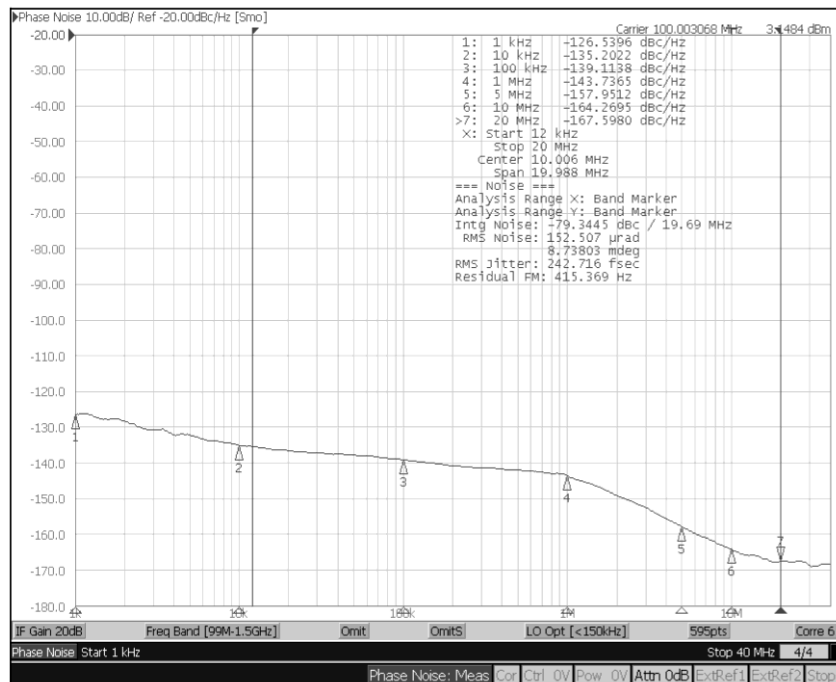
Truth Tables

| S1 | S0 | OUTPUT |
|----|----|--------|
| 0 | 0 | 25MHz |
| 0 | 1 | 100MHz |
| 1 | 0 | 125MHz |
| 1 | 1 | 200MHz |

Phase Noise Plots



Phase Noise Plot: 100MHz, 1.875MHz–20MHz 104fs



Phase Noise Plot: 100MHz, 12kHz–20MHz 242fs

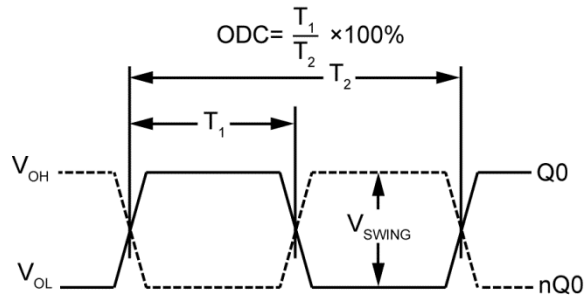


Figure 1. Duty Cycle Timing

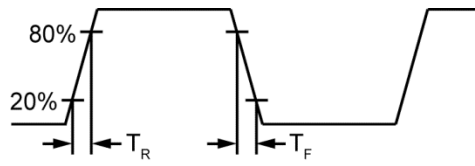
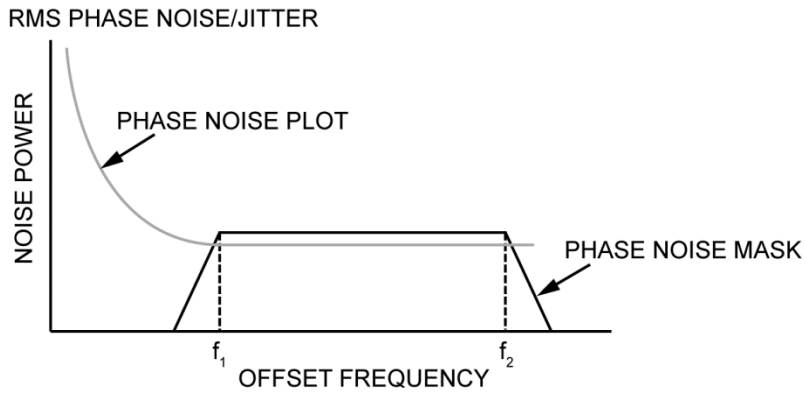


Figure 2. All Outputs Rise/Fall Time



$RMS\ JITTER = \sqrt{\text{AREA UNDER THE MASKED PHASE NOISE PLOT}}$

Figure 3. RMS Phase/Noise Jitter

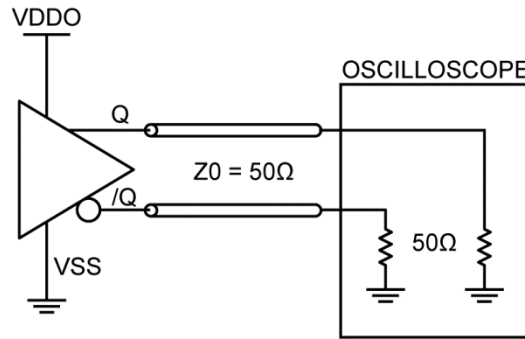


Figure 4. HCSL Output Load and Test Circuit

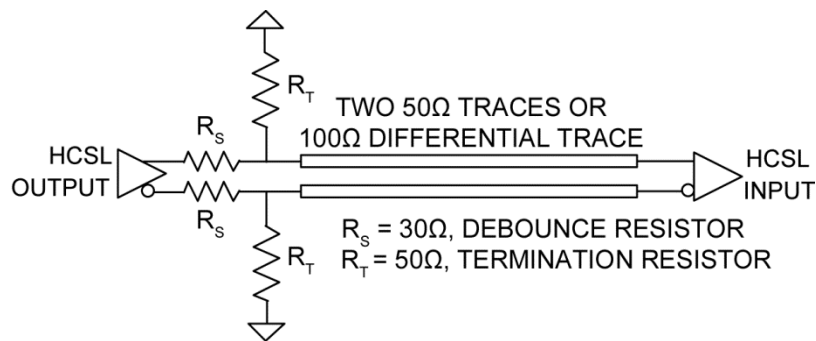


Figure 5. HCSL Recommended Application Termination (Source Terminated)

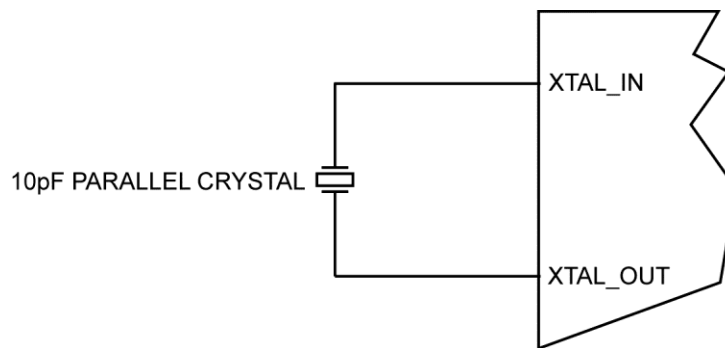


Figure 6. Crystal Input Interface

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for more details.

Contact Micrel's HBW applications group at: tcghelp@micrel.com if you need help selecting a suitable crystal for your application.

Power Supply and Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the PL602041.

The impedance value of the Ferrite Bead (FB) needs to be between 240Ω and 600Ω with a saturation current ≥150mA.

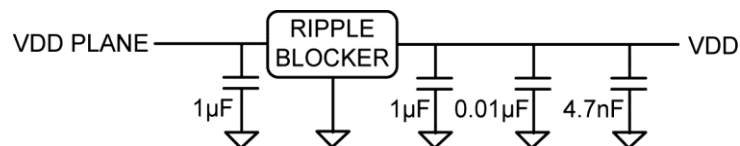
VDDO1 and VDDO2 pins connect directly to the VDD plane. All VDD pins on the PL602041 connect to VDD after the power supply filter.

HCSL Outputs

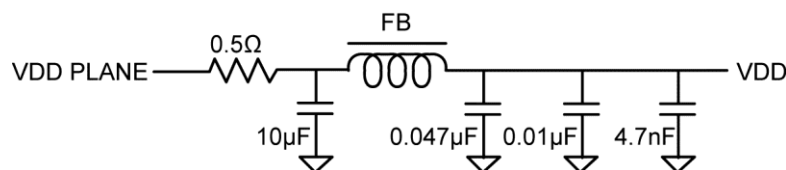
HCSL outputs are to be terminated with 50Ω to VSS. For best performance load all outputs. If you want to AC-couple or change the termination, contact Micrel's application group: tcghelp@micrel.com (see Figure 5).

Power Supply Filtering Recommendations

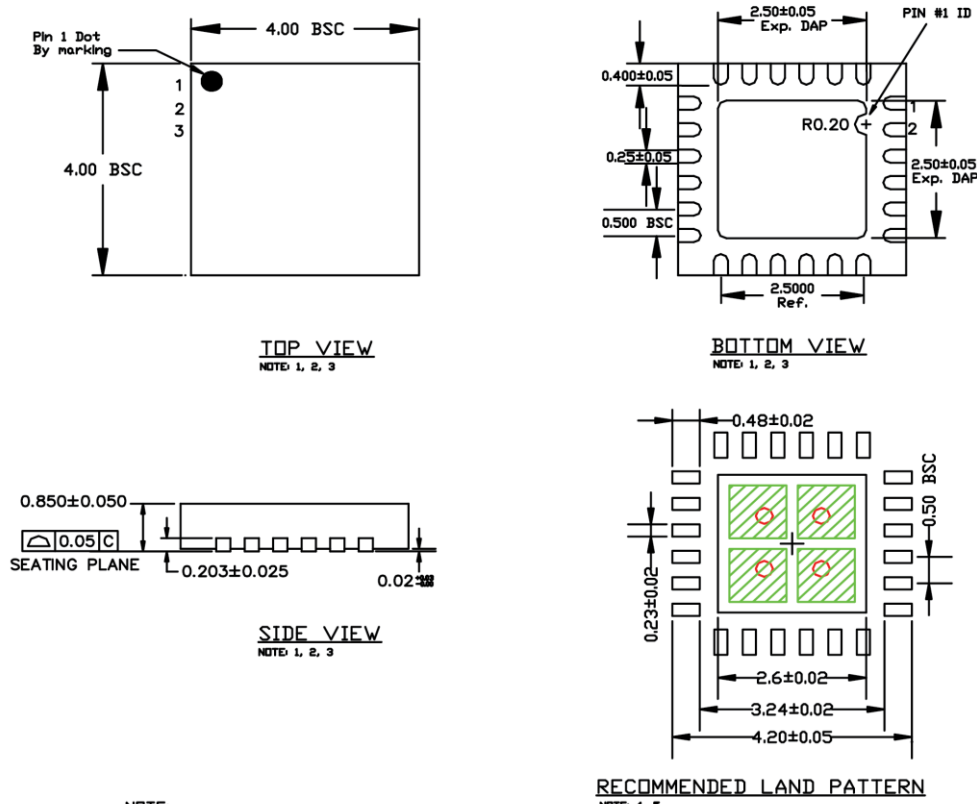
Preferred filter, using Micrel MIC94300 or MIC94310 Ripple Blocker™:



Alternative, traditional filter, using a ferrite bead:



Package Information⁽⁹⁾



NOTE:
 1. MAX PACKAGE WARPAGE IS 0.05 MM
 2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
 3. PIN #1 IS ON TOP WILL BE LASER MARKED
 4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
 5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

24-Pin Package Type (QFN)

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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