

16-Channel (2 Banks of 8-Channels), High Voltage, Analog Switch With Bleed Resistors

Features

- ▶ HVCMOS® technology for high performance
- ▶ 220V operating conditions
- ▶ 22Ω typical output on-resistance
- ▶ Integrated bleed resistors on the outputs
- ▶ 3.3V and 5.0V CMOS logic compatibility
- ▶ Very low quiescent power dissipation (-10μA)
- ▶ -45dB min off isolation at 7.5MHz
- ▶ Low parasitic capacitance
- ▶ Excellent noise immunity
- ▶ Flexible operating supply voltages
- ▶ 48-lead LQFP package

Applications

- ▶ Medical ultrasound imaging
- ▶ Non-destructive evaluation

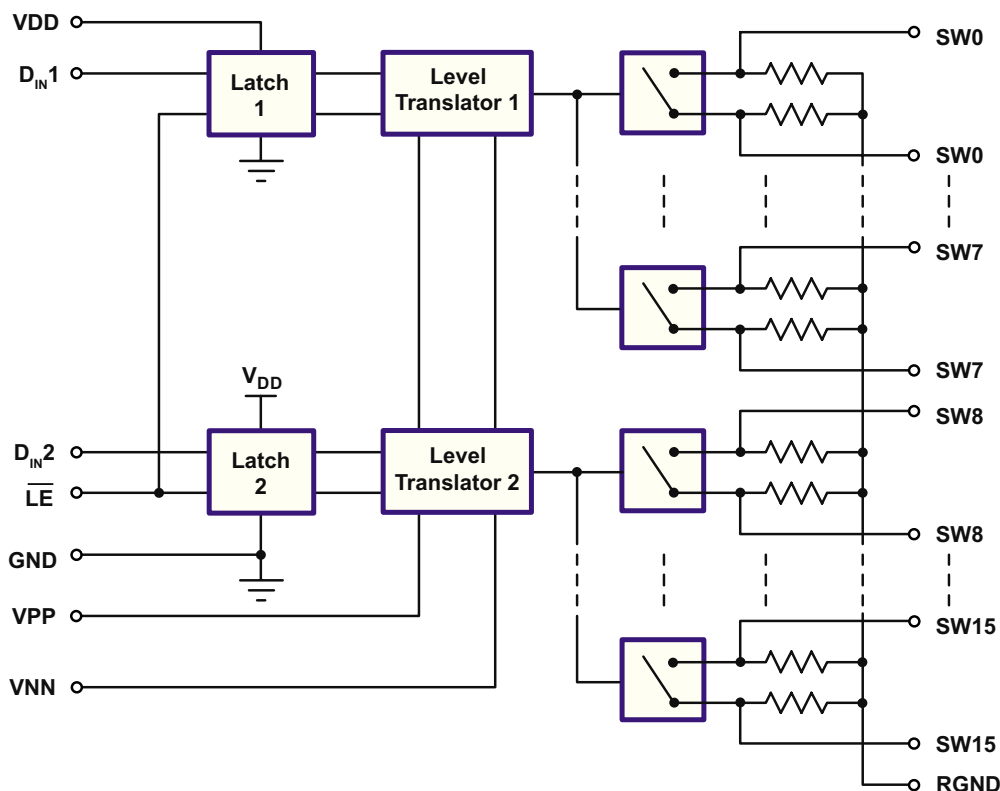
General Description

The Supertex HV2731 is a 220V, 16-channel, high voltage, analog switch integrated circuit (IC) with output bleed resistors (R_{INT}). The output switches are configured as 2 sets of 8 single pole, single throw analog switches. The IC is intended to be used in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging.

The 2 sets of 8 analog switches are controlled by 2 input logic controls, D_{IN1} and D_{IN2} . A logic high on D_{IN1} will turn on switches 0 to 7 and a logic high on D_{IN2} will turn on switches 8 to 15. The bleed resistors help to significantly reduce voltage built up on capacitive loads such as piezoelectric transducers connected to the outputs.

Using HVCMOS® technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Block Diagram



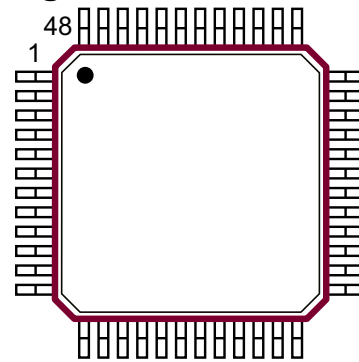
Ordering Information

| Device | 48-Lead LQFP 7.00x7.00mm body 1.60mm height (max) 0.50mm pitch |
|--------|---|
| HV2731 | HV2731FG-G |

-G indicates package is RoHS compliant ("Green")



Pin Configuration



48-Lead LQFP (FG)
(top view)

Absolute Maximum Ratings

| Parameter | Value |
|---|-------------------------|
| V_{DD} logic supply | -0.5V to +7.0V |
| V_{PP} - V_{NN} differential supply | 225V |
| V_{PP} positive supply | -0.5V to V_{NN} +225V |
| V_{NN} negative supply | +0.5V to -225V |
| Logic input voltage | -0.5V to V_{DD} +0.3V |
| Analog signal range | V_{NN} to V_{PP} |
| Peak analog signal current/channel | 2.5A |
| Storage temperature | -65°C to 150°C |
| Power dissipation | 1.0W |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

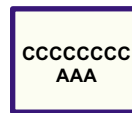
Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number

Bottom Marking



C = Country of Origin*
A = Assembler ID*
— = "Green" Packaging

*May be part of top marking

Package may or may not include the following marks: Si or

48-Lead LQFP (FG)

Recommended Operating Conditions

| Sym | Parameter | Value |
|-----------|------------------------------------|--------------------------------|
| V_{DD} | Logic power supply voltage | 3.0V to 5.5V |
| V_{PP} | Positive driver supply | +50V to +110V |
| V_{NN} | Negative high voltage supply | -10V to V_{PP} -220V |
| V_{IH} | High level input voltage | V_{DD} -1.0V to V_{DD} |
| V_{IL} | Low-level input voltage | 0V to 1.0V |
| V_{SIG} | Analog signal voltage peak-to-peak | V_{NN} +10V to V_{PP} -10V |
| T_A | Operating free air temperature | 0°C to 70°C |

Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
- Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0msec.

DC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Units | Conditions |
|----------------------|--|-----|------|-------|-----|------|-------|------|-------|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| R _{ONS} | Small signal switch on-resistance | - | 30 | - | 26 | 32 | - | 40 | Ω | V _{SIG} = 0V, I _{SIG} = 5.0mA, V _{PP} = +50V, V _{NN} = -170V |
| | | - | 25 | - | 22 | 27 | - | 35 | | V _{SIG} = 0V, I _{SIG} = 200mA, V _{PP} = +50V, V _{NN} = -170V |
| | | - | 25 | - | 22 | 27 | - | 30 | | V _{SIG} = 0V, I _{SIG} = 5.0mA, V _{PP} = +110V, V _{NN} = -110V |
| | | - | 20 | - | 18 | 22 | - | 25 | | V _{SIG} = 0V, I _{SIG} = 200mA, V _{PP} = +110V, V _{NN} = -110V |
| ΔR _{ONS} | Small signal switch on-resistance matching | - | 20 | - | 5.0 | 20 | - | 20 | % | V _{SIG} = 0V, I _{SIG} = 5.0mA, V _{PP} = +110V, V _{NN} = -110V |
| R _{ONL} | Large signal switch on-resistance | - | - | - | 15 | - | - | - | Ω | V _{SIG} = 0V, I _{SIG} = 1.0A |
| R _{INT} | Output switch shunt resistance | - | - | 20 | 35 | 50 | - | - | KΩ | Output switch to R _{GND} I _{RINT} = 0.5mA |
| I _{SOL} | Switch off-leakage per switch | - | 5.0 | - | 1.0 | 10 | - | 15 | μA | V _{SIG} = V _{PP} -10V, V _{NN} = +10V |
| V _{OS(OFF)} | DC offset switch off | - | 300 | - | 100 | 300 | - | 300 | mV | No load |
| V _{OS(ON)} | DC offset switch on | - | 500 | - | 100 | 500 | - | 500 | | |
| I _{PPQ} | Quiescent V _{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches off |
| I _{NNQ} | Quiescent V _{NN} supply current | - | - | - | -10 | -50 | - | - | | |
| I _{PPQ} | Quiescent V _{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches on, I _{SW} = 5.0mA |
| I _{NNQ} | Quiescent V _{NN} supply current | - | - | - | -10 | -50 | - | - | | |
| I _{SW} | Switch output peak current | - | 2.0 | - | - | 2.0 | - | 2.0 | A | V _{SIG} duty cycle < 0.1% |
| f _{SW} | Output switching frequency | - | - | - | - | 50 | - | - | kHz | Duty cycle = 50% |
| I _{PP} | Average V _{PP} supply current | - | 8.1 | - | - | 8.8 | - | 10 | mA | V _{PP} = 50V, V _{NN} = -170V, All switches turning on and off at 50kHz |
| I _{NN} | Average V _{NN} supply current | - | -8.1 | - | - | -8.8 | - | -10 | | |
| I _{PP} | Average V _{PP} supply current | - | 8.1 | - | - | 6.3 | - | 6.9 | mA | V _{PP} = 110V, V _{NN} = -110V, All switches turning on and off at 50kHz |
| I _{NN} | Average V _{NN} supply current | - | -8.1 | - | - | -6.3 | - | -6.9 | | |
| I _{DDQ} | Quiescent V _{DD} supply current | - | 10 | - | - | 10 | - | 10 | μA | All logic inputs are static |
| I _{DD} | Average V _{DD} supply current | - | 2.0 | - | - | 2.0 | - | 2.0 | mA | D _{IN1} = D _{IN2} = 3.0MHz, LE = high |
| C _{IN} | Logic input capacitance | - | 10 | - | - | 10 | - | 10 | pF | --- |

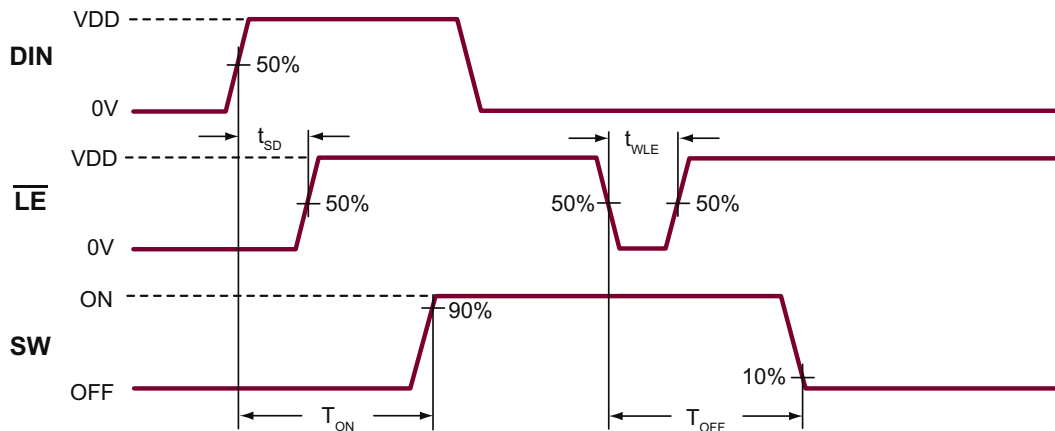
AC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Units | Conditions |
|-------------------|--|-----|-----|-------|-----|-----|-------|-----|-------|------------|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| t _{WLE} | Time width of \overline{LE} | 150 | - | 150 | - | - | 150 | - | ns | --- |
| t _{WDIN} | Time width of D _{IN} | 150 | - | 150 | - | - | 150 | - | ns | --- |
| t _{SD} | Set up time before \overline{LE} rises | 150 | - | 150 | - | - | 150 | - | ns | --- |

AC Electrical Characteristics (cont.) (Over recommended operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Units | Conditions |
|----------------------|---------------------------------------|-----|-----|-------|-----|-----|-------|-----|-------|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| t _{ON} | Turn on time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | V _{SIG} = V _{PP} -10V, R _{LOAD} = 10KΩ |
| t _{OFF} | Turn off time | - | 5.0 | - | - | 5.0 | - | 5.0 | | |
| dv/dt | Maximum V _{SIG} slew rate | - | 20 | - | - | 20 | - | 20 | V/ns | --- |
| K _O | Off isolation | -30 | - | -30 | -33 | - | -30 | - | dB | f = 5.0MHz, load = 1.0KΩ//15pF |
| | | -45 | - | -45 | -50 | - | -45 | - | | f = 7.5MHz, R _{LOAD} = 50Ω |
| K _{CR} | Switch crosstalk | -45 | - | -45 | - | - | -45 | - | dB | f = 5.0MHz, R _{LOAD} = 50Ω |
| I _{ID} | Output switch isolation diode current | - | 300 | - | - | 300 | - | 300 | mA | 300ns pulse width, 2.0% duty cycle |
| C _{SG(OFF)} | Off capacitance SW to GND | 5.0 | 17 | 5.0 | 12 | 17 | 5.0 | 17 | pF | V _{SIG} = 0V, f = 1.0MHz |
| C _{SG(ON)} | On capacitance SW to GND | 25 | 50 | 25 | 38 | 50 | 25 | 50 | pF | V _{SIG} = 0V, f = 1.0MHz |
| +V _{SPK} | Output voltage spike | - | - | - | 250 | - | - | - | mV | R _{LOAD} = 50Ω |
| -V _{SPK} | | - | - | - | 500 | - | - | - | | |
| QC | Charge injection | - | - | - | 770 | - | - | - | PC | V _{PP} = +50V, V _{NN} = -170V |
| | | - | - | - | 620 | - | - | - | | V _{PP} = +110V, V _{NN} = -110V |

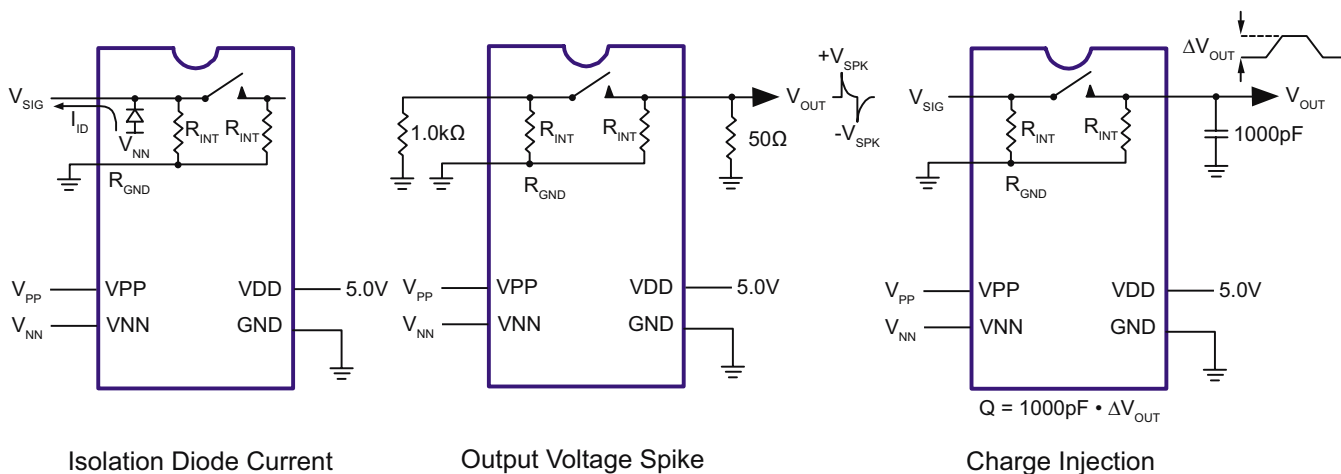
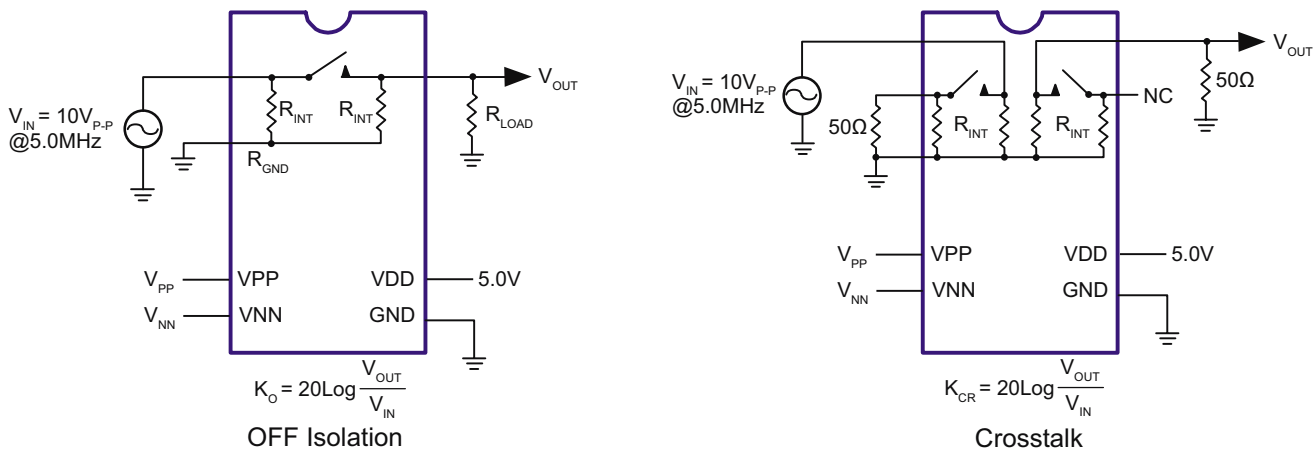
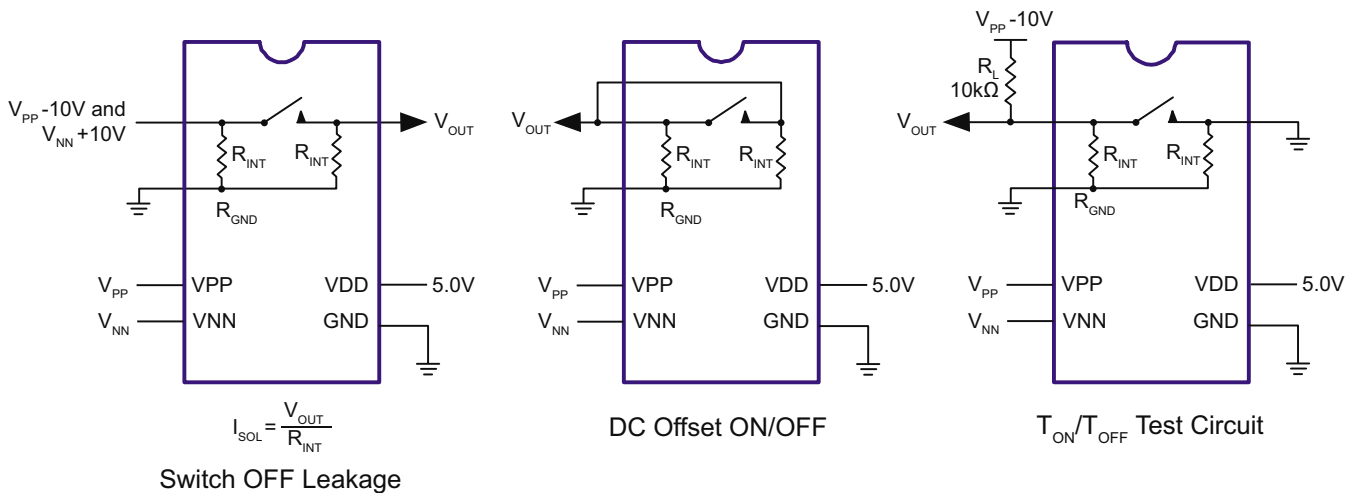
Logic Timing Waveforms



Truth Table

| DIN2 | DIN1 | LE | SW0 to SW7 | SW8 to SW15 |
|------|------|----|---------------------|-------------|
| L | L | L | OFF | OFF |
| L | H | L | ON | OFF |
| H | L | L | OFF | ON |
| H | H | L | ON | ON |
| X | X | H | Hold Previous State | |

Test Circuits

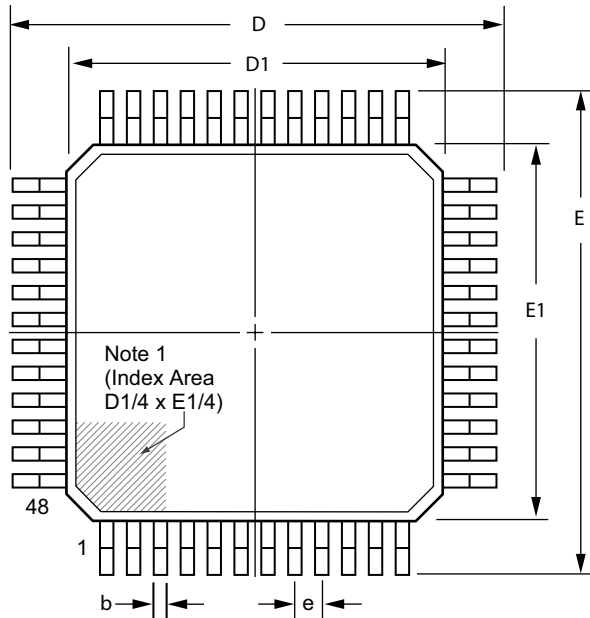


Pin Configuration

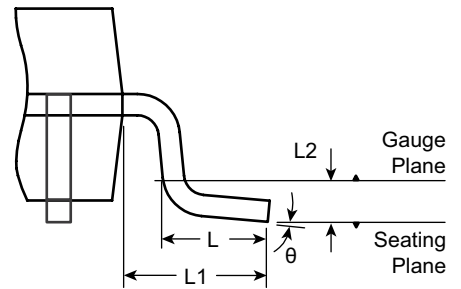
| Pin | Function | Pin | Function |
|-----|------------------------|-----|----------|
| 1 | VNN | 25 | SW10 |
| 2 | N/C | 26 | SW10 |
| 3 | VPP | 27 | SW9 |
| 4 | N/C | 28 | SW9 |
| 5 | D _{IN} 1 | 29 | SW8 |
| 6 | $\overline{\text{LE}}$ | 30 | SW8 |
| 7 | D _{IN} 2 | 31 | SW7 |
| 8 | N/C | 32 | SW7 |
| 9 | N/C | 33 | SW6 |
| 10 | VDD | 34 | SW6 |
| 11 | GND | 35 | SW5 |
| 12 | N/C | 36 | SW5 |
| 13 | RGND | 37 | SW4 |
| 14 | SW15 | 38 | N/C |
| 15 | SW15 | 39 | SW4 |
| 16 | SW14 | 40 | N/C |
| 17 | SW14 | 41 | SW3 |
| 18 | SW13 | 42 | SW3 |
| 19 | SW13 | 43 | SW2 |
| 20 | SW12 | 44 | SW2 |
| 21 | SW12 | 45 | SW1 |
| 22 | SW11 | 46 | SW1 |
| 23 | SW11 | 47 | SW0 |
| 24 | N/C | 48 | SW0 |

48-Lead LQFP Package Outline (FG)

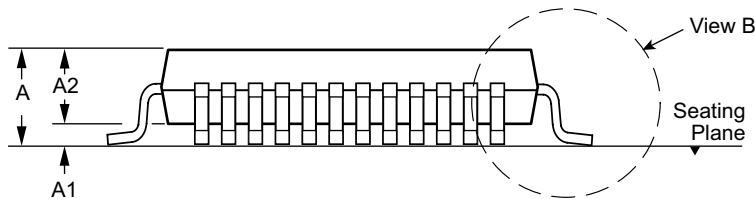
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



View B



Side View

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | |
|----------------|-----|-------|------|------|------|-------|-------|-------|-------|----------|------|----------|----------|----|
| Dimension (mm) | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | 0.50 BSC | 0.45 | 1.00 REF | 0.25 BSC | 0° |
| | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 | | 0.60 | | 3.5° | |
| | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* | | 0.75 | | 7° | |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
 * This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.
 Supertex Doc. #: DSPD-48LQFPFG Version, D041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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