

General Description

The MAX5661 single 16-bit DAC with precision highvoltage amplifiers provides a complete solution for programmable current and voltage-output applications. The output amplifiers swing to industry-standard levels of ±10V (voltage output) or source from 0mA (or from 4mA) to 20mA (current output). The voltage output (OUTV) drives resistive loads greater than $2k\Omega$ and capacitive loads of up to 1.2µF. Voltage-output forcesense connections compensate for series protection resistors and field-wiring resistance. Short-circuit protection on the voltage output limits output current to 10mA (typ) sourcing or -11.5mA (typ) sinking. The current output (OUTI) drives resistive loads up to 37.5V (max) and inductive loads up to 1H.

The MAX5661 provides either a current output or a voltage output. Only one output is active at any given time, regardless of the configuration. The MAX5661 voltage output operates with $\pm 13.48V$ to $\pm 15.75V$ supplies (VDDV, VSSV) and the current output operates with a single +13.48V to +40V supply (V_{DDI}) . A +4.75V to +5.25V digital supply (VCC) powers the rest of the internal circuitry. A buffered reference input accepts an external +4.096V reference voltage.

Update the DAC outputs using software commands or the asynchronous LDAC input. An asynchronous CLR input sets the DAC outputs to the value stored in the clear register or to zero. The FAULT output asserts when the DAC's current output is an open circuit, the DAC's voltage output is a short circuit, or when the CLR

The MAX5661 communicates through a 4-wire 10MHz SPITM-/QSPITM-/MICROWIRETM-compatible serial interface. The DOUT output allows daisy chaining of multiple devices. The MAX5661 is available in a 10mm x 10mm, 64-pin, LQFP package and operates over the -40°C to +105°C temperature range.

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Applications

Industrial Analog Output Modules Industrial Instrumentation Programmable Logic Controls/Distributed Control Systems Process Control

Features

- **♦ 10-Bit Programmable Full-Scale Output** Adjustment for Up to ±25% Over Range
- **♦ Programmable Voltage Output** Unipolar Range: 0 to +10.24V ±25% Bipolar Range: ±10.24V ±25%
- **♦ Programmable Current Output** Unipolar Low Range: 0 to 20.45mA Unipolar High Range: 3.97mA to 20.45mA
- ♦ Flexible Analog Supplies (See Table 16) ±13.48V to ±15.75V for Voltage Output +13.48V to +40V for Current Output
- **♦** Force-Sense Connections (Voltage Output) for Differential Voltage-Output Remote Sensing
- **♦ Voltage-Output Current Limit**
- ♦ Dropout Detector Senses Out-of-Regulation **Current Output**
- ♦ CLR and LDAC Inputs for Asynchronous DAC **Updates**
- ♦ CLR Input Resets Output to Programmed Value or
- **♦ FAULT Output Indicates Open-Circuited Current Output, Short-Circuited Voltage Output, or Clear**
- **♦** Temperature Drift

Voltage Output: ±0.4ppm FSR/°C Current Output: ±7.9ppm FSR/°C

♦ Small 64-Pin LQFP Package (10mm x 10mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5661GCB+	-40°C to +105°C	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

MIXIM

ABSOLUTE MAXIMUM RATINGS

VDDCORE to VSSV		OUTV, SVP,
V _{DDI} to AGND	0.3V to +42V	OUTI, COMP
V _{DDV} to AGND	0.3V to +17V	Maximum Cu
V _{SSV} to AGND	17V to +0.3V	Continuous F
V _{DDI} to V _{SSV}	0.3V to +59V	64-Pin, 10
VCC to DGND	0.3V to +6V	above +70
DGND, DUTGND, DUTGNDS, DACGI	ND,	Junction-to-A
DACGNDS to AGND	0.3V to +6V	in Still Air (
Digital Inputs (CS, DIN, SCLK, CLR, L		Junction-to-0
CNF_) to DGND	0.3V to (V _{CC} + 0.3V)	Operating Te
Digital Outputs (DOUT, FAULT) to DO	3ND	Junction Ten
0.3V to the less	ser of (V _{CC} + 0.3V) or +6V	Storage Tem
REF to AGND	0.3V to +6V	Lead Tempe

OUTV, SVP, SVN, COMPV to VSSV0.3V to (VDDV + 0.3V) OUTI, COMPI, OUTI4/ $\overline{0}$ to AGND0.3V to (VDDI + 0.3V) Maximum Current into Any Pin±100mA Continuous Power Dissipation (TA = +70°C)
64-Pin, 10mm x 10mm TQFP (derate 25mW/°C above +70°C)
Junction-to-Ambient Thermal Resistance
in Still Air (θJA)
Operating Temperature Range40°C to +105°C
Junction Temperature+150°C Storage Temperature Range65°C to +150°C
Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONI	MIN	TYP	MAX	UNITS		
STATIC PERFORMANCE	•	•		•			•	
Resolution				16			Bits	
		Vout		±0.2	±4			
		I_{OUT} , $V_{DDI} = 40V$,	4–20mA		±6			
Integral Nonlinearity	INL	Vssv = V _{DDV} = 0 (Note 2)	0 to 20mA			±10	LSB	
		IOUT, VDDI = VDDV	4–20mA		±2			
		$= +15V, V_{SSV} = -15V$ (Note 2)	0 to 20mA		±6			
Differential Nonlinearity	DNL	Guaranteed monotor	-1.0		+1.0	LSB		
Zero-Scale Voltage Error	V/705	OUTV	Unipolar		±0.01	±3	mV	
Zero-Scale Voltage Error	V _{ZSE}	0017	Bipolar		±2.0	±10		
		0 to 20mA mode	$T_A = +25^{\circ}C$	-45	-30	-15	μΑ	
Zero-Scale Current		0 to zoma mode	$T_A = T_{MIN}$ to T_{MAX}	-60	-30	0		
ero-Scale Voltage Error		4–20mA mode	T _A = +25°C	3.955	3.97	3.985		
		4–20MA Mode	TA = TMIN to TMAX	3.94	3.97	4.00	mA	
		0.4 00 4	T _A = +25°C	-15	±2.0	+15		
Zero-Scale Current Error		0 to 20mA mode	TA = TMIN to TMAX	-30	±2.0	+30	1	
(Note 4)	IZSE	4.00 4	$T_A = +25^{\circ}C$	-15	±3.0	+15	μΑ	
	Ì	4–20mA mode	$T_A = T_{MIN}$ to T_{MAX}	-30	±7.0	+30	j	
V.II. O" LE D'"	TO) (OLITY /	Unipolar		±0.5		ppm of	
Voltage-Offset Error Drift	TCV _{OS}	OUTV	Bipolar		±0.2		FSR/°C	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DACGND} = 0V, R_{SERIES} = 47\Omega, OUTV loaded with <math>2k\Omega$ || 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_{A} = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $T_{A} = +25^{\circ}C$. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	COI	NDITIONS	MIN	TYP	MAX	UNITS				
Coursest Offeet Farer Drift	TOLER	OLITI	0 to 20mA		±4		ppm of				
Current-Offset Error Drift	TCIOS	0011	4–20mA		±4		FSR/°C				
		OUTV	Unipolar		±2.5	±10	ma\/				
Caia France	0.5	OUTV	Bipolar		±4.5	±20	- mV				
Gain Error	GE	OUT	$T_A = +25^{\circ}C$		±8.0	±70					
	rent-Offset Error Drift TCIOS OUTV OUTV OUTI OUTV OUTI OUTV OUTI OUTV, unipolar or VDDV from +13.4 OUTV, bipolar or VSSV from -13.48 OUTI, full-scale or +40V, VSSV = -15 OUTI, full-scale or +40V, VDDV = VS ERENCE INPUT Brence Input Current IREF Brence Input Voltage Range VREF NAMIC PERFORMANCE Out-Voltage Noise at 10kHz Out-Current Noise at 10kHz Dut-Current Noise at 10kHz	0011	$T_A = T_{MIN}$ to T_{MAX}		±40	±130	μΑ				
	OUTV OUTI OUTV OUTI OUTV OUTI OUTV OUTI OUTV, unipolar or VDDV from +13.4 OUTV, bipolar or VSSV from -13.48 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VSSV = -1 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or +40V, VDDV = VSSV from +13.4 OUTI, full-scale or	OUTV	Unipolar	Unipolar ±0.4							
Cain From Drift	TOOF	0017	Bipolar		±0.4		ppm of				
Gain-Error Dilit	ICGE	OUT	0 to 20mA		-7.9		FSR/°C				
		0011	4–20mA		-8.6						
		OUTV, unipolar out V _{DDV} from +13.48V	put, full-scale code, / to +15.75V		20	200	- μV/V				
Dawer Cumply Dejection Datio	DCDD	OUTV, bipolar outp VSSV from -13.48V		20	200	μν/ν					
Power-supply Rejection Ratio	PORR		de, V _{DDI} from +13.48V to '5V, V _{DDV} = +15.75V		0.013	5					
		OUTI, full-scale coo +40V, VDDV = VSSV	0.017		5	μA/V					
REFERENCE INPUT											
Reference Input Current	I _{REF}				0.050	1	μΑ				
Reference Input Voltage Range	V _{REF}			4.0	4.096	4.2	V				
DYNAMIC PERFORMANCE											
Output Voltage Noise at 10kHz		Unipolar output, Vo	OUTV = +10.48V		230		nV/√Hz				
Output-voitage Noise at Toki iz	₽N	Bipolar output, Vol	$JTV = \pm 10.48V$	300			110/1112				
Output Current Noise at 10kHz	į.	0 to 20mA range		132			pA/√Hz				
Output-Current Noise at Tokinz	ın	4-20mA range		120		pA/ VHZ					
Voltage-Output Slew Rate		C _{OUTV} = 100pF, R ₀ step = 20V, C _{EXT} =			0.1		V/µs				
Current-Output Slew Rate		Louti = 0, Routi =	500Ω, step = 20mA		0.15		mA/µs				
		_	OUTV		1		μV∙s				
Major Code Transition Glitch			0 to 20mA		2.0						
		to code 8000n	OUTI 4–20mA		2.0		nA∙s				
Digital Feedthrough			OUTV		0.1		nV∙s				
Digital Feeduli ough		0V to V _{CC} and back to 0V	OUTI, $R_L = 500\Omega$		0.2		pA∙s				

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DACGND} = 0$ $V_{DACGND} = 0V, R_{SERIES} = 47\Omega, OUTV$ loaded with $2k\Omega$ || 100pF to AGND, OUTI loaded with 500 Ω to AGND, $T_{A} = -40^{\circ}C$ to +105°C, unless otherwise noted. Typical values are at $T_{A} = +25^{\circ}C$. See the *Typical Operating Circuit.*) (Note 1)

PARAMETER	SYMBOL	СО	NDITIONS	MIN	TYP	MAX	UNITS	
SETTLING TIME		1						
		Bipolar output,	Couty = 1nF, Routy = $2k\Omega$		3		ma	
		CCOMPV = 3.3nF, to 0.1%	Couty = 1.2 μ F, Routy = 2 $k\Omega$		5.44		ms	
		Bipolar output, CCOMPV = 0nF, to 0.1%	$C_{OUTV} = 100pF,$ $R_{OUTV} = 2k\Omega$		244		μs	
		Unipolar output, CCOMPV = 3.3nF,	$C_{OUTV} = 1nF,$ $R_{OUTV} = 2k\Omega$		1.8	ms		
		to 0.1%	$C_{OUTV} = 1.2\mu F,$ $R_{OUTV} = 2k\Omega$		3 5.44 244	IIIS		
		Unipolar output, CCOMPV = 0nF, to 0.1%	$C_{OUTV} = 100pF,$ $R_{OUTV} = 2k\Omega$		130		μs	
			$R_{OUTI} = 500\Omega$		1.5			
		0 to 20.45mA	L _{OUTI} = 1mH		1.66]	
		range to 0.1%	L _{OUTI} = 10mH		1.66		ms	
surrent-Output Settling Time			L _{OUTI} = 1H		1.97			
			$R_{OUTI} = 500\Omega$		1.43			
		3.97mA to 20.45mA range	L _{OUTI} = 1mH		1.58			
		to 0.1%	L _{OUTI} = 10mH		1.58		[
			L _{OUTI} = 1H		1.73			

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DACGND} = 0V, R_{SERIES} = 47\Omega, OUTV loaded with <math>2k\Omega$ || 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_{A} = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $T_{A} = +25^{\circ}C$. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ОИТУ ОИТРИТ			·				
OUTV Linear Output Voltage Range				V _{SSV} + 3.0		V _{DDV} - 3.0	V
Default OUTV Output Voltage	\/ - -	Unipolar, V _{DDV} = +13.48V, V _{SSV}	v = -13.48V	0		+10.48	V
Ranges (0V to Full Scale)	Vout	Bipolar, $V_{DDV} = +13.48V$, V_{SSV}	= -13.48V	-10.48		+10.48	V
Minimum OUTV Output Voltage	V	Unipolar			+7.68		V
Range (FS to ADJ)	V _{OUT}	Bipolar			±7.68		V
Maximum OUTV Output Voltage	Vout	Unipolar			+12.8		V
Range (FS to ADJ)	VOU1	Bipolar			±12.8		V
DC Output Impedance					0.1		Ω
OUTV Off-State Leakage Current		OUTV off or disabled, output leakage current from OU	ITV to AGND		2.5	10	μΑ
OUTV Short-Circuit Output	1	Sourcing		7	10	13	Λ
Current	Isc	Sinking		-18.0	-11.5	-9.0	mA
Minimum OUTV Resistive Load	Routv	Full-scale code			2		kΩ
Maximum OLITY Canaditive Load	Court	C _{COMPV} = 3.3nF			1.2		μF
Maximum OUTV Capacitive Load	Coutv	CCOMPV = 0nF			1		nF
ОИТІ ОИТРИТ							
OUTI Voltage Compliance		Full-scale output, R _{OUTI} = 1500	Ω (Note 5)		V	_{DDI} - 2.5	V
OUTI Output Current Range		0 to 20mA mode includes FS ca (Note 4)	alibration	0		20.45	mA
		4-20mA mode includes FS calib	oration	3.97		20.45	
DC Output Impedance		OUTI = full scale			45		MΩ
OUTI Off-State Leakage Current		OUTI off or disabled, 0V < V _{OUTI} < V _{DDI}			0.1	10	μΑ
Current-Mode Dropout Detection		V _{DDI} - V _{OUTI} , FAULT does not a	ssert		1.3		V
FEEDBACK SENSE BUFFER INP	UTS						
Input Current		V _{SSV} + 1.7V < SVP, SVN < V _{DD}	v - 1.7V		0.05	1	μA
Input Voltage Range		SVP, SVN		V _{SSV} + 1.7		V _{DDV} - 1.7	V
DIGITAL INPUTS	•	•	•				
Input High Voltage	VIH	V _{CC} = 4.75V to 5.25V		2.4			V
Input Low Voltage	VIL	V _{CC} = 4.75V to 5.25V				0.8	V
Input Capacitance	CIN				10		рF
Input Leakage Current	I _{IN}	V _{IN} = 0V or V _{CC}		-1		+1	μΑ
DIGITAL OUTPUTS							
Output High Voltage	V _{OH}	I _{SOURCE} = 400µA, except FAUL	_T	V _{CC} - 0.5			V
Output Low Voltage	\/a:	V _{CC} = 4.75V	mA			0.4	V
Culput Low Voltage	V _{OL}	$V_{CC} = 4.75V$ $I_{SINK} = 10r$	mA			1	V

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DACGND} = 0$ $V_{DACGND} = 0V, R_{SERIES} = 47\Omega, OUTV$ loaded with $2k\Omega$ || 100pF to AGND, OUTI loaded with 500 Ω to AGND, $T_{A} = -40^{\circ}C$ to +105°C, unless otherwise noted. Typical values are at $T_{A} = +25^{\circ}C$. See the *Typical Operating Circuit.*) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Output High Leakage Current		FAULT only		0.1	2	μΑ	
Three-State Output Leakage Current		DOUT only		±0.1	±2	μΑ	
POWER SUPPLIES (see Table 16)					•	
V _{CC} Supply Range	Vcc		+4.75		+5.25	V	
		Only OUTV powered	+13.48		+15.75		
V _{DDV} Supply Range	V_{DDV}	Only OUTI powered		AGND		V	
		Both OUTV and OUTI powered	+13.48		+15.75		
		Only OUTV powered	-15.75		-13.48		
V _{SSV} Supply Range	V _{SSV}	Only OUTI powered		AGND		V	
		Both OUTV and OUTI powered	-15.75		-13.48		
		Only OUTV powered		V_{DDV}			
V _{DDI} Supply Range	V _{DDI}	Only OUTI powered	+13.48		+40.00	V	
		Both OUTV and OUTI powered	V_{DDV}		+40		
		Only OUTV powered		V_{DDV}			
V _{DDCORE} Supply Range	VDDCORE	Only OUTI powered		V			
		Both OUTV and OUTI powered		V_{DDV}			
Analog and Digital Supply	VDDV + VDDI + OUTV powered, VDDV = VDDI = VDDCORE +15.75V, VSSV = -15.75V, VCC = +5.25V, VDDI = VDDCORE +5.25V, +5.25V,			4.5	6.5		
Currents (OUTV Active)	lyssy	OUTV unloaded, all ditgital inputs at V _{CC} or	-5	-2.5		mA	
,	IAGND	DGND	-3.0	-1.6			
	lvcc			0.03	0.2		
Analog and Digital Supply	I _{VDDV} + I _{VDDI} + I _{VDDCORE}	OUTI powered, V _{DDV} = V _{SSV} = AGND,		2.8	5.5		
Currents (OUTI Active), 0 to	lyssy	$V_{DDI} = V_{DDCORE} = +12V \text{ to } +40V, V_{CC} =$	-1.0	-0.03		mA	
20mA Mode	IAGND	+5.25V, zero code	-4.0	-2.1			
nalog and Digital Supply urrents (OUTV Active) nalog and Digital Supply urrents (OUTI Active), 0 to 0mA Mode	lvcc			0.03	0.2		
Analog and Digital Supply	IVDDV + IVDDI + IVDDCORE	OUTI powered, V _{DDV} = V _{SSV} = AGND,		6.8	9.5		
,	lyssy	V _{DDI} = V _{DDCORE} = +12V to +40V, V _{CC} =	-1.0	-0.03		mA	
Mode	IAGND	+5.25V, zero code	-4.0	-2.1			
	lvcc			0.03	0.2		
	IVDDV + IVDDCORE	Both OUTV and OUTI powered, V _{DDV} =		4.2	6		
Analog and Digital Supply	lyssy	V _{DDCORE} = +15.75V, V _{SSV} = -15.75V, V _{DDI} = +40V, V _{CC} = +5.25V, OUTV unloaded at zero	-4.0	2.6			
Currents (Either OUTV or OUTI	IAGND	code, all ditgital inputs at VCC or DGND	-4.0	-2.0		mA	
Active)	lvcc			0.03	0.2		
	Ivddi	0 to 20mA at zero code		1.3	2		
	Ivddi	4-20mA at zero code		5.3	6.5		

TIMING CHARACTERISTICS

 $(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, AGND = DGND = DUTGND = DACGND = 0V, R_{SERIES} = 47\Omega, OUTV loaded with <math>2k\Omega$ || 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$. See Figure 1.) (Notes 1, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise or Fall to $\overline{\text{CS}}$ Fall Setup Time	tcso		45			ns
CS Fall to SCLK Rise or Fall Setup Time	tcss		40			ns
SCLK Pulse-Width High	tсн		45			ns
SCLK Pulse-Width Low	tCL		45			ns
DIN to SCLK High Setup Time	t _{DS}		40			ns
DIN to SCLK High Hold Time	tDH		0			ns
SCLK Period	tcp		100			ns
CS Pulse-Width High	tcsw		100			ns
CS High to SCLK High or Low Setup Time	tCS1		45			ns
SCLK High to $\overline{\text{CS}}$ Hold Time	tcsh		45			ns
SCLK Fall to DOUT Valid Propagation Delay	tDO	C _{DOUT} = 100pF			100	ns
CS Transitions to DOUT Enable/Disable Delay	t _{DV}	C _{DOUT} = 100pF			100	ns
SCLK Fall or Rise to $\overline{\text{CS}}$ Rise Time	tscs		15	_	_	ns
LDAC Pulse-Width Low	t _{LDL}		40			ns
CS Rise to LDAC Rise Time	tcsld		80			ns

Note 1: Devices are 100% production tested at $T_A = +25^{\circ}C$ and $+105^{\circ}C$. Operation to $-40^{\circ}C$ is guaranteed by design.

Note 2: IOUT INL 100% production tested from 0 to 20mA only.

Note 3: IOUT DNL guaranteed by VOUT DNL.

Note 4: 0 to 20mA zero-scale current extrapolated by interpolation from full scale and code 192. See the *Measuring Zero-Code Current (0 to 20mA Mode)* section.

Note 5: OUTI voltage compliance measured at $V_{DDI} = +33.22V$.

Note 6: When updating the DAC registers, allow 5µs before sending the next command.

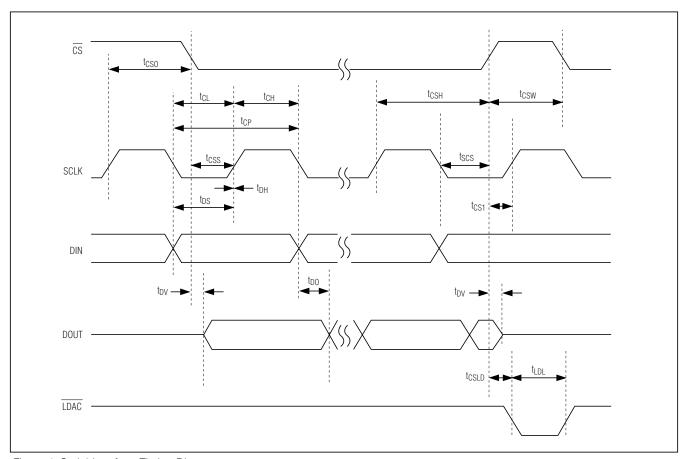
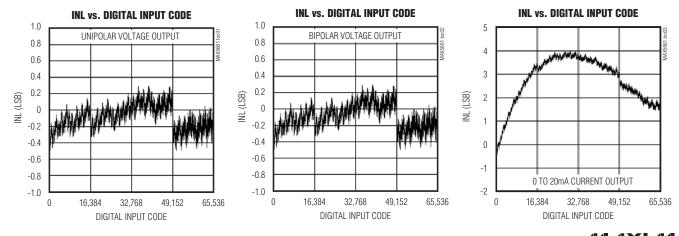


Figure 1. Serial-Interface Timing Diagram

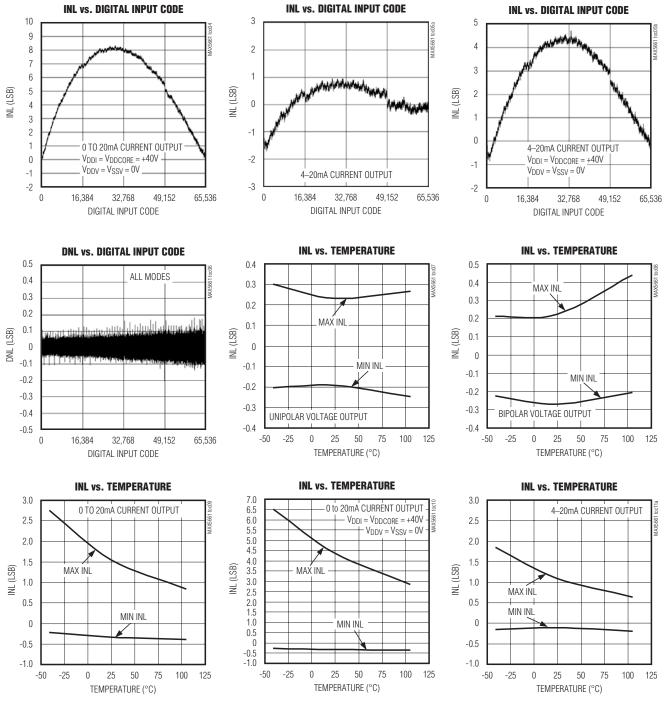
Typical Operating Characteristics

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{AGND} =$



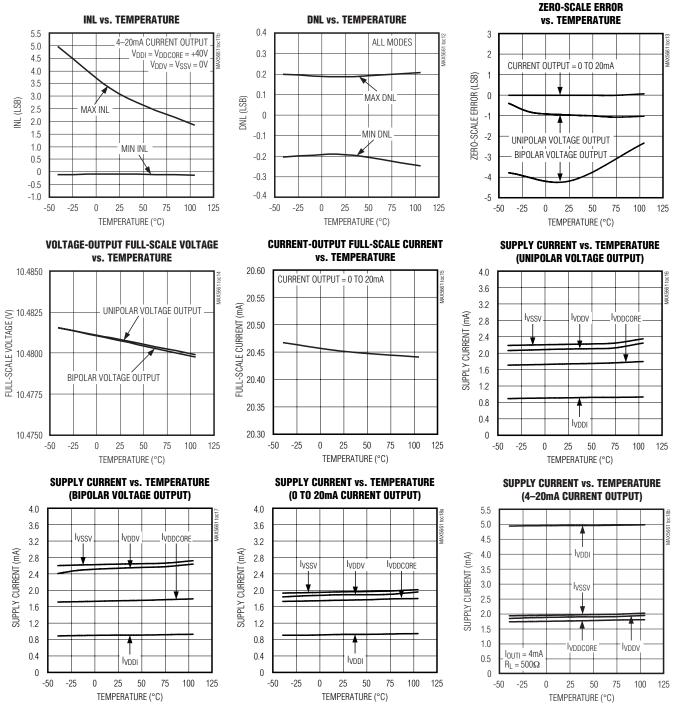
Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RSERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_A = +25^{\circ}C$.)



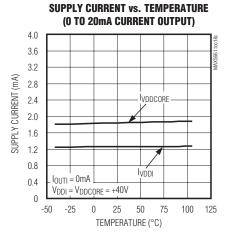
Typical Operating Characteristics (continued)

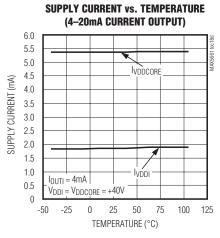
(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RSERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $V_{AGND} = V_{AGND} = 0V$, $V_{AGND} = 0V$, V_{AGND}

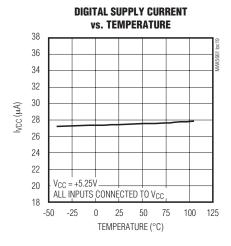


Typical Operating Characteristics (continued)

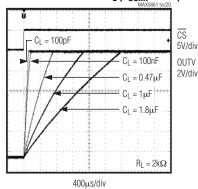
(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RSERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_A = +25^{\circ}C$.)

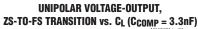


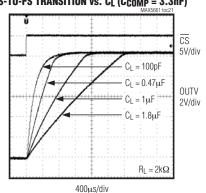




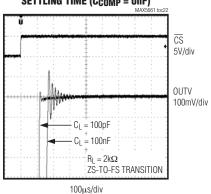




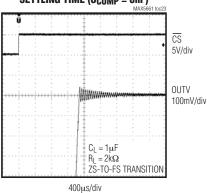


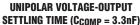


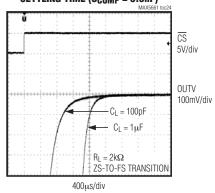
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (CCOMP = OnF)



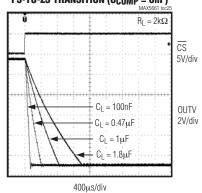
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (CCOMP = Onf)





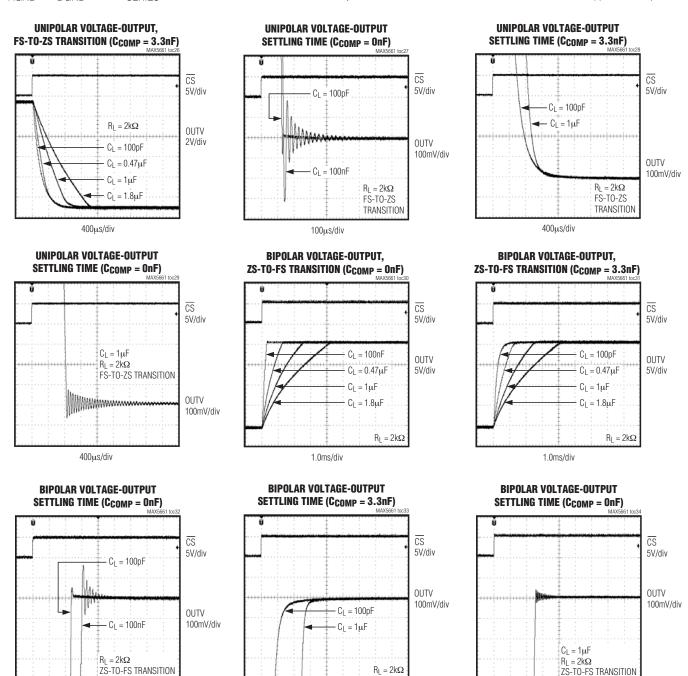


UNIPOLAR VOLTAGE-OUTPUT, FS-TO-ZS TRANSITION (CCOMP = OnF)



Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $V_{AGND} = V_{AGND} = 0V$, $V_{AGND} = 0V$,



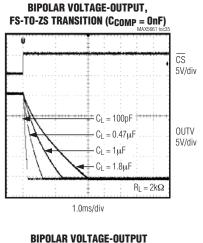
1.0ms/div

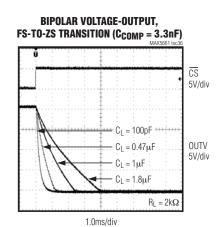
1.0ms/div

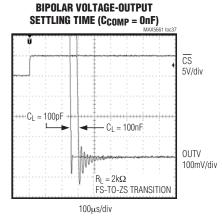
100µs/div

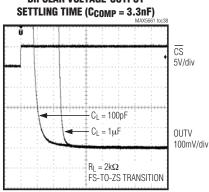
Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RSERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_{A} = +25^{\circ}C$.)

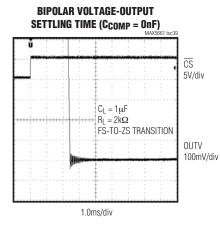


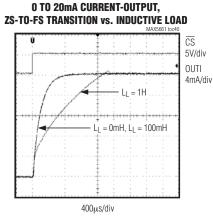


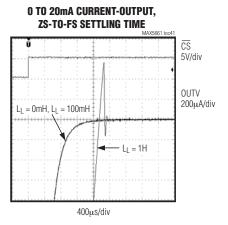


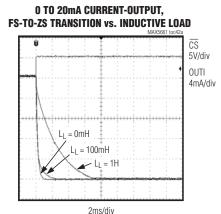


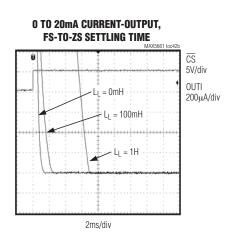
1.0ms/div







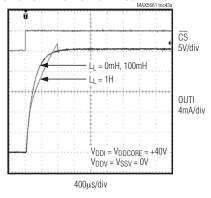




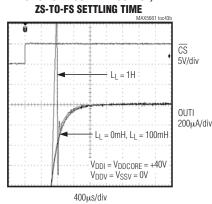
Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RSERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $V_{AGND} = V_{AGND} = 0V$, $V_{AGND} = 0V$, V_{AGND}

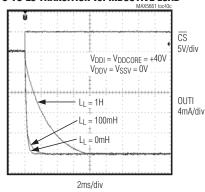
O TO 20mA CURRENT-OUTPUT, ZS-TO-FS TRANSITION vs. INDUCTIVE LOAD



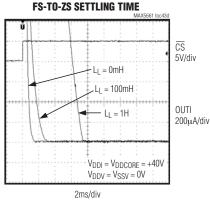
O TO 20mA CURRENT-OUTPUT,



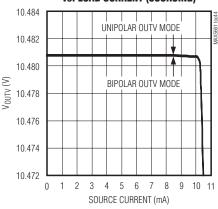
O TO 20MA CURRENT-OUTPUT, FS-TO-ZS TRANSITION VS. INDUCTIVE LOAD



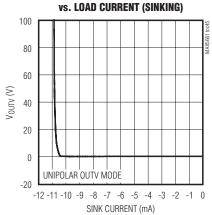
O TO 20mA CURRENT-OUTPUT, FS-TO-7S SETTLING TIME



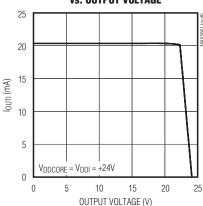
OUTV OUTPUT VOLTAGE vs. LOAD CURRENT (SOURCING)



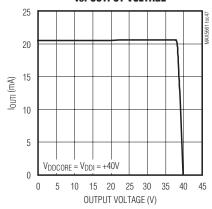
OUTV OUTPUT VOLTAGE



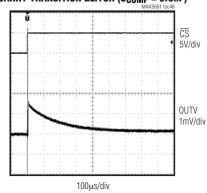
OUTI OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTI OUTPUT CURRENT vs. OUTPUT VOLTAGE



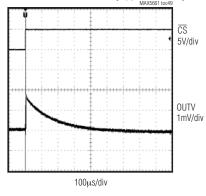
UNIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (CCOMP = 3.3nF)



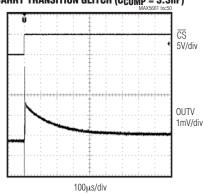
Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RSERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $T_A = +25^{\circ}C$.)

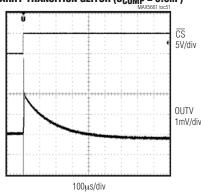
UNIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH ($C_{COMP} = 3.3nF$)



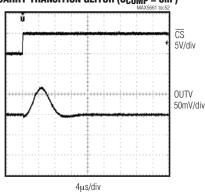
BIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH ($C_{COMP} = 3.3nF$)



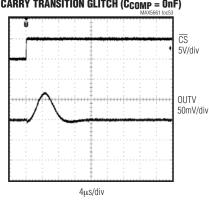
BIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH ($C_{COMP} = 3.3nF$)



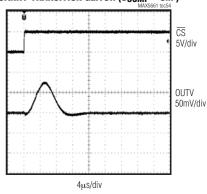
UNIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 0nf)



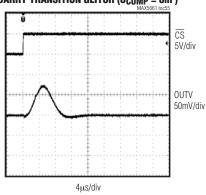
UNIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = Onf)



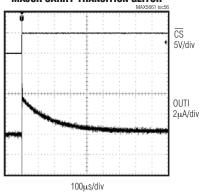
BIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (CCOMP = OnF)



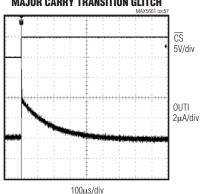
BIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH (CCOMP = OnF)



O TO 20mA CURRENT-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH

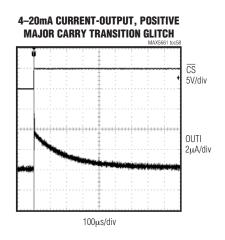


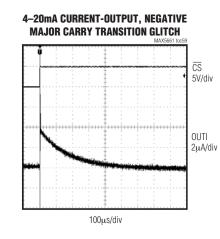
O TO 20MA CURRENT-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH

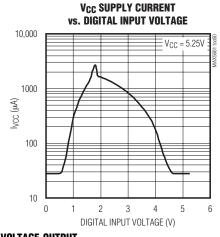


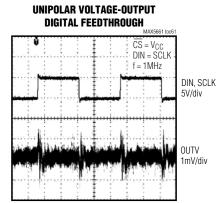
Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $V_{AGND} = V_{AGND} = 0V$, $V_{AGND} = 0V$,

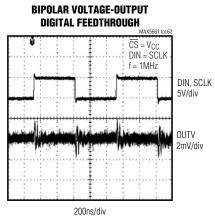


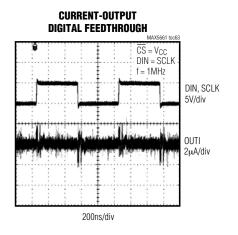


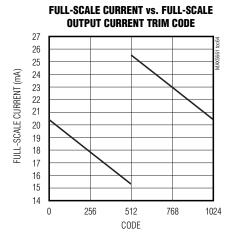




200ns/div

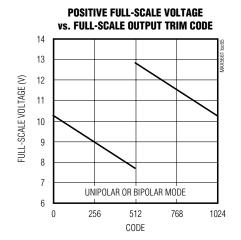


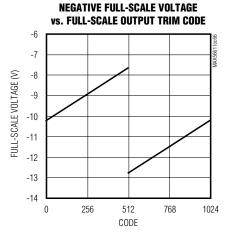




Typical Operating Characteristics (continued)

(Typical Operating Circuit, $V_{CC} = +5V$, $C_{COMPI} = 22nF$, $V_{DDV} = V_{DDCORE} = +15V$, $V_{SSV} = -15V$, $V_{DDI} = +24V$, $V_{REF} = +4.096V$, $V_{AGND} = V_{DGND} = 0V$, $V_{RERIES} = 47\Omega$, OUTV loaded with $2k\Omega$ II 100pF to AGND, OUTI loaded with 500Ω to AGND, $V_{AGND} = V_{AGND} = 0V$, $V_{AGND} = 0V$,





Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 8, 10, 15–20, 29–34, 36, 38, 42, 44, 46–52, 58, 61–64	N.C.	No Connection. Not internally connected.
2	OUTI	DAC Current-Source Output. OUTI sources either from 0 to 20mA or from 4–20mA.
4	V _{DDI}	DAC Current-Output Positive Supply. Connect V _{DDI} to a power supply between +13.48V and +40V to power the DAC current-output (OUTI) buffer. Bypass V _{DDI} with a 0.1µF capacitor to AGND, as close as possible to the device.
6	СОМРІ	OUTI Noise-Limiting Capacitor Connection. Connect a 22nF capacitor from COMPI to V _{DDI} to reduce transient noise at OUTI.
9	OUTI4/0	Current-Output Range Selection Input. Connect OUTI4/0 to AGND to select the 0 to 20mA OUTI current-output range. Connect OUTI4/0 to VDDI to select the 4–20mA OUTI current-output range. The OUTI current range can also be set by software. When using software to set the OUTI current range, connect OUTI4/0 to AGND.
11	REF	Buffered Voltage Reference Input. Connect an external +4.096V voltage reference to REF. Bypass REF with a $0.1\mu F$ capacitor to DACGND, as close as possible to the device. Use a $1k\Omega$ resistor in series to the reference input for optimum performance.
12	DACGND	DAC Analog Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
13	DACGNDS	DAC Analog Sense Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
14	CNF1	Voltage/Current Configuration Input. CNF1 and CNF0 control the OUTV and OUTI outputs. See Tables 13 and 14.
21	CNF0	Voltage/Current Configuration Input. CNF0 and CNF1 control the OUTV and OUTI outputs. See Tables 13 and 14.

____Pin Description (continued)

PIN	NAME	FUNCTION
22	DIN	Serial-Data Input. Data is clocked into the serial interface on the rising edge of SCLK.
23	SCLK	Serial-Clock Input
24	CS	Active-Low Chip-Select Input. Drive $\overline{\text{CS}}$ low to enable the serial interface. Drive $\overline{\text{CS}}$ high to disable the serial interface. DOUT is high impedance when $\overline{\text{CS}}$ is high.
25	DGND	Digital Ground
26	VCC	Digital Power Supply. Connect V_{CC} to a power supply between +4.75V and +5.25V. Bypass V_{CC} with a 0.1 μ F capacitor to DGND, as close as possible to the device.
27	LDAC	Active-Low Asynchronous Load DAC Input. Drive LDAC low to transfer the contents of the input register to the DAC register to immediately update the output. Connect LDAC to V _{CC} if unused.
28	FAULT	Active-Low Open-Drain Fault Output. FAULT asserts low for an OUTI open-circuit condition, an OUTV short-circuit condition, or when the CLR input is low (see Table 12 and Figure 9). Ignore the FAULT pin function in single supply mode.
35	DOUT	Serial Data Output. Data transitions at DOUT on SCLK's falling edge. DOUT is high impedance when \overline{CS} is high. Use DOUT to read the shift register contents or for daisy chaining multiple MAX5661 devices.
37	CLR	Active-Low Clear Input. Drive $\overline{\text{CLR}}$ low to set the DAC code to the value stored in the clear register, to 0V in voltage mode, or 0mA/4mA depending on the output current mode. Program the contents of the clear register through the serial interface. Enable and disable the $\overline{\text{CLR}}$ input through the control register's $\overline{\text{CLREN}}$ bit (see Table 4).
39	VDDCORE	DAC Core Positive Supply. Connect V _{DDCORE} to V _{DDI} or V _{DDV} (see Table 16). Bypass V _{DDCORE} with a 0.1µF capacitor to AGND, as close as possible to the device.
40	DUTGNDS	DUT Analog Sense Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
41	DUTGND	DUT Analog Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
43	COMPV	OUTV Amplifier Compensation Feedback Node. Connect a 3.3nF capacitor from OUTV to COMPV when OUTV drives capacitive loads of up to 1.2µF. Leave COMPV open for faster response time.
45	AGND	Analog Ground
53	SVP	Remote Ground Sense Input. Connect SVP to the bottom terminal of R _{OUTV} . See the <i>Typical Operating Circuit</i> .
54, 59	I.C.	Internal Connection. Leave unconnected.
55	VSSV	DAC Voltage-Output Negative Power Supply. Always connect V _{SSV} to a power supply between -13.48V and -15.75V. Bypass V _{SSV} with a 0.1µF capacitor to AGND, as close as possible to the device.
56	OUTV	DAC Unipolar/Bipolar Voltage Output. OUTV provides 0 to +10.48V in unipolar mode and -10.48V to +10.48V in bipolar mode.
57	VDDV	DAC Voltage-Output Positive Power Supply. Connect V _{DDV} to a power supply between +13.48V and +15.75V. Bypass V _{DDV} with a 0.1µF capacitor to AGND, as close as possible to the device.
60	SVN	Remote Voltage Sense Input. Connect to the top terminal of R _{OUTV} . See the <i>Typical Operating Circuit</i> .

Detailed Description

The MAX5661 single 16-bit DAC with precision high-voltage amplifiers provides a complete solution for programmable current and voltage-output applications. The programmable output amplifiers swing to industry-standard voltage levels of $\pm 10 V$ or current levels from 0mA (or from 4mA) to 20mA. The OUTV voltage output drives resistive loads greater than $2k\Omega$ and capacitive loads up to 1.2µF. Force and sense connections on the voltage output compensate for series protection resistors and field wiring resistance. Short-circuit protection on the voltage output limits output current. The OUTI current output drives resistive loads from 0Ω and higher, up to a compliance voltage of (VDDI - 2.5V). The OUTI current output also drives inductive loads up to 1H.

The MAX5661 provides a current output or a voltage output, with only one output active at any given time. The MAX5661 operates with ±13.48V to ±15.75V dual supplies (VDDV, VSSV) for the voltage output and a +13.48V to +40V single supply (VDDI) for the current output (see Table 16). The +4.75V to +5.25V digital supply (VCC) powers the digital circuitry and VDDCORE powers the rest of the internal analog circuitry. A buffered reference input accepts a +4.096V reference voltage.

The \overline{LDAC} and \overline{CLR} inputs asynchronously update the DAC outputs. \overline{CLR} sets the DAC code to the value stored in the clear register (software clear), or to zero scale (hardware clear). The \overline{FAULT} output asserts for an open-circuit current output, a short-circuit voltage output, or a clear state condition when \overline{CLR} is low. The power-on reset circuitry guarantees the outputs remain off at power-up and all register bits are set to zero to ensure a glitchless power-up sequence.

A 10MHz SPI-/QSPI-/MICROWIRE-compatible serial interface programs the DAC outputs and configures the device. The DOUT output allows shift-register reads or daisy chaining of several devices. The double-buffered interface includes an input register and a DAC register. Use software commands or the asynchronous LDAC input to transfer the input register contents to the DAC register and update the DAC outputs.

4-Wire SPI-Compatible Serial Interface

The MAX5661 communicates through a serial interface compatible with SPI, QSPI, and MICROWIRE devices. For SPI, ensure that the SPI bus master (typically a

microcontroller (μ C)) runs in master mode to generate the serial-clock signal. Set the SCLK frequency to 10MHz or less, and set the clock polarity (CPOL) and phase (CPHA) in the μ C control registers to the same value. The MAX5661 operates with SCLK idling high or low, and thus operates with CPOL = CPHA = 0 (see Figure 2) or CPOL = CPHA = 1 (see Figure 3). Force $\overline{\text{CS}}$ low to input data at DIN on the rising edge of SCLK. Output data at DOUT updates on the falling edge of SCLK (see Figure 1).

A high-to-low transition on $\overline{\text{CS}}$ initiates the 24-bit data input cycle. Once $\overline{\text{CS}}$ is low, write an 8-bit command byte (MSB first) at DIN to send data to the appropriate internal register (see Tables 1, 2, and 3). C7 is the MSB of the command byte and C0 is the LSB. Following the command byte, write 2 data bytes containing bits D15–D0. D15 is the MSB of the 2 data bytes and D0 is the LSB (see Figure 4 and the *Register Descriptions* section). Data loads into the shift register 1 bit at a time.

Write the data as one continuous 24-bit stream, always keeping $\overline{\text{CS}}$ low throughout the entire 24-bit word. The MAX5661 stores the 24 most recent bits received, including bits from previous transmission(s). Ensure SCLK has 24 rising and falling edges between $\overline{\text{CS}}$ falling low to $\overline{\text{CS}}$ returning high. Data loads into the shift register on the rising edge of SCLK. Once $\overline{\text{CS}}$ returns high, data transfers from the shift register into the appropriate internal register.

When reading data, write an 8-bit command byte and 16 data bits at DIN. On the following 24-bit sequence, read out the shift register's contents (command byte and the 16 data bits) at DOUT (see Figure 5). Data transitions at DOUT on the falling edge of SCLK. While reading data at DOUT on the second 24-bit sequence, load another command byte and 2 data bytes at DIN or write a no-operation command. DOUT three-states when $\overline{\text{CS}}$ is high. The DAC outputs update on the rising edge of $\overline{\text{CS}}$ after writing to the DAC register or by pulling $\overline{\text{LDAC}}$ low.

Daisy chain multiple devices by connecting the first DOUT to the second DIN, and so forth. Daisy chaining allows communication with multiple MAX5661 devices using single $\overline{\text{CS}}$ and SCLK signals. See the Daisy Chaining Multiple MAX5661 Devices section.

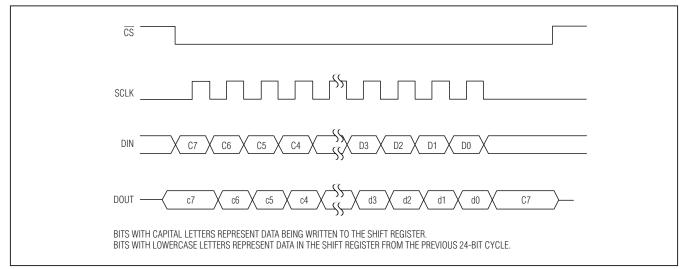


Figure 2. MICROWIRE- or SPI-Interface Timing Diagram (CPOL = CPHA = 0)

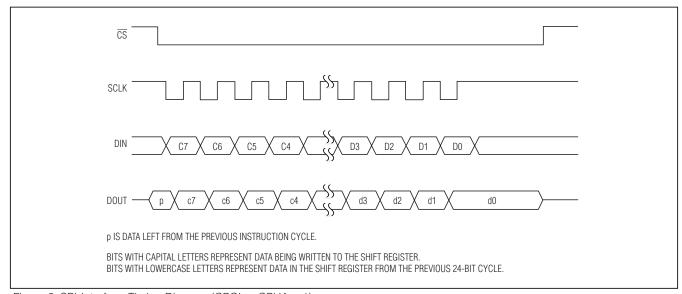


Figure 3. SPI-Interface Timing Diagram (CPOL = CPHA = 1)

Table 1. Input Command Bits

	24-BIT SERIAL INPUT WORD																				
COMMAND BYTE														DA	ТА В	ITS					
MSB													LSB								
C7	C6	C5	C4	СЗ	C2	C1	C0	D15	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2									D1	D0		

Table 2. Register Description

			СОММА	ND BITS	}			OPERATION
C 7	C6	C 5	C4	C3	C2	C1	C0	OPERATION
X	X	X	X	0	0	0	0	No operation. Transfer shift register's data to DOUT.
Х	Χ	Χ	Χ	0	0	0	1	Write control register.
Х	Х	Χ	Х	0	0	1	0	Read control register.
X	Х	Х	Х	0	0	1	1	Load input register. DAC register unchanged.
X	Х	Х	Х	0	1	0	0	Load DAC and input register.
Х	Х	Х	Х	0	1	0	1	Load DAC register. Transfer input register data to DAC register. DAC outputs update on $\overline{\text{CS}}$'s rising edge.
Х	Х	Х	Х	0	1	1	0	Write clear register.
Х	Х	Х	Х	0	1	1	1	Read input register.
X	Х	Х	Х	1	0	0	0	Read DAC register.
Х	Х	Х	Х	1	0	0	1	Read clear register.
Х	Χ	Χ	Χ	1	1	1	1	No operation. Transfer shift register's data to DOUT.

X = Don't care. All other commands are reserved for factory use. Do not use.

Register Descriptions

The MAX5661 communicates between its internal registers and the external bus lines through the 4-wire SPI-/QSPI-/MICROWIRE-compatible serial interface. Table 1 details the command bits (C7–C0) and the data bits (D15–D0) of the serial input word. Tables 2 and 3 detail the command byte and the subsequent register accessed. Tables 4–8 detail the various read/write internal registers and their power-on reset states. When updating the DAC register, allow 5µs before sending the next command.

Control Register (Read/Write)

Write to the control register to enable the current or voltage output, set the voltage output for unipolar or bipolar

mode, and set the current-output range. The control register also initializes the clear and fault modes. Set the command byte to 0x01 to write to the control register. Set the command byte to 0x02 to read from the control register. Write or read data bits D15–D5. D4–D0 are don't-care bits for a write operation. D4, D3, and D2 are read-only bits. D1 and D0 are don't-care bits for a read operation (see Table 4).

Set the OUTVON bit (D15) to 1 to enable the OUTV DAC voltage output. Set the OUTION bit (D14) to 1 to enable the OUTI DAC current output. Always set bit D13 to 0. Set the \overline{B}/U bit (D12) to determine whether the OUTV output operates in bipolar mode ($\overline{B}/U=0$) or unipolar mode ($\overline{B}/U=1$).

Table 3. Register Bit Descriptions

					COMMA	ND BY	TE					1	ST DAT	BYTE						2	ND DAT/	BYTE			
OPERATION	DESCRIPTION	C7	C6	C5	C4	C3	C2	C1	CO	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	DO
No operation.	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	0	0	0	0	Х	Х	Х	Х	х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
Transfer shift- register data to DOUT.	Data in shift register after CS driven high and command executed								Sa	me as lin	ne above.	Shift-re	gister da	ta not ch	anged by	this op	eration.								
No operation. Transfer shift-	Data in shift register before CS driven high and command executed	Х	х	Х	Х	1	1	1	1	Х	Х	Х	Х	х	Х	Х	Х	Х	х	Х	Х	х	Х	Х	х
register data to DOUT.	Data in shift register after CS driven high and command executed		Same as line above. Shift-register data not changed by this operation.																						
Write control	Data in shift register before CS driven high and command executed	Х	х	х	х	0	0	0	1	NOVTUO	OUTION	0	Β/U	OUTI4/Õ EN	14 to 20 BIT	CLREN	CLRMODE	RCLR	FAULTEN	CLRFLAGEN	х	х	Х	Х	х
register	Data in shift register after CS driven high and command executed					•			Sa	me as lin	ne above.	Shift-re	gister da	ta not ch	anged by	this op	eration.								
Read control	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	0	0	1	0	х	Х	Х	Х	х	Х	Х	Х	Х	х	Х	Х	х	Х	Х	Х
register	Data in shift register after CS driven high and command executed			San	ne as line	above.				NOVTUO	NOILION	0	<u>B</u> /U	0UTI4/0 EN	14 to 20 BIT	CLREN	CLRMODE	RCLR	FAULTEN	CLRFLAGEN	FAULTV	FAULTI	CLEARST	х	Х
Load input register from shift	Data in shift register before CS driven high and command executed	х	Х	Х	Х	0	0	1	1					•	MSI	3 < 16-	Bit DAC	Data>	- LSB		•	'		•	
register. DAC register unchanged.	Data in shift register after CS driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Load input register and DAC	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	0	1	0	0						MSI	3< 16-	Bit DAC	Data>	- LSB						
register from shift register.	Data in shift register after CS driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Load DAC register from input	Data in shift register before CS driven high and command executed	х	Х	Х	Х	0	1	0	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
register	Data in shift register after CS driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Write clear register	Data in shift register before CS driven high and command executed	Х	X X X X 0 1 1 0 MSB < 16-Bit Clear-Register Data> LSB																						
iegistei	Data in shift register after CS driven high and command executed								Sa	me as lin	ne above.	Shift-re	gister da	ta not ch	anged by	this op	eration.								
Read input register	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	0	1	1	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
	Data in shift register after CS driven high and command executed			San	ne as line	above.								N	ISB < 1	6-Bit In	out-Regi	ster Data	> LSB						
Read DAC register	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	1	0	0	0	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х
logistor	Data in shift register after CS driven high and command executed			San	ne as line	above.								٨	ISB <	16-Bit D	AC-Regi:	ster Data	> LSB						
Read clear	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	1	0	0	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Χ	Х	Х
register	Data in shift register after CS driven high and command executed		ı	San	ne as line	above.						1	1	MSB	< 16-E	it DAC (Clear Reç	gister Dat	ia> LS	В	ı	I		ı	
Write full-scale	Data in shift register before CS driven high and command executed	Х	Х	Х	Х	1	0	1	0	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	Х	Х	Х
output trim register	Data in shift register after CS driven high and command executed			San	ne as line	e above.				FS_EN	Х	х	х	Х	Х	FS_ BIT 9 (MSB)	FS_BIT 8	FS_ BIT 7	FS_ BIT 6	FS_BIT 5	FS_BIT 4	FS_BIT 3	FS_BIT 2	FS_BIT 1	FS_BIT 0 (LSB)

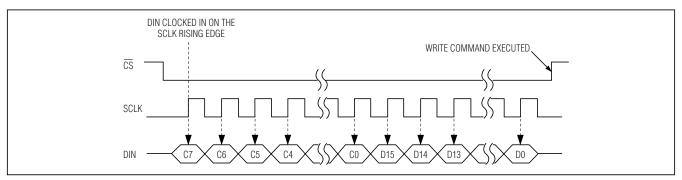


Figure 4. Write Timing

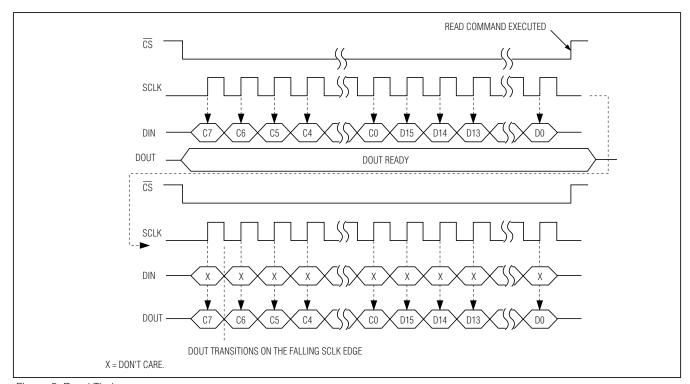


Figure 5. Read Timing

Set the OUTI4/OEN bit (D11) low to enable the OUTI4/O hardware input. Set the I4TO20BIT bit (D10) high to select the current-output range through the software. Set the CLREN bit (D9) low to enable the CLR hardware input. Set the CLRMODE bit (D8) high to force the output to the value in the clear register or the zero state when the CLR hardware input is pulled low. Set the RCLR bit (D7) high to remain in the clear state. Set the FAULTEN bit (D6) high to enable the FAULT output

functionality. Set the CLRFLAGEN bit (D5) high to activate the FAULT output when the MAX5661 is in the clear state.

Bits D4, D3, and D2 are read-only bits. The FAULTV bit (D4) is set to 1 when OUTV is short circuited. The FAULTI bit (D3) is set to 1 when OUTI is open circuited. The CLEARST bit (D2) is set to 1 when the MAX5661 is in the clear state.

Table 4. Control Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
OUTVON	D15	0	DAC OUTV output enable bit. Set to 1 to enable the OUTV output.
OUTION	D14	0	DAC OUTI output enable bit. Set to 1 to enable the OUTI output.
_	D13	0	Reserved. Always set to 0.
B/U	D12	0	Voltage-output unipolar/bipolar mode select bit. Set to 0 (default power-up state) to select the bipolar output range ($\pm 10.48V$). Set to 1 to select the unipolar output range (0 to $\pm 10.48V$).
OUTI4/0EN	D11	0	OUTI4/0 enable bit. Set to 0 (default power-up state) to enable the OUTI4/0 hardware input. Set to 1 to disable the OUTI4/0 hardware input, thereby controlling the current-output range through software commands.
I4TO20BIT	D10	0	OUTI current range bit. Set to 0 to set the OUTI current range from 0 to 20mA. Set to 1 to set the OUTI current range from 4–20mA.
CLREN	D9	0	Clear enable bit. Set to 0 to enable the external $\overline{\text{CLR}}$ input. Set to 1 to disable the external $\overline{\text{CLR}}$ input.
CLRMODE	D8	0	Clear mode bit. Set to 1 and drive the external $\overline{\text{CLR}}$ input low to force the DAC output to the value stored in the clear register. Set to 0 and drive the external $\overline{\text{CLR}}$ input low to force the DAC output to 0V in voltage mode or 0mA/4mA depending on output-current mode.
RCLR	D7	0	Remain in clear bit. Set to 1 to remain in the clear state. The RCLR bit determines the steps required to exit the clear state. See the \overline{CLR} Input section.
FAULTEN	D6	0	Fault output enable. Set to 1 to enable the FAULT output functionality. Set to 0 to disable the FAULT output functionality. In single supply mode, set to 0 to disable the FAULT pin function.
CLRFLAGEN	D5	0	Clear flag enable. Set to 1 to enable the FAULT output to report when the device is in the clear state.
FAULTV	D4	0	Output voltage fault bit (read only). The FAULTV bit is set to 1 when FAULT triggers due to an OUTV short-circuit condition. The FAULTV bit is a don't-care bit for control-register write commands. In single supply mode, FAULTV = 1 must be ignored.
FAULTI	D3	0	Output-current fault bit (read only). The FAULTI bit is set to 1 when FAULT triggers due to an OUTI open-circuit condition. The FAULTI bit is a don't-care bit for the control register write commands. In single supply mode, monitor the FAULTI bit for any FAULTI condition.
CLEARST	D2	0	Clear state bit (read only). The CLEARST bit is set to 1 when $\overline{\text{CLR}}$ is low and CLREN = 0. The CLRST bit is a don't-care bit for control register write commands.
X	D1, D0	0	Not used.

Input Register (Read/Write)

Write to the input register to store the DAC code. Transfer the value written to the input register to the DAC register by pulling the LDAC input low or by writing to the load DAC register (0x05). Set the command byte to 0x03 to write to the input register. Set the command byte to 0x07 to read from the input register. Bits D15–D0 contain the straight binary data (see Table 5).

DAC Register (Read/Write)

Write to the <u>DAC</u> register to update the OUTV and OUTI outputs after <u>CS</u> returns high. Set the command byte to 0x04 to write to the DAC register. Set the command byte to 0x08 to read from the DAC register. Bits D15–D0 contain the straight binary data (see Table 6).

Load DAC Register (Write)

Write to the load DAC register to transfer the input register data to the DAC register and update the DAC out-

put. Set the command byte to 0x05 to write to the load DAC register. Bits D15-D0 are don't-care bits.

Clear Register (Read/Write)

Write to the clear register to set the DAC output value when the $\overline{\text{CLR}}$ hardware input is pulled low (forcing the MAX5661 into the clear state). Set the command byte to 0x06 to write to the clear register. Set the command byte to 0x09 to read the clear register. Bits D15–D0 contain the straight binary data (see Table 7).

No Operation

Set the command byte to 0x0F or 0x00 to perform a nooperation command. After writing the command byte and 2 data bytes (16 don't-care bits), read out the shift register's contents on the following 24-bit cycle.

Table 5. Input Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
IN15-IN0	D15-D0	0000 0000 0000 0000 (unipolar/current) 1000 0000 0000 0000 (bipolar)	IN15 is the MSB and IN0 is the LSB. Data format is straight binary.

Table 6. DAC Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
DAC15-DAC0	D15-D0	0000 0000 0000 0000 (unipolar/current) 0000 0000 0000 0000 (bipolar)	DAC15 is the MSB and DAC0 is the LSB. Data format is straight binary.

Table 7. Clear Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
CLR15-CLR0	D15-D0	0000 0000 0000 0000 (unipolar/current) 1000 0000 0000 0000 (bipolar)	CLR15 is the MSB and CLR0 is the LSB. Data format is straight binary.

Table 8. Full-Scale Output Trim Register (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
FS_EN + FS_BIT9- FS_BIT0	D9-D0	0000 0000 0000 0000	FS_EN (D15) enables the full-scale output adjustment feature. D9 is the MSB and D0 is the LSB. D9 is straight binary, D8–D0 are inverted binary.

Full-Scale Output Current Trim Register (Write)

Write to the full-scale output trim register to adjust the output voltage or current $\pm 25\%$. Set command bits to 0x06 to write to the output trim register. Bit 15 enables the output trim register. Bits D9–D0 program the 10-bit trim DAC (Table 8).

Table 9. N to D: Full-Scale Output Trim Register Bits Map

N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
D9	D8	D7	D6	D5	D 4	D3	D2	D1	D0

Table 10. Full-Scale Output Variation vs. N and B

DECIMAL VALUE (N)	BIT DECIMAL VALUE (B)	% CHANGE
0	511	-25
256	255	-12.5
511	0	0-
512	1023	0+
767	768	+12.5
1023	512	+25

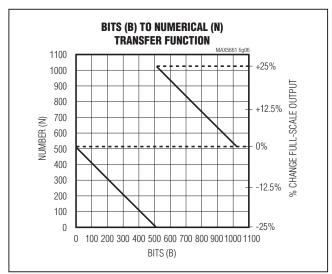


Figure 6. Transfer Function of Bits (B) to Numerical (N) Representation

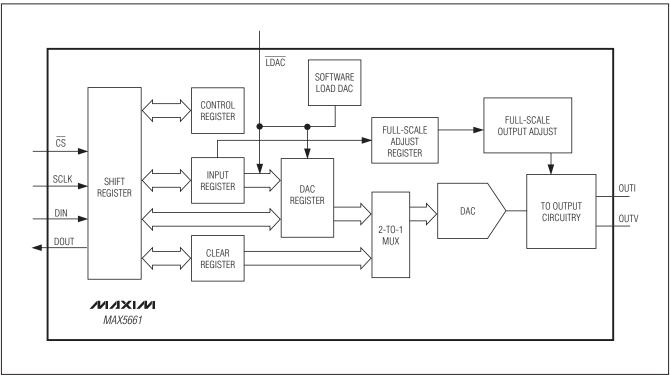


Figure 7. Functional Diagram

Reference Input

Connect an external voltage reference in the +4V to +4.2V range through a $1k\Omega$ series resistor to the buffered REF input. Use a high-accuracy, lownoise +4.096V voltage reference such as the MAX6126AASA41 (3ppm/°C temperature drift and 0.02% initial accuracy) for best 16-bit static accuracy. REF does not accept AC signals. See Table 17 for a listing of +4.096V references.

LDAC Input

The MAX5661 features an active-low load DAC (LDAC) logic input that allows asynchronous updates to the DAC outputs. Drive LDAC high to VCC during normal operation while controlling the MAX5661 using only the serial interface. Drive LDAC low to update the DAC output with the input register data. Hold LDAC low to make the input register transparent and immediately update the DAC output with the input register data. Figure 8 shows the LDAC timing with respect to OUT_.

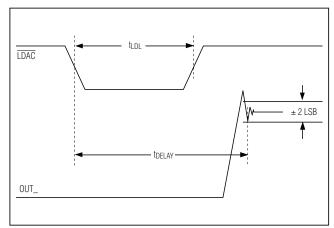


Figure 8. LDAC Timing

CLR Input

The active-low external $\overline{\text{CLR}}$ input asynchronously sets the DAC code to the value in the clear register (software clear) or to the zero state (hardware clear), depending on the control register's CLRMODE bit setting (see Tables 4 and 11). Set the CLRMODE bit to 1 and drive external $\overline{\text{CLR}}$ low to force the output to the value stored in the clear register. Set the CLRMODE bit to 0 and drive the external $\overline{\text{CLR}}$ input low to force the output to the zero state. The zero state value is 0mA in 0 to 20mA current mode, 3.97mA in 4–20mA current mode, or 0V in voltage mode (unipolar or bipolar).

Disable the external $\overline{\text{CLR}}$ input functionality by setting the control register's $\overline{\text{CLREN}}$ bit to 1. Set the $\overline{\text{CLREN}}$ bit to 0 to enable the external $\overline{\text{CLR}}$ input functionality.

After setting the CLREN bit to 0, force the external CLR input low to set the MAX5661 into the clear state. The control register's read-only CLEARST bit is set to 1 while in the clear state. The RCLR (remain in clear) bit determines the steps required to exit the clear state.

With the RCLR bit set to 1, exit the clear state in one of three ways:

- 1) Pull the external CLR input high and then write to the DAC register (0x04) or the load DAC register (0x05) or force LDAC low.
- 2) Pull the external CLR input high and set the RCLR bit low
- 3) Initiate a power-on reset (POR) to reset the RCLR bit to 0.

With the RCLR bit set to 0, exit the clear state one of three ways:

- 1) Set the CLREN bit high.
- 2) Pull the external CLR input high.
- 3) Initiate a power-on reset (POR).

FAULT Output

The open-drain active-low FAULT output asserts low for a current-output open circuit or dropout condition, for a voltage-output short circuit, or when the MAX5661 is in the clear state (see the *CLR Input* section).

Enable and disable the FAULT output with the control register's FAULTEN and CLRFLAGEN bits (see Tables 4, 12, and Figure 9). Set the FAULTEN bit to 1 to enable the FAULT output to report fault conditions on OUTV and OUTI. Set FAULTEN to 0 to disable the FAULT output for fault conditions on OUTV and OUTI. Set the CLRFLAGEN bit to 1 to enable the FAULT output to report when the device is in the clear state. Set CLRFLAGEN to 0 to disable a hardware indication of the clear state. The FAULT output asserts low if CLRFLAGEN = 1 and CLEARST = 1.

Read the control register to determine the source of a FAULT output condition. The FAULTV read-only bit is set to 1 when the voltage output (OUTV) is short-circuited. The FAULTI bit is set to 1 when the current output (OUTI) is open circuited or in a dropout condition (VDDI - VOUTI at 1.3V typ). The FAULT output asserts low if FAULTEN is set to 1 and either the FAULTV bit or FAULTI bit is set to 1.

Table 11. Hardware-Clear and Software-Clear Truth Table

CLEARST BIT (READ)	CLRMODE BIT (READ/WRITE)	HARDWARE CLEAR	SOFTWARE CLEAR		
0 (not in clear state)	X	Х	X		
1 (in clear state)	0	DAC code set to zero state*	_		
1 (in clear state)	1	_	DAC code set by clear register data		

X = Don't care.

^{*}Zero state is 0V in unipolar voltage mode, -10.48V in bipolar voltage mode, and 0mA/4mA depending on output-current mode.

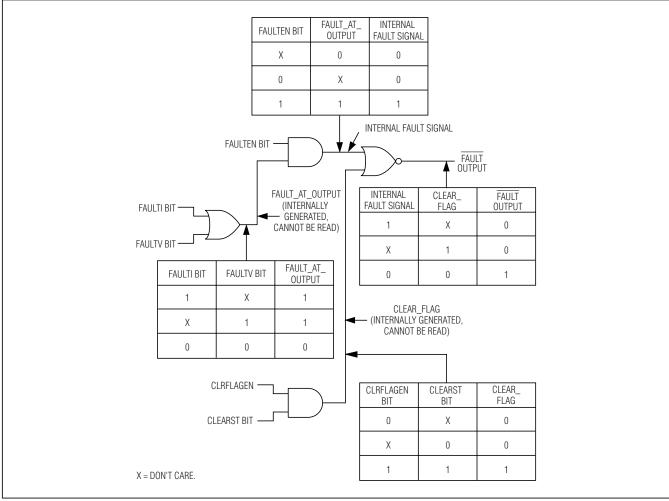


Figure 9. FAULT Output Logic Diagram

Table 12. FAULT Output Truth Table

OUTV SHORT CIRCUITED	OUTI OPEN CIRCUITED OR IN DROPOUT	CLEARST BIT	FAULTEN BIT	CLRFLAGEN BIT	FAULT OUTPUT
No	No	0	X	X	High
No	No	X	X	0	High
X	Χ	1	X	1	Low
X	X	0	0	X	High
No	Yes	X	1	X	Low
X	X	X	0	0	High
Yes	No	X	1	X	Low

X = Don't care. Only one output (OUTV or OUTI) is active at a time.

Output Configurations

The CNF0, CNF1, and OUTI4/0 hardware inputs determine whether the hardware or software controls the MAX5661 DAC outputs (see Table 13). The CNF0 and CNF1 inputs enable and disable the DAC outputs or allow software control of the outputs (see Table 14). The OUTI4/0 input sets the current range of the OUTI output. Hardware inputs take precedence over the software commands.

The V_{CC} digital supply powers the CNF1, CNF0, and OUTI4/ $\overline{0}$ inputs. If V_{CC} = 0V, the DAC outputs enter the zero state and all register bits are set to 0. The zero state of the voltage output (OUTV) is 0V. The zero state of the current output (OUTI) is 0mA when OUTI4/ $\overline{0}$ = AGND or 4mA when OUTI4/ $\overline{0}$ = V_{DDI}.

Table 13. Output Configuration

CONTROL SIGNAL	HARDWARE INPUT/SOFTWARE BIT	DESCRIPTION	DETAILS
CNF1	Hardware input	Enables/disables the DAC	CNF1, CNF0: 00 = both outputs disabled 01 = OUTI active, set to 0 to 20mA range
CNF0	Hardware input	OUTV and OUTI outputs.	10 = OUTV active, set to bipolar mode 11 = outputs controlled by serial interface
OUTI4/0	Hardware input	Sets the OUTI current range.	Set the OUTI4/0EN bit to 0 (default power-up state) to enable the OUTI4/0 hardware input. Connect the OUTI4/0 hardware input to AGND to set the OUTI current range to 0 to 20mA. Connect the OUTI4/0 hardware input to V _{DDI} to set the OUTI current range to 4–20mA. Set the OUTI4/0EN bit to 1 to disable the OUT14/0 hardware input. Connect OUTI4/0 to AGND when controlling the current output through software.
OUTI4/0EN	Software bit	Enables and disables the OUTI4/0 input.	Set the OUTI4/0EN bit to 0 (default power-up state) to enable the OUTI4/0 hardware input. Set to 1 to disable the OUTI4/0 hardware input.
OUTVON	Software bit	Enables and disables the DAC OUTV and OUTI	When the CNF1 and CNF0 hardware inputs are high, the OUTION and OUTVON bits control the DAC output OUTI and OUTV settings. OUTVON, OUTION:
OUTION	Software bit	outputs.	00 = both outputs powered down 01 = OUTI active 10 = OUTV active 11 = both outputs powered down
B/U	Software bit	Sets the voltage output to unipolar mode or bipolar mode.	Set \overline{B}/U to 0 to set the OUTV output to bipolar mode (±10.48V). Set \overline{B}/U to 1 to set the OUTV output to unipolar mode (0 to +10.48V).
I4TO20BIT	Software bit	Sets the OUTI current range through software.	Set I4TO20BIT to 0 to set the OUTI current range from 0 to 20mA. Set I4TO20BIT to 1 to set the OUTI current range from 4–20mA.

CNF0/CNF1 Hardware Inputs

The CNF0 and CNF1 inputs enable the DAC's voltage (OUTV) or current (OUTI) outputs. Drive CNF0 and CNF1 low to disable both the OUTV and OUTI outputs. Drive CNF0 high and CNF1 low to enable the OUTI output. Drive CNF0 low and CNF1 high to enable the OUTV output. Drive CNF0 and CNF1 high to control the OUTV and OUTI outputs through the serial interface. Table 14 summarizes the output behavior when programmed by the CNF0/CNF1 hardware inputs.

OUTI Current-Output Configuration

Drive CNF0 high and CNF1 low to enable the OUTI output through the hardware. Alternatively, drive CNF0 and CNF1 high to control OUTI with the serial interface. With CNF1 and CNF0 high, the control register's OUTION bit enables the OUTI output. Set OUTION to 1 to enable the OUTI output. Set OUTION to 0 (default power-up state) to disable the OUTI output.

The OUTI current output derives power from V_{DDI} and V_{DDCORE} (+13.48V to +40V). Connect V_{DDCORE} to V_{DDI} when using the OUTI output.

The control register's OUTI4/OEN bit (see Tables 4 and 13) determines whether the OUTI4/O hardware input or the control register's I4TO20BIT bit controls the OUTI current range. Set the OUTI4/OEN bit to 0 (default power-up state) to control the current range through the OUTI4/O hardware input. Connect the OUTI4/O hardware input to AGND to select the 0 to 20mA mode. Connect the OUTI4/O hardware input to VDDI to select the 4–20mA mode.

Set the OUTI4/0EN bit to 1 to allow software control of the OUTI current range through the I4TO20BIT bit (see Table 13). Set I4TO20BIT to 0 to select the 0 to 20mA mode. Set I4TO20BIT to 1 to select the 4–20mA mode.

OUTV Voltage-Output Configuration

Drive CNF0 low and CNF1 high to enable the OUTV output through the hardware (see Table 14). Alternatively, drive CNF0 and CNF1 high to control OUTV with the serial interface. With CNF1 and CNF0 high, the control register's OUTVON bit enables the OUTV output. Set OUTVON to 1 to enable the OUTV output. Set OUTVON to 0 (default power-up state) to disable the OUTV output.

The OUTV output derives power from VDDV, VSSV, and VDDCORE. Connect VDDCORE to VDDV (+13.48V to +15.75V) when using the OUTV output. Always connect a negative supply to VSSV (-13.48V to -15.75V) (see Table 16).

The control register's \overline{B}/U bit sets OUTV for bipolar or unipolar mode. Set \overline{B}/U to 0 (default power-up state) to select the bipolar output range ($\pm 10.48V$). Set \overline{B}/U to 1 to select the unipolar output range (0 to $\pm 10.48V$).

Output Transfer Functions

The DAC output voltage/current is a function of the various hardware control inputs and digital inputs in the control register (see Table 13). The transfer functions below assume that the outputs are on, and a reference voltage of +4.096V is applied to the reference input. For the voltage output, the sense input is at the same potential as the DAC output (OUTV = SVP and AGND = SVN). Table 15a details the bipolar output voltage transfer function. Table 15b details the unipolar output voltage transfer function. Table 15c details the 0 to 20mA current-range transfer function. Table 15d details the 4mA to 20mA current-range transfer function.

Table 14. CNF1/CNF0 Hardware Settings

CNF1	CNF0	OUTV, OUTI SETTING	
DGND	DGND	Both DAC outputs disabled.	
DGND	Vcc	OUTI enabled. OUTV disabled.	
Vcc	DGND	OUTV enabled. OUTI disabled.	
Vcc	Vcc	DAC outputs controlled by the serial interface.	

Table 15a. Bipolar Voltage Output

DAC CODE (DECIMAL VALUE)	OUTPUT VOLTAGE (V)	RANGE	
65535	10.47984	Overrange	
64769	10.23485	Overrange	
64768	10.23453	Nominal range	
64767	10.23421	Nominal range	
48769	5.117585	Nominal range	
48768	5.117266	Nominal range	
48767	5.116946	Nominal range	
35969	1.023773	Nominal range	
35968	1.023453	Nominal range	
35967	1.023133	Nominal range	
32769	0.00032	Nominal range	
32768	0	Nominal range	
32767	-0.00032	Nominal range	
29569	-1.02313	Nominal range	
29568	-1.02345	Nominal range	
29567	-1.02377	Nominal range	
16769	-5.11695	Nominal range	
16768	-5.11727	Nominal range	
16767	-5.11759	Nominal range	
769	-10.2342	Nominal range	
768	-10.2345	Nominal range	
767	-10.2349	Underrange	
0	-10.4802	Underrange	

Table 15b. Unipolar Voltage Output

DAC CODE (DECIMAL VALUE)	OUTPUT VOLTAGE (V)	RANGE
65535	10.48	Overrange
64001	10.23469	Overrange
64000	10.23453	Nominal range
32001	5.117425	Nominal range
32000	5.117266	Nominal range
31999	5.117106	Nominal range
6401	1.023613	Nominal range
6400	1.023453	Nominal range
6399	1.023293	Nominal range
1	0.00016	Nominal range
0	0	Nominal range

Table 15c. 0 to 20mA Current Output

DAC CODE (DECIMAL)	ACTUAL OUTPUT CURRENT (mA)	RANGE	EXTENSION OF OUTPUT CURRENT LINEAR RANGE (mA)
65535	20.449688	Overrange	20.449688
64001	19.970313	Overrange	19.970313
64000	19.970000	Nominal range	19.970000
63999	19.969688	Nominal range	19.969688
32001	9.970313	Nominal range	9.970313
32000	9.970000	Nominal range	9.970000
31999	9.969688	Nominal range	9.969688
12801	3.970313	Nominal range	3.970313
12800	3.970000	Nominal range	3.970000
12799	3.969688	Nominal range	3.969688
97	0.000313	Nominal range	0.000313
96	0.000000	Nominal range	0.00000
95	0.000000	Underrange	-0.000313
80	0.000000	Underrange	-0.005000
60	0.000000	Underrange	-0.011250
40	0.000000	Underrange	-0.017500
30	0.000000	Underrange	-0.020625
0	0.000000	Underrange	-0.030000

Table 15d. 4-20mA Current Output

DAC CODE (DECIMAL)	OUTPUT CURRENT (mA)	RANGE	
65535	20.449688	Overrange	
64000	20.063690	Overrange	
63634	19.971655	Nominal range	
60000	19.057835	Nominal range	
50000	16.543196	Nominal range	
40000	14.028556	Nominal range	
30000	11.513917	Nominal range	
20000	8.999278	Nominal range	
16000	7.993423	Nominal range	
5000	5.227320	Nominal range	
500	4.095732	Nominal range	
238	4.029848	Nominal range	
200	4.020293	Underrange	
100	3.970000	Underrange	
80	3.970000	Underrange	
60	3.970000	Underrange	
30	3.970000	Underrange	
0	3.970000	Underrange	

Measuring Zero-Code Current (0 to 20mA Mode)

After setting the MAX5661 for 0 to 20mA current-range mode, determine the LSB size as follows:

- 1) Measure IOUT at full scale (FS).
- 2) Measure IOUT at code 192.
- 3) Measure IOUT at code 193:

$$I_{LSB} = \frac{I_{OUT} \text{ at FS} - I_{OUT} \text{ at } 192}{(2^{16} - 1) - 192}$$

If I_{OUT} (code 193) - I_{OUT} (code 192) > 0.5 I_{LSB} , I_{OUT} (code 192) is inside the linear region of the I_{OUT} transfer curve.

Obtain the straight-line equation from I_{OUT} (FS) and I_{OUT} (192) and substituting code 0 for I_{OUT} (zero scale) in the equation:

$$(I - I_{OUT} \text{ at } 192) = \left(\frac{I_{OUT} \text{ at } FS - I_{OUT} \text{ at } 192}{65535 - 192}\right) \times (\text{code} - 192)$$

$$I_{OUT} \text{ at } ZS = (I_{OUT} \text{ at } 192 - I_{OUT} \text{ at } FS) \times 0.0029383 + I_{OUT} \text{ at } 192$$

The expected current is -30µA (typ).

Applications Information

Power-Supply Sequencing and Bypassing

After connecting all ground inputs, apply the analog supply voltages VSSV first followed by the most positive supply, the second most positive supply, etc. Before applying power, connect the VDDCORE supply to either VDDV or VDDI, as shown in Table 16, depending on whether the current output or voltage output is used. Do not apply VDDCORE separate from the main supply (VDDV/VSSV or VDDI) in the preferred configuration (Table 16). Ensure that there are no unconnected power-supply connections when powering the MAX5661. If VSSV cannot be powered first, connect a Schottky diode between VSSV and AGND.

Daisy Chaining Multiple MAX5661 Devices

In standard SPI-/QSPI-/MICROWIRE-compatible systems, a microcontroller (µC) communicates with its slave devices through a 3- or 4-wire serial interface. The typical interface includes a chip select signal (CS), a serial clock (SCLK), a data input signal (DIN), and sometimes a data signal output (DOUT). In this system, the µC allots an independent chip-select signal to each slave device so that they can be addressed individually (see Figure 10). Only the slaves with their $\overline{\text{CS}}$ inputs asserted low acknowledge and respond to the activity on the serial clock and data lines. This is simple to implement when there are very few slave devices in the system. An alternative programming method is daisy chaining. Daisy chaining, in serial-interface applications, is a method of propagating commands through multiple devices connected in series (see Figure 11). Daisy chaining reduces $\overline{\text{CS}}$ and DIN line routing, and saves board space when using the MAX5661.

Daisy chain multiple MAX5661 devices by connecting the DOUT of one device to the DIN of the next. Connect the SCLK of all devices to a common clock and connect the $\overline{\text{CS}}$ from all devices to a common chip-select line. Data shifts out of DOUT 24.5 clock cycles after it is shifted into DIN on the falling edge of SCLK. Hold $\overline{\text{CS}}$ low until each slave in the chain receives its 24-bit word (8 command bits and 16 data bits). In this configuration, the μC only needs three signals ($\overline{\text{CS}}$, SCLK, and DIN) to control all the slaves in the network. The SPI-/QSPI-/MICROWIRE-compatible serial interface normally works at up to 10MHz, but must be slowed to 6MHz if daisy chaining. DOUT is high impedance when $\overline{\text{CS}}$ is high.

Figure 10 details a method of controlling multiple MAX5661 devices using separate \overline{CS} lines. This method allows writes to and reads from each device without shifting data through the other device's shift register. Figure 10 shows the \overline{FAULT} outputs shorted together. This configuration requires a read from each device to determine which one has the fault condition and saves an optocoupler in isolated applications. It is not necessary to short the \overline{FAULT} outputs together.

 Table 16. Application Modes and Supply-Voltage Limits

APPLICATION MODE	V _{DDV}	V _{SSV}	V _{DDI}	V _{DDCORE}
Voltage from OUTV	+13.48V to +15.75V	-13.48V to -15.75V	V_{DDV}	V_{DDV}
Current from OUTI (Single Supply)	AGND	AGND	+13.48V to +40V	V _{DDI}
Voltage from OUTV and Current from OUTI*	+13.48V to +15.75V	-13.48V to -15.75V	V _{DDV} to +40V	V _{DDV}

^{*}On-the-fly switching. Only one output is active at a time.

Figure 11 shows a method of daisy chaining multiple MAX5661 devices using a single $\overline{\text{CS}}$ and SCLK line with the $\overline{\text{FAULT}}$ outputs shorted together. Connect DOUT from IC1 to DIN of IC2, and DOUT from IC2 to DIN of

IC3. Hold $\overline{\text{CS}}$ low for three 24-bit write cycles to load data into all three devices. Due to the latency of reading and writing to the different devices, using separate lines for each $\overline{\text{FAULT}}$ output does not save time.

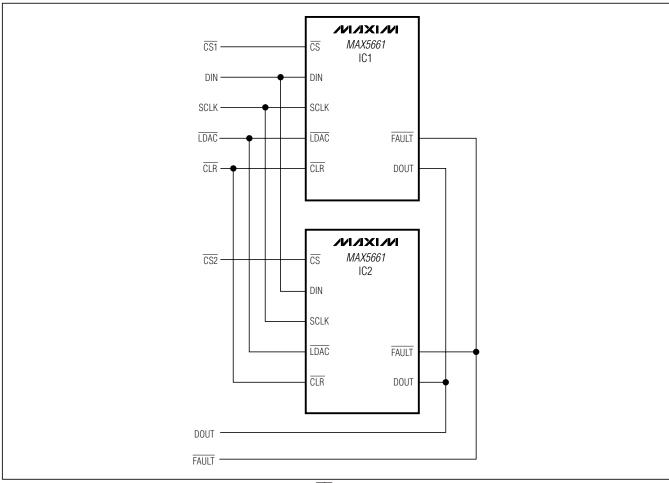


Figure 10. Address Two MAX5661 Devices Through Separate CS Lines

Driving Inductive Loads from IOUT

When driving inductive loads > $275\mu H$ with the current output (I_{OUT}), connect a 1nF capacitor between V_{DDI} and I_{OUT} for optimal performance.

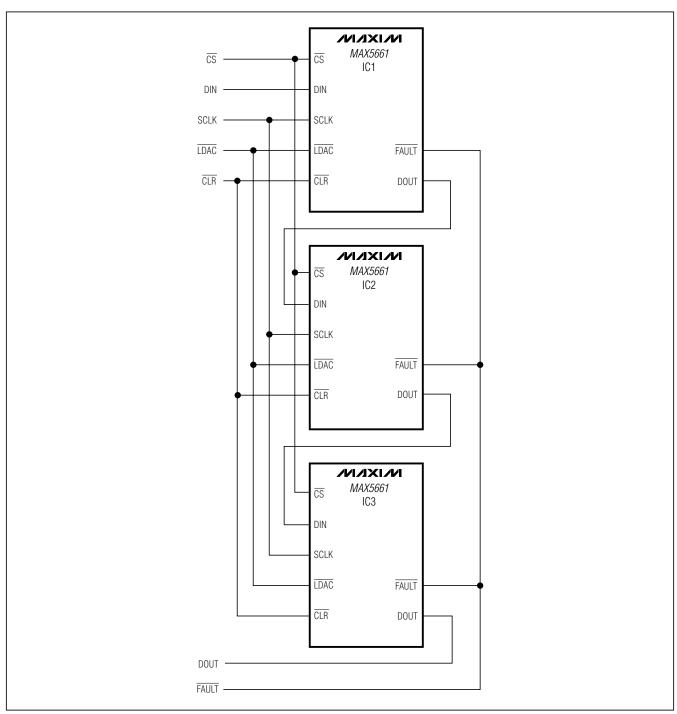


Figure 11. Address Three MAX5661 Devices Through Separate CS Lines

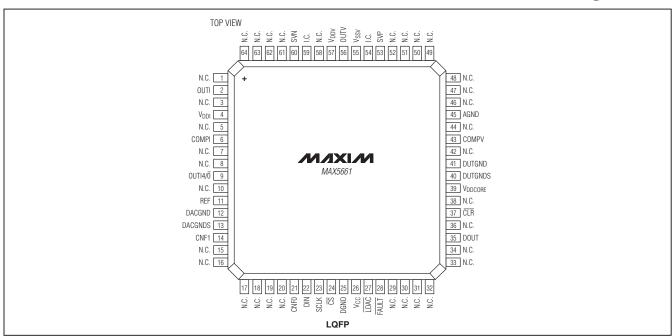
Table 17. +4.096V Reference Selector Guide

PART	SUPPLY VOLTAGE RANGE (V)	TEMPERATURE DRIFT (ppm/°C max)	INITIAL ACCURACY (%)	FEATURES	
MAX6341	+8 to +36	1	0.02	Ultra-low drift, 2.4µV _{P-P} output noise	
MAX6241	+8 to +36	3	0.02	Low drift, 2.4µV _{P-P} output noise	
MAX6174	+4.3 to +40	3	0.06	High-precision reference with temperature sensor	
MAX6133_41	+4.3 to +12.6	3	0.04	Ultra-low drift, µMAX®	
MAX6126_41	+4.3 to +12.6	3	0.02	Ultra-low noise, µMAX	
MAX6043_41	+6 to +40	3	0.05	High voltage, low drift	
MAX6143_41	+6 to +40	8	0.1	High precision	
MAX6033_41	+4.3 to +12.6	10	0.04	10mA output current, ultra-low drift, SOT23	
MAX6041	+4.3 to +12.6	20	0.2	Low power, low drift, low dropout	
MAX6064	+4.3 to +12.6	20	0.2	5mA current output, precision SOT23	
MAX6220	+8 to +40	20	0.1	-40°C to +125°C, 15mA output	
MAX6037_41	+4.3 to +5.5	25	0.2	SOT23 with shutdown	
MAX6034_41	+4.3 to +5.5	30	0.2	Low supply current in SC70	
MAX6029	+4.3 to +12.6	30	0.15	Ultra-low supply current, SOT23	

Chip Information

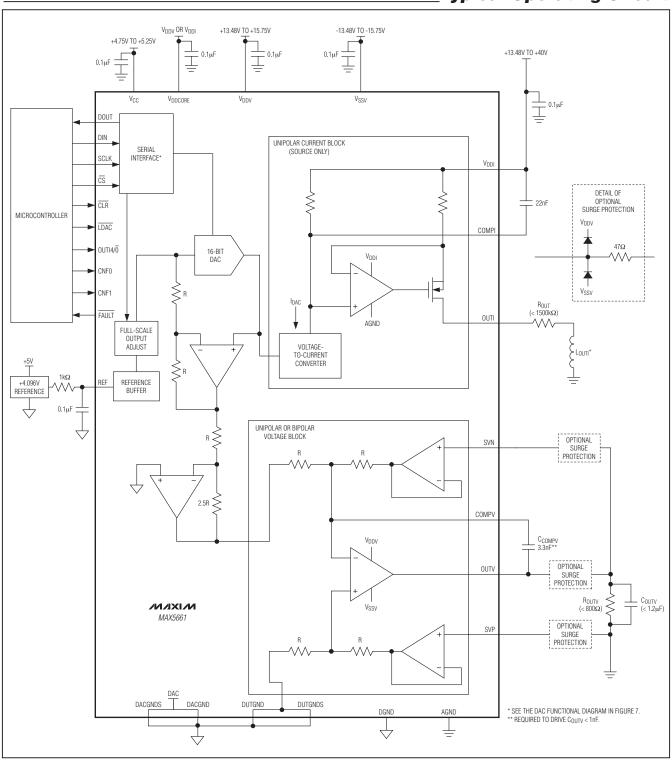
PROCESS: BiCMOS

Pin Configuration



 μMAX is a registered trademark of Maxim Integrated Products, Inc.

Typical Operating Circuit



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
64 LQFP	C64-8	<u>21-0083</u>

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/08	Initial release	_
1	5/09	Clarified how the part operates in single supply mode	18, 24

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