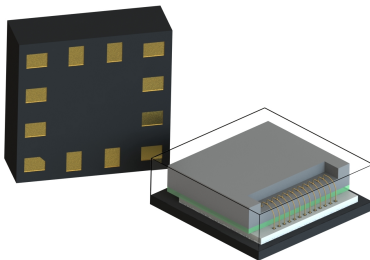


Ultra-compact two-axis gyroscope for optical image stabilization



LGA-12 (2.0 x 2.0 x 0.7 mm)

Features

- ± 100 dps / ± 200 dps full-scale range
- 5 degree phase delay
- 3.8 mdps/ $\sqrt{\text{Hz}}$ rate noise density
- Wide supply voltage range: 1.7 V to 3.6 V
- Low-voltage compatible IOs
- 3- and 4-wire SPI digital interface
- Embedded temperature sensor
- Embedded self-test
- Integrated low-pass filters with user-selectable bandwidth
- Power-down and sleep modes for smart power saving
- ECOPACK[®], RoHS and “Green” compliant

Applications

- Optical image stabilization

Description


The **L20G20IS** is a two-axis MEMS gyroscope for optical image stabilization applications.

It includes a sensing element and an IC interface capable of providing the measured angular rate to the application through an SPI digital interface.

The unique sensing element is manufactured using a dedicated micromachining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

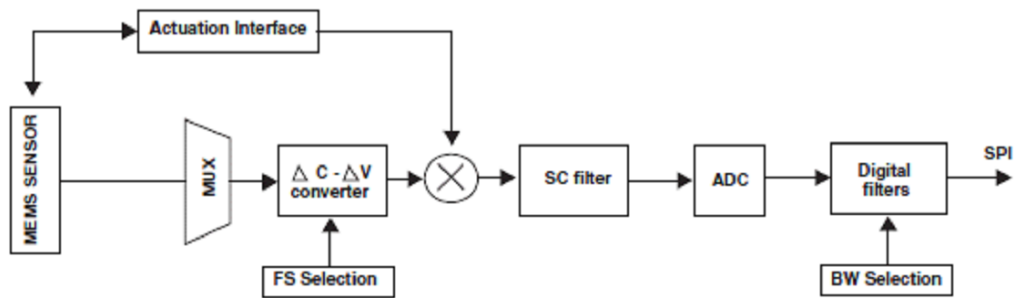
The L20G20IS is available in a plastic land grid array (LGA) package and can operate over a temperature range of -40 °C to +85 °C.

| Product status link | | |
|---|--------------------|---------------|
| L20G20IS | | |
| Product summary | | |
| Order code | L20G20IS | L20G20ISTR |
| Temperature range | -40 °C to +85 °C | |
| Package | 2.0 x 2.0 x 0.7 mm | |
| Packing | Tray | Tape and reel |
| Product label | | |
|  | | |

1 Block diagram and pin description

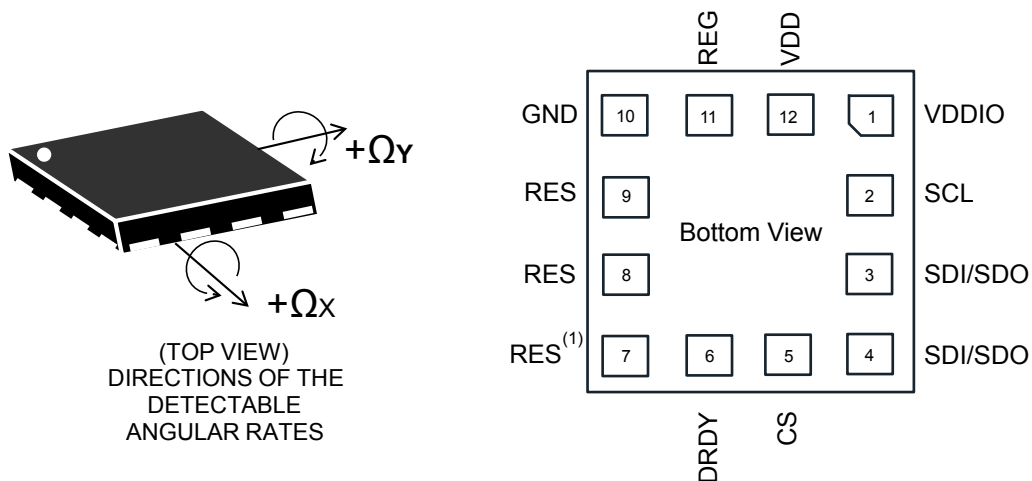
1.1 System block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections



1. Leave pin electrically unconnected and soldered to PCB.

Table 1. Pin description

| Pin # | Pin name | Function |
|-------|--------------------|---|
| 1 | VDDIO | Power supply for I/O pins |
| 2 | SCL | Clock line for SPI interface |
| 3 | SDI/SDO | Serial data input (SDI) 3-wire interface serial data output (SDO) |
| 4 | SDO | Serial data output (SDO) |
| 5 | CS | Chip-select line |
| 6 | DRDY | Data-ready signal |
| 7 | RES ⁽¹⁾ | Leave unconnected |
| 8 | RES | Connect to GND |
| 9 | RES | Connect to GND |
| 10 | GND | 0 V power supply |
| 11 | REG | Capacitance connection pin for internal regulator |
| 12 | VDD | Power supply |

1. Leave pin electrically unconnected and soldered to PCB.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

The values listed in the table below are specified for $V_{dd} = 2.4\text{ V}$, $T_{amb} = 25\text{ °C}$ unless otherwise specified.

Table 2. Mechanical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--------|--|---|------|---------------------|------|--------------------------|
| FS | Measurement range | | | ±100 | | dps |
| | | | | ±200 | | |
| So | Sensitivity | FS = ±100 dps | | 262 | | LSB/dps |
| | | FS = ±200 dps | | 131 | | |
| So | Sensitivity initial tolerance ⁽²⁾ | | | ±1.5 | | % |
| TSo | Sensitivity drift vs. temp. ⁽³⁾ | Delta from 25°C; range [-20°C to 75°C] | | 1 | | % |
| DVoff | Digital zero-rate level ⁽⁴⁾ | | | ±5 | | dps |
| TDVoff | Digital zero-rate level drift vs. temp. | Delta from 25°C; range [-20°C to 75°C] | | 0.03 | | dps/°C |
| Rn | Rate noise density ⁽⁵⁾ | at 20 Hz | | 3.8 | | mdps/ $\sqrt{\text{Hz}}$ |
| PhD | Phase delay ⁽⁶⁾ | at 20 Hz (450 Hz BW selected) | | 5 | | deg |
| ODR | Output data rate | | | 9.33 | | kHz |
| Ton | Turn-on time | | | 35 | | ms |
| ST | Gyroscope self-test | | 20 | | 90 | dps |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. Sensitivity value after factory calibration test and trimming.
3. Measurements are performed in a uniform temperature setup and they are based on characterization data with a limited number of samples, not measured during final test production.
4. Zero-rate level value after factory calibration test and trimming.
5. Guaranteed by design.
6. Refer to [Section 4 L20G20IS filtering chain](#) for filtering details.

2.2 Electrical characteristics

The values listed in the table below are specified for $V_{dd} = 2.4\text{ V}$, $T_{amb} = 25\text{ °C}$ unless otherwise specified.

Table 3. Electrical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--------------------|-----------------------------------|---------------------------------------|--------------|---------------------|-------------|------|
| VDD | Supply voltage | | 1.7 | | 3.6 | V |
| VDD_IO | I/O pins supply voltage | | 1.7 | | 3.6 | V |
| I _{dd} | Supply current in normal mode | | | 1.4 | | mA |
| I _{ddPDN} | Supply current in power-down mode | | | 5 | | uA |
| V _{IH} | Digital high-level input voltage | | 0.7 *VDD_IO | | | V |
| V _{IL} | Digital low-level input voltage | | | | 0.3 *VDD_IO | V |
| V _{OH} | High-level output voltage | I _{OH} = 4 mA ⁽²⁾ | VDD_IO - 0.2 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 4 mA ⁽²⁾ | | | 0.2 | V |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed
2. 4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL} .

2.3 Temperature sensor characteristics

The values listed in the table below are specified for $V_{dd} = 2.4\text{ V}$, $T_{amb} = 25\text{ °C}$ unless otherwise specified.

Table 4. Temperature sensor characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--------|--|----------------|------|---------------------|------|----------|
| TSDr | Temperature sensor output change vs. temp | | | 0.0625 | | °C/digit |
| TODR | Temperature refresh rate | | | 70 | | Hz |
| TACC | Temperature absolute accuracy ⁽²⁾ | | | ±4 | | °C |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed
2. The output of the temperature is 0 at 25 °C.

2.4 SPI - serial peripheral interface

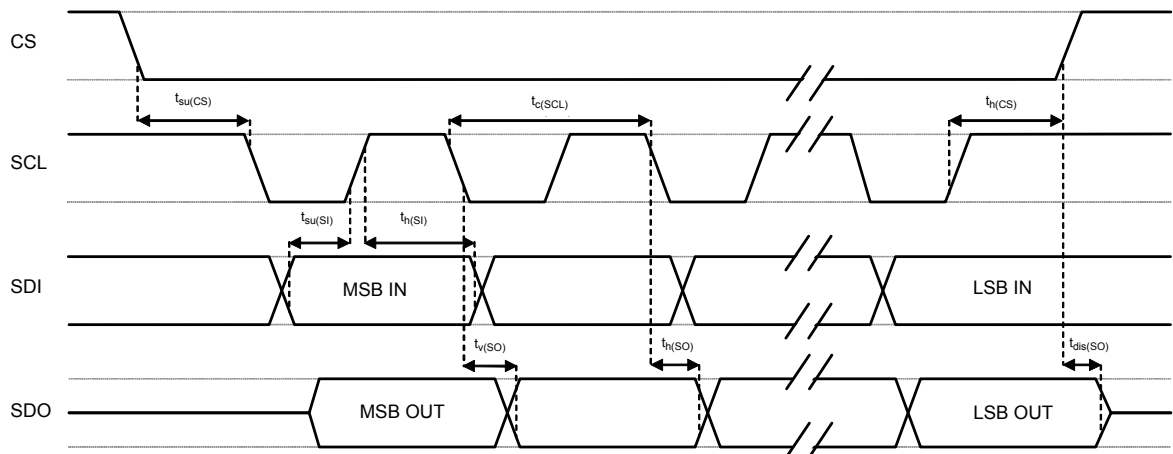
Subject to general operating conditions for V_{dd} and T_{op}.

Table 5. SPI slave timing values

| Symbol | Parameter | Value ⁽¹⁾ | | Unit |
|---------------|-------------------------|----------------------|-----|------|
| | | Min | Max | |
| $t_{c(SCL)}$ | SPI clock cycle | 100 | | ns |
| $f_{c(SCL)}$ | SPI clock frequency | | 10 | MHz |
| $t_{su(CS)}$ | CS setup time | 5 | | ns |
| $t_{h(CS)}$ | CS hold time | 8 | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | |
| $t_{v(SO)}$ | SDO valid output time | | 50 | |
| $t_{h(SO)}$ | SDO output hold time | 6 | | |
| $t_{dis(SO)}$ | SDO output disable time | | 50 | |

1. Values are guaranteed at 10 MHz clock frequency for SPI, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·V_{dd_IO} and 0.8·V_{dd_IO}, for both input and output ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

| Symbol | Ratings | Maximum value | Unit |
|------------------|--|---------------------|----------|
| Vdd | Power supply | -0.3 to 4.8 | V |
| Vdd_IO | Power supply for I/O pins | -0.3 to Vdd | V |
| Vin | Input voltage on: (CS, SDI/SDO, SDO, SCL) | -0.3 to Vdd_IO +0.1 | V |
| T _{STG} | Storage temperature range | -40 to +125 | °C |
| Sg | Acceleration <i>g</i> for 0.2 ms | 10,000 | <i>g</i> |
| ESD | Electrostatic discharge protection | 2 (HBM) | kV |

Note: Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology and functionality

3.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

3.2 Zero-rate level

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of highly accurate MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor on a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

3.3 Data-ready interrupt and synchronous reading

On the L20G20IS the angular rate data can be retrieved using a synchronous read. To perform a synchronous read, [CTRL4_OIS \(0Eh R/W\)](#) (DRDY_EN) has to be set to '1' in order to enable the data-ready interrupt on the DRDY pin (refer to [Figure 7. L20G20IS electrical connections](#)). To properly perform a synchronous read, the angular rate data have to be read every time the DRDY pin goes high.

The DRDY signal can be latched (default condition) or pulsed if [CTRL1_OIS \(0Bh R/W\)](#)(DR_DRDY) is set to '1'. When a latched condition is selected, the interrupt goes low when the high part of one of the output channels is read (OUT_X_H (04h) or OUT_Y_H (06h)) and returns high when new data is generated. When a pulsed condition is selected, the interrupt behavior is independent from the read operations and remains high for 75 µsec every time new data is generated. The DRDY pin is set by default as push-pull output, but it can be configured as open-drain output by setting [CTRL4_OIS \(0Eh R/W\)](#) (DRDY_OD) to '1'.

3.4 Temperature sensor

The temperature data can be retrieved from the [TEMP_OUT_L \(01h R\)](#), [TEMP_OUT_H \(02h R\)](#) registers, as two's complement data in 12-bit format left-justified. The output of the temperature sensor is 0 at 25 °C.

4 L20G20IS filtering chain

The filtering chain for the L20G20IS appears in the figure below.

Figure 6. Filtering chain block diagram

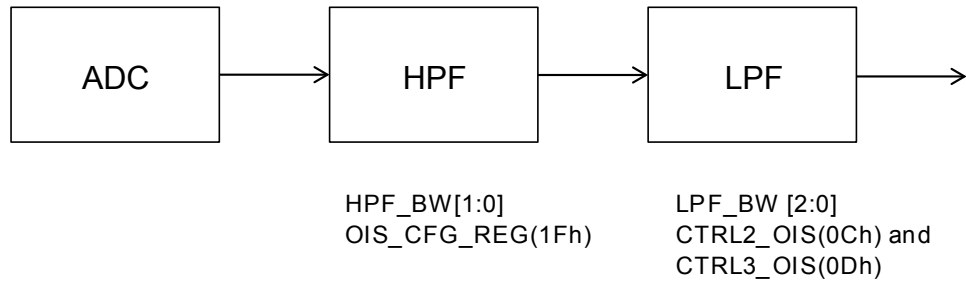


Table 7. Digital LPF configuration

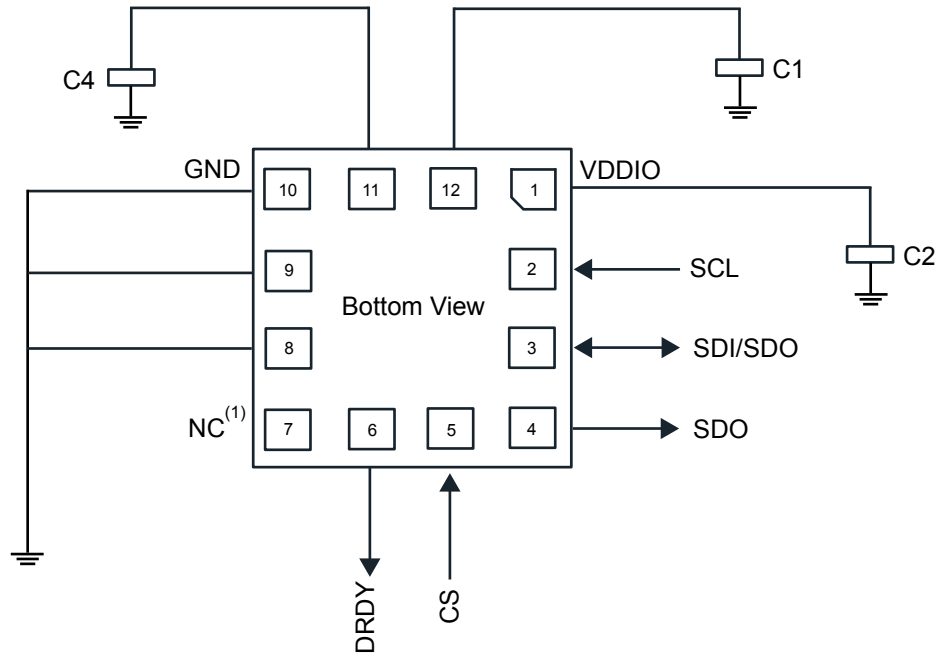
| LPF_BW2 | LPF_BW1 | LPF_BW0 | LPF BW [Hz] | Phase delay [°] |
|---------|---------|---------|-------------|-----------------|
| 0 | 0 | 0 | 290 | 7 @ 20 Hz |
| 0 | 0 | 1 | 210 | 9 @ 20 Hz |
| 0 | 1 | 0 | 160 | 11 @ 20 Hz |
| 0 | 1 | 1 | 450 | 5 @ 20 Hz |
| 1 | x | x | 1150 | 1 @ 10 Hz |

Table 8. Digital HPF configuration

| HPF_BW[1:0] | HPF cutoff [Hz] |
|-------------|-----------------|
| 00 | 0.023 |
| 01 | 0.091 |
| 10 | 0.324 |
| 11 | 1.457 |

5 Application hints

Figure 7. L20G20IS electrical connections



| External Component | Value | Purpose |
|--------------------|------------------|--------------------|
| C1 | 100nF | Decoupling |
| C2 | 100nF | Decoupling |
| C4 | 100nF (5V class) | Internal Regulator |

1. Leave pin electrically unconnected and soldered to PCB.

Power supply decoupling capacitors (C1, C2) should be placed as near as possible to the supply pins on the device (common design practice).

5.1 Internal pin status

Table 9. Internal pin status

| Pin # | Pin name | Function | Status |
|-------|----------|--|--------------------------------|
| 1 | VDDIO | Power supply for I/O pins | |
| 2 | SCL | Clock line for SPI interface | Default: input without pull-up |
| 3 | SDI/SDO | Serial data input (SDI) 3-wire interface serial data output (SDO) | Default: input without pull-up |
| 4 | SDO | Serial data output (SDO) | Default: input without pull-up |
| 5 | CS | Chip-select line | Default: input without pull-up |
| 6 | DRDY | Data ready signal | Default: push-pull to gnd |
| 7 | RES | Leave unconnected | Default: push-pull to gnd |
| 8 | RES | Connect to GND | Internally unconnected |
| 9 | RES | Connect to GND | Internally unconnected |
| 10 | GND | 0 V power supply | |
| 11 | REG | Capacitance connection pin for internal regulator | |
| 12 | VDD | Power supply | |

6 Digital interfaces

The registers embedded inside the L20G20IS may be accessed through the SPI serial interfaces.

Table 10. Serial interface pin description

| Pin name | Pin description |
|----------|--|
| CS | Chip-select line |
| SCL | SPI serial port clock |
| SDI/SDO | Serial data input (SDI) 3-wire interface serial data output (SDO) |
| SDO | Serial data output (SDO) |

6.1 SPI bus interface

The SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface connects to applications using 4 wires: **CS**, **SCL**, **SDI** and **SDO**.

CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SCL** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SCL** and should be captured at the rising edge of **SCL**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SCL**. The first bit (bit 0) starts at the first falling edge of **SCL** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SCL** just before the rising edge of **CS**.

bit 0: \overline{RW} bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive SDO at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

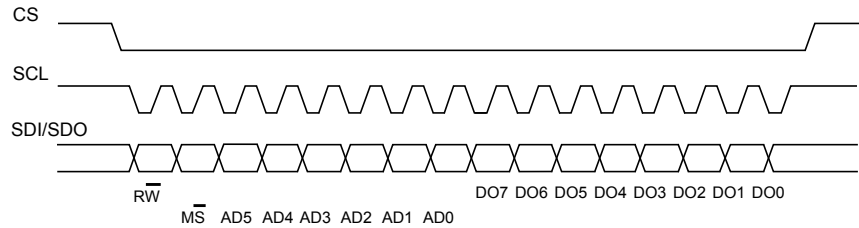
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The function and the behavior of SDI and SDO remain unchanged.

6.1.1 SPI read

3-wire mode is entered by setting the (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 8. SPI read protocol



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: \overline{MS} bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

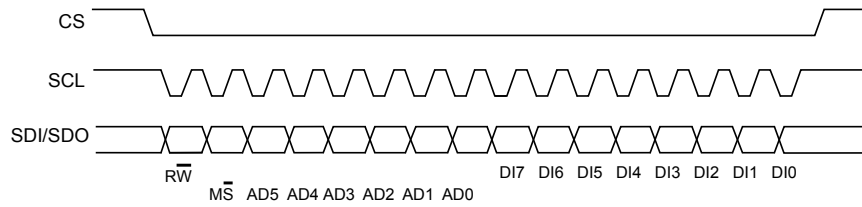
bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

A multiple read command is also available.

6.1.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

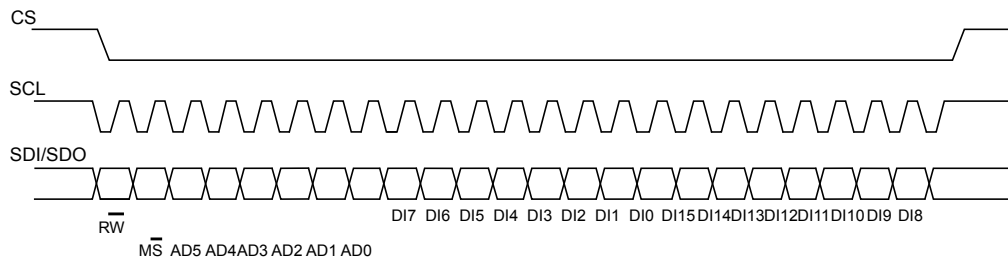
bit 1: \overline{MS} bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 10. Multiple byte SPI write protocol (2-byte example)



7 Register mapping

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 8 bits, is used to identify them and to write the data through the serial interface.

Table 11. Register address map

| Name | Type | Register address [Hex] | Default [Hex] |
|-----------------|------|---------------------------|------------------|
| WHO_AM_I | r | 00 | DA |
| TEMP_OUT_L | r | 01 | output |
| TEMP_OUT_H | r | 02 | output |
| OUT_X_L | r | 03 | output |
| OUT_X_H | r | 04 | output |
| OUT_Y_L | r | 05 | output |
| OUT_Y_H | r | 06 | output |
| DATA_STATUS_OIS | r | 0A | output |
| CTRL1_OIS | r/w | 0B | 00 |
| CTRL2_OIS | r/w | 0C | 00 |
| CTRL3_OIS | r/w | 0D | 00 |
| CTRL4_OIS | r/w | 0E | 00 |
| OFF_X | r/w | 0F | 00 |
| OFF_Y | r/w | 10 | 00 |
| Reserved | -- | 11 to 1E | -- |
| OIS_CFG_REG | r/w | 1F | 00 |

Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 8 bits, is used to identify them and to write the data through the serial interface.

8.1 WHO_AM_I (00h R)

Table 12. WHO_AM_I register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|

8.2 TEMP_OUT_L (01h R), TEMP_OUT_H (02h R)

Table 13. TEMP_OUT_L register

| | | | | | | | |
|-------|-------|-------|-------|---|---|---|---|
| Temp3 | Temp2 | Temp1 | Temp0 | 0 | 0 | 0 | 0 |
|-------|-------|-------|-------|---|---|---|---|

Table 14. TEMP_OUT_H register

| | | | | | | | |
|--------|--------|-------|-------|-------|-------|-------|-------|
| Temp11 | Temp10 | Temp9 | Temp8 | Temp7 | Temp6 | Temp5 | Temp4 |
|--------|--------|-------|-------|-------|-------|-------|-------|

Table 15. TEMP_OUT register description

| | |
|--------------|---|
| Temp11-Temp0 | Temperature data. Refer to Section 3.4 Temperature sensor on how to read the temperature sensor output data. |
|--------------|---|

8.3 OUT_X_L (03h R), OUT_X_H (04h R)

X-axis angular rate data. The value is expressed as two's complement.

8.4 OUT_Y_L (05h R), OUT_Y_H (06h R)

Y-axis angular rate data. The value is expressed as two's complement.

8.5 DATA_STATUS_OIS (0Ah R)

Table 16. DATA_STATUS_OIS register

| | | | | | | | |
|----------|---------|---------|---|----------|---------|---------|---|
| XYOR_OIS | XOR_OIS | YOR_OIS | 0 | XYDA_OIS | XDA_OIS | YDA_OIS | 0 |
|----------|---------|---------|---|----------|---------|---------|---|

Table 17. DATA_STATUS_OIS description

| | |
|----------|--|
| XYOR_OIS | OIS chain global data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set before the read) |
| XOR_OIS | OIS chain X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new X-axis data has overwritten a previous value before the read) |
| YOR_OIS | OIS Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new Y-axis data has overwritten a previous value before the read) |
| XYDA_OIS | OIS chain global new data available. Default value: 0 (0: a new set of data (X,Y axes) is not yet available; 1: a new set of data (X,Y axes) is available) |
| XDA_OIS | OIS chain X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available) |
| YDA_OIS | OIS chain Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available) |

8.6 CTRL1_OIS (0Bh R/W)

Table 18. CTRL1_OIS register

| | | | | | | | |
|------|-----------|-----|-----|-----|--------|-----|-----|
| BOOT | DR_PULSED | BLE | SIM | ODU | ORIENT | PW1 | PW0 |
|------|-----------|-----|-----|-----|--------|-----|-----|

Table 19. CTRL1_OIS register description

| | |
|-----------|---|
| BOOT | Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content) ⁽¹⁾ |
| DR_PULSED | DRDY signal pulsed. Default value: 0 (0: DRDY is latched; 1: DRDY is pulsed) |
| BLE | Big/Little Endian Data Selection. Default value: 0 (0: Data LSbyte @ lower address; 1: Data MSbyte @ lower address) |
| SIM | SPI Serial Interface Mode configuration. Default value: 0 (0: 4-wire interface; 1: 3-wire interface) |
| ODU | Output Data Update. Default value: 0 (0: output registers not updated until MSB and LSB have been read; 1: OIS output registers are updated continuously) |

| | |
|---------|--|
| ORIENT | Directional orientation selection. Default value: 0 (0: X-axis - Y-axis; 1: Y-axis - X-axis) |
| PW[1:0] | Power mode selection. Default: 00 Refer to Table 20. Operating mode selection . |

1. Boot request is executed as soon as internal oscillator is turned on. It is possible to set this bit while in power-down mode in which case it will be served at the next normal mode or sleep mode.

Table 20. Operating mode selection

| PW1 | PW0 | Operating mode selection |
|-----|-----|--------------------------|
| 0 | 0 | Power-down |
| 0 | 1 | Power-down |
| 1 | 0 | Sleep mode |
| 1 | 1 | Normal mode |

8.7 CTRL2_OIS (0Ch R/W)

Table 21. CTRL2_OIS register

| | | | | | | | |
|-------|-------|---------|---------|------------------|--------|--------|-----|
| SignX | SignY | LPF_BW1 | LPF_BW0 | 0 ⁽¹⁾ | HP_RST | SW_RST | HPF |
|-------|-------|---------|---------|------------------|--------|--------|-----|

1. This bit must be set to '0' for proper operation of the device.

Table 22. CTRL2_OIS register description

| | |
|-------------|--|
| SignX | X-axis angular rate sign selection. Default: 0 (0: sign not inverted; 1: sign inverted) |
| SignY | Y-axis angular rate sign selection. Default: 0 (0: sign not inverted; 1: sign inverted) |
| LPF_BW[1:0] | Low-pass filter bandwidth selection. Refer to Figure 6. Filtering chain block diagram and Table 23. Digital LPF configuration . |
| HP_RST | Reset high-pass filter. (0: disabled; 1: enabled) |
| SW_RST | Software reset. (0: disabled; 1: enabled) |
| HPF | Digital high-pass filter enable. Default: 0 (0: high-pass filter is disabled; 1: high-pass filter is enabled) |

Table 23. Digital LPF configuration

| LPF_BW2 | LPF_BW1 | LPF_BW0 | LPF BW [Hz] | Phase delay [°] |
|---------|---------|---------|-------------|-----------------|
| 0 | 0 | 0 | 290 | 7 @ 20 Hz |
| 0 | 0 | 1 | 210 | 9 @ 20 Hz |
| 0 | 1 | 0 | 160 | 11 @ 20 Hz |
| 0 | 1 | 1 | 450 | 5 @ 20 Hz |
| 1 | x | x | 1150 | 1 @ 10 Hz |

8.8 CTRL3_OIS (0Dh R/W)

Table 24. CTRL3_OIS register

| | | | | | | | |
|------------------|------------------|------------------|---------|-------|------------------|------------|---------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | ST_SIGN | ST_EN | 0 ⁽¹⁾ | H_L_ACTIVE | LPF_BW2 |
|------------------|------------------|------------------|---------|-------|------------------|------------|---------|

1. These bits must be set to '0' for proper operation of the device

Table 25. CTRL3_OIS register description

| | |
|------------|---|
| ST_SIGN | Self-test sign. Default value: 0 (0: not inverted sign; 1: inverted sign) |
| ST_EN | Self-test enable. Default value: 0 (0: ST disabled; 1: ST enabled) |
| H_L_ACTIVE | Data-ready signal active level. Default value: 0 (0: active high; 1: active low) |
| LPF_BW2 | Low-pass filter bandwidth selection. Refer to Figure 6. Filtering chain block diagram and Table 23. Digital LPF configuration . |

8.9 CTRL4_OIS (0Eh R/W)

Table 26. CTRL4_OIS register

| | | | | | | | |
|------------------|------------------|------------------|---------|------------------|-------------------|---------|------------------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | DRDY_EN | 0 ⁽¹⁾ | TEMP_DATA_ON_DRDY | DRDY_OD | 0 ⁽¹⁾ |
|------------------|------------------|------------------|---------|------------------|-------------------|---------|------------------|

1. These bits must be set to '0' for proper operation of the device.

Table 27. CTRL4_OIS register description

| | |
|-------------------|--|
| DRDY_EN | Data ready enable on DRDY pin. Default: 0 (1: DRDY on pin). Refer to Section 3.3 Data-ready interrupt and synchronous reading |
| TEMP_DATA_ON_DRDY | Temperature data-ready signal on DRDY pad. (0: disabled; 1: enabled) |
| DRDY_OD | DRDY pin configuration. Default value: 0 (0: push-pull; 1: open drain) |

8.10 OFF_X (0Fh R/W)

Table 28. OFF_X register

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| 0 ⁽¹⁾ | OFFX6 | OFFX5 | OFFX4 | OFFX3 | OFFX2 | OFFX1 | OFFX0 |
|------------------|-------|-------|-------|-------|-------|-------|-------|

1. This bit must be set to '0' for proper operation of the device

Table 29. OFF_X register description

| | |
|------------|---|
| OFFX [6:0] | User offset correction for X-axis. Default value: 000 0000 The value is expressed as two's complement. |
|------------|---|

The calibration step is -0.98 dps/LSB.

8.11 OFF_Y (10h R/W)

Table 30. OFF_Y register

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| 0 ⁽¹⁾ | OFFY6 | OFFY5 | OFFY4 | OFFY3 | OFFY2 | OFFY1 | OFFY0 |
|------------------|-------|-------|-------|-------|-------|-------|-------|

1. This bit must be set to '0' for proper operation of the device

Table 31. OFF_Y register description

| | |
|------------|---|
| OFFY [6:0] | User offset correction for Y-axis. Default 000 0000 The value is expressed at two's complement |
|------------|---|

Calibration step is 0.98 dps/LSB.

8.12 OIS_CFG_REG (1Fh R/W)

Table 32. OIS_CFG_REG register

| | | | | | | | |
|------------------|------------------|------------------|------------------|--------|------------------|-----------|-----------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | FS_SEL | 0 ⁽¹⁾ | HPF_BW[1] | HPF_BW[0] |
|------------------|------------------|------------------|------------------|--------|------------------|-----------|-----------|

1. These bits must be set to '0' for proper operation of the device

Table 33. OIS_CFG_REG register description

| | |
|-------------|--|
| FS_SEL | Full-scale selection. Default value: 0 (0: ±100 dps; 1: ±200 dps) |
| HPF_BW[1:0] | Digital HPF cutoff selection. Refer to Table 34. Digital HPF configuration |

Table 34. Digital HPF configuration

| HPF_BW[1:0] | HPF cutoff [Hz] |
|-------------|-----------------|
| 00 | 0.023 |
| 01 | 0.091 |
| 10 | 0.324 |
| 11 | 1.457 |

9 Package information

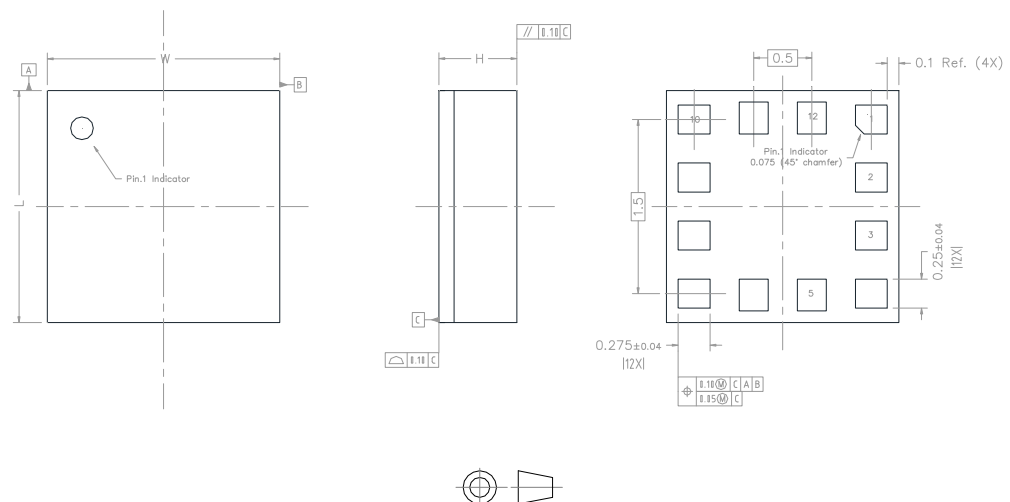
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020. Land pattern and soldering recommendations are available at www.st.com/mems.

9.2 LGA-12 package

Figure 11. LGA-12: package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.15mm unless otherwise specified

OUTER DIMENSIONS

| ITEM | DIMENSION [mm] | TOLERANCE [mm] |
|------------|----------------|----------------|
| Length [L] | 2 | ±0.1 |
| Width [W] | 2 | ±0.1 |
| Height [H] | 0.7 MAX | / |

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9.3 LGA-12 packing information

Figure 12. Carrier tape information for LGA-12 package

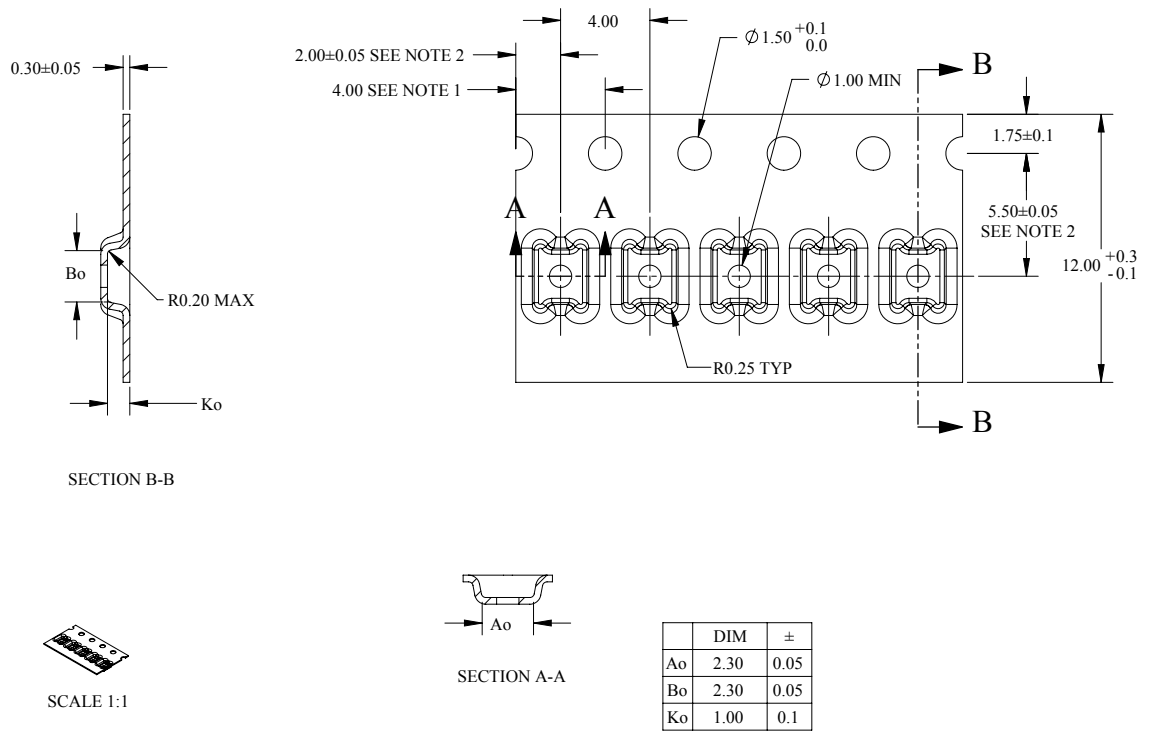


Figure 13. LGA-12 package orientation in carrier tape

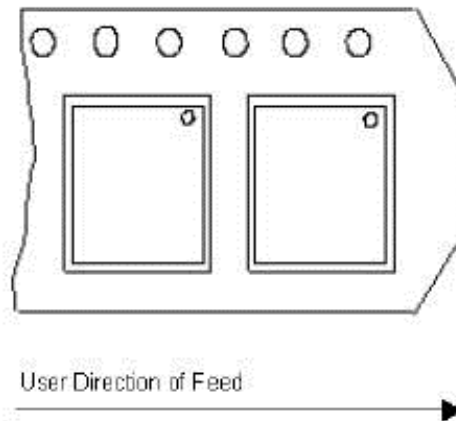


Figure 14. Reel information for carrier tape of LGA-12 package

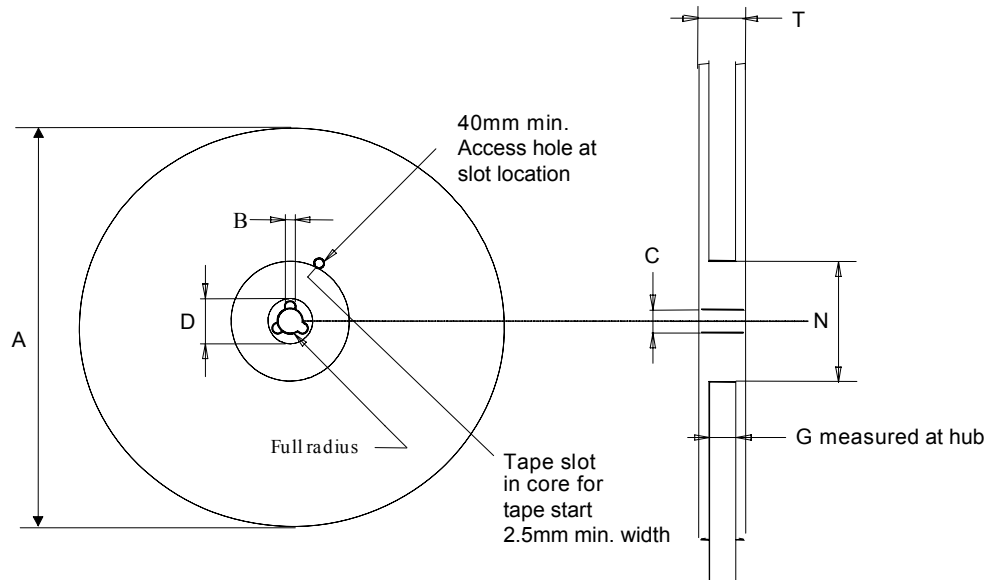


Table 35. Reel dimensions for carrier tape of LGA-12 package

| Reel dimensions (mm) | |
|----------------------|------------|
| A (max) | 330 |
| B (min) | 1.5 |
| C | 13 ±0.25 |
| D (min) | 20.2 |
| N (min) | 60 |
| G | 12.4 +2/-0 |
| T (max) | 18.4 |

Revision history

Table 36. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 27-Jun-2016 | 1 | Initial release |
| 03-Jul-2017 | 2 | Document status promoted to production data Updated Section 9: Package information |
| 01-Oct-2018 | 3 | Added product label indicating participation in ST's sustainable technology program |

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