General Description

The MAX98307/MAX98308 fully differential mono Class DG multilevel power amplifiers with integrated inverting charge pumps offer highly efficient, high-power audio solutions for portable applications.

Class DG multilevel modulation extends the dynamic range of the output signal by employing a charge-pump-generated negative rail as needed to extend the supply range. This scheme results in high efficiency over a wide output power range.

The ICs combine Maxim's active emissions limiting edge rate and overshoot control circuitry with multilevel output modulation to greatly reduce EMI. These features eliminate the need for output filtering as compared to traditional Class D devices, reducing component count and cost.

The MAX98307's 16-pin TQFN package features an adjustable gain set by external resistors. The MAX98308's space-saving 12-bump WLP package features an internally fixed gain of 8.5dB, 11.5dB, 14.5dB, 17.5dB, and 20.5dB set by a single gain input. Both devices operate over the extended -40°C to +85°C temperature range.

Applications

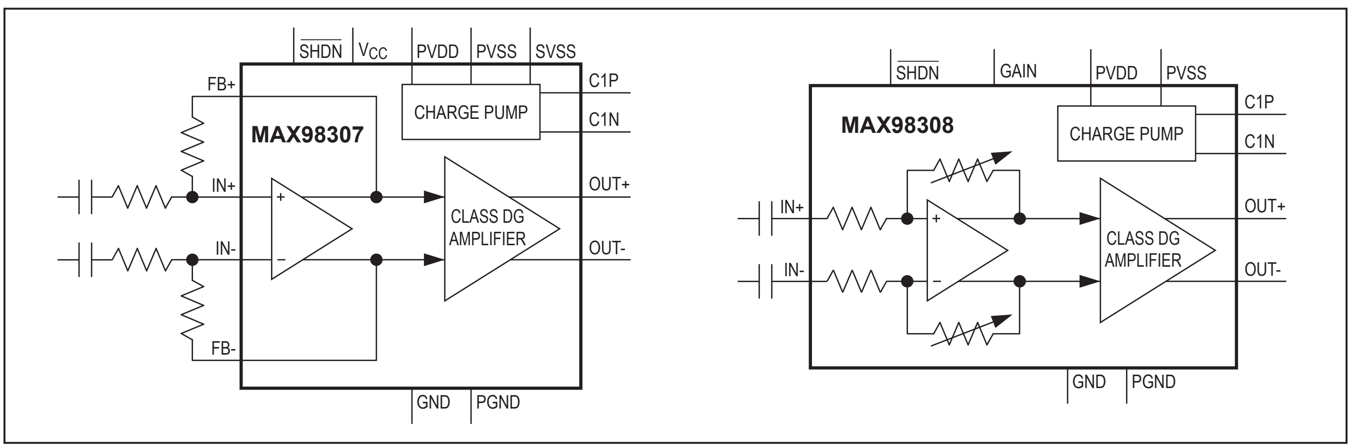
- Cellular Phones
- Smartphones
- Notebook Computers
- VoIP Phones
- Portable Audio
- Tablet PCs

Benefits and Features

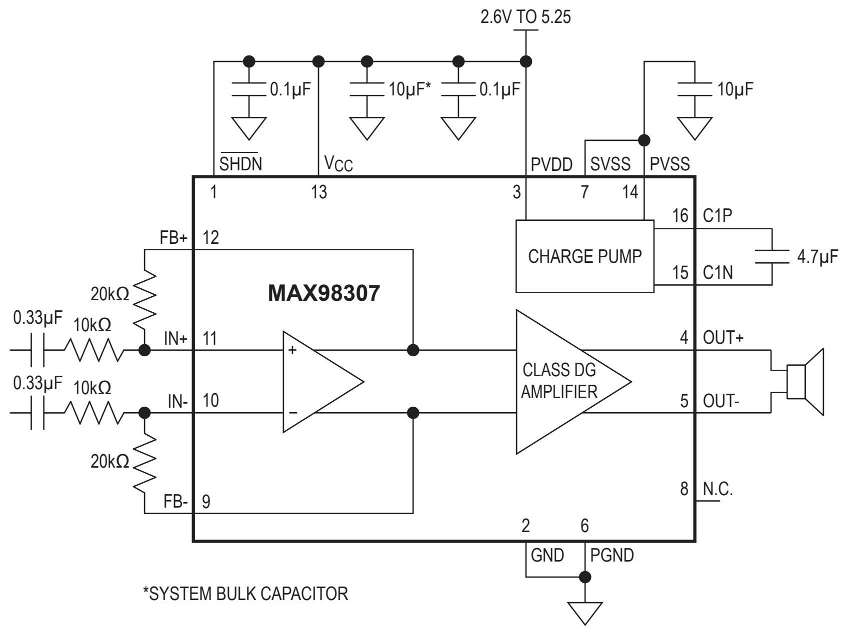
- High Efficiency Combined with High Output Power
  - Class DG Multilevel Modulation Ensures Maximum Efficiency Over Wide Output Power Range
- Improves Battery Life
  - Low 1.85mA Quiescent Current
- High Output Power at 1% THD+N
  - 1.54W at V_{PVDD} = 3.6V, 8Ω + 68µH Load
  - 2.85W at V_{PVDD} = 5V, 8Ω + 68µH Load
- High Output Power at 10% THD+N
  - 1.77W at V_{PVDD} = 3.6V, 8Ω + 68µH Load
  - 3.3W at V_{PVDD} = 5V, 8Ω + 68µH Load
- 84% Efficiency (V_{PVDD} = 3.6V, at 500mW Output)
- Active Emissions Limiting and Class DG Multilevel Output Modulation Eliminates EMI Output Filtering Requirement
- Integrated Charge Pump and High Efficiency Results in Small Solution Size
- Excellent RF Immunity
- Click-and-Pop Suppression
- Thermal and Overcurrent Protection
- Low-Current Shutdown Mode

***Ordering Information* appears at end of data sheet.**

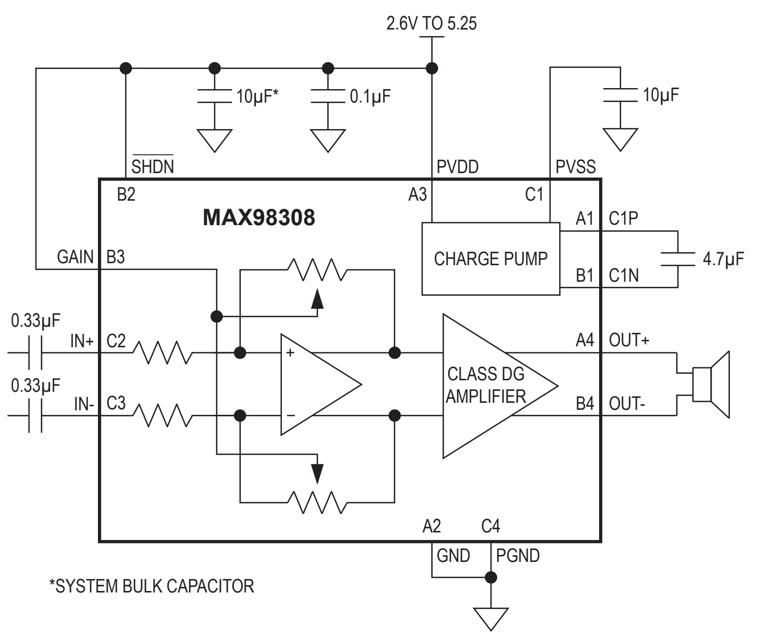
Simplified Block Diagrams



MAX98307 Typical Application Circuit



MAX98308 Typical Application Circuit



Absolute Maximum Ratings

PVDD to GND ....-0.3V to +6V
PGND to GND ....-0.3V to +0.3V
C1N to GND .... (V_{PVSS} - 0.3V) to +0.3V
IN+, IN- (MAX98307)............................... -0.3V to (V_{CC} + 0.3V)
V_{CC} to PVDD (MAX98307).................................-0.3V to +0.3V
PVSS to SVSS (MAX97307)...............................-0.3V to +0.3V
PVSS, SVSS to GND (MAX98307)........................-6V to +0.3V
IN+, IN- (MAX98308)..-0.3V to +6V
PVSS to GND (MAX98308) ....-6V to +0.3V
All Other Pins to GND ....-0.3V to (V_{PVDD} + 0.3V)
Continuous Current Into/Out of PVDD, V_{CC}, PGND, GND, OUT+, OUT-, C1P, C1N, PVSS, SVSS ....±800mA
Continuous Current (all other pins) ....±20mA
Duration of OUT+/OUT- Short Circuit to PGND or PVDD ....Continuous
Short-Circuit Duration Between OUT+ and OUT- Pins ....Continuous
Continuous Power Dissipation (T_A = +70°C) for Multilayer Board
TQFN (derate 20.8mW/°C above +70°C).................1667mW
WLP (derate 13.7mW/°C above +70°C)...................1100mW
Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) (TQFN-EP).............+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..............10°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....73°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..............30°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{PVDD} = V_{CC} = $V_{\overline{SHDN}}$ = 3.6V, V_{PGND} = V_{GND} = 0V, Z_L = 8Ω + 68μH between OUT+ and OUT-. [MAX98307 R_{IN+} = R_{IN-} = 10kΩ, R_{FB+} = R_{FB-} = 20kΩ] C_{IN+} = C_{IN-} = 0.33μF, A_V = 14.5dB, AC measurement bandwidth 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Range	V_{PVDD}, V_{CC}	Guaranteed by PSRR test		2.6		5.25	V
Quiescent Current	I_{DD}	V_{PVDD} = 3.6V			1.85	2.7	mA
Shutdown Current	I_{SHDN}	$\overline{SHDN}$ = GND			0.225	10	μA
Power-Supply Rejection Ratio (Note 4)	PSRR	V_{PVDD} = 2.6V to 5.25V			78		dB
		f = 217Hz, 200mV_{P-P} ripple			78		
		f = 10kHz, 200mV_{P-P} ripple			67		
Turn-On Time	t_{ON}	Time from shutdown or power-on to full operation	MAX98308		25	40	ms
			MAX98307, R_{IN} = 10kΩ		50	80	
Input DC Bias Voltage	V_{BIAS}				1.3		V
Input Resistance (MAX98308)	R_{IN}	A_V = 20.5dB (maximum gain)		15	22		kΩ
		A_V = 17.5dB			22		
		A_V = 14.5dB			22		
		A_V = 11.5dB			28		
		A_V = 8.5dB			40		

Electrical Characteristics (continued)

($V_{PVDD} = V_{CC} = V_{\overline{SHDN}}$ = 3.6V, $V_{PGND} = V_{GND}$ = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-. [MAX98307 $R_{IN+} = R_{IN-}$ = 10kΩ, $R_{FB+} = R_{FB-}$ = 20kΩ] $C_{IN+} = C_{IN-}$ = 0.33µF, A_V = 14.5dB, AC measurement bandwidth 20Hz to 20kHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Gain (MAX98308)	A_V	GAIN = short to GND		20	20.5	21	dB
		GAIN = 100kΩ pulldown to GND		17	17.5	18	
		GAIN = short to PVDD		14	14.5	15	
		GAIN = 100kΩ pullup to PVDD		11	11.5	12	
		GAIN = unconnected		8	8.5	9	
Common-Mode Rejection Ratio (MAX98308)	CMRR	f_{IN} = 1kHz			65		dB
Output Power (MAX98307)	P_{OUT}	f_{IN} = 1kHz, THD+N = 1%	Z_L = 8Ω + 68µH, V_{PVDD} = 3.6V		1.54		W
			Z_L = 8Ω + 68µH, V_{PVDD} = 4.2V		2		
			Z_L = 8Ω + 68µH, V_{PVDD} = 5.0V		2.85		
		f_{IN} = 1kHz, THD+N = 10%	Z_L = 8Ω + 68µH, V_{PVDD} = 3.6V		1.77		
			Z_L = 8Ω + 68µH, V_{PVDD} = 4.2V		2.3		
			Z_L = 8Ω + 68µH, V_{PVDD} = 5.0V		3.3		
Output Power (MAX98308)	P_{OUT}	THD+N ≤ 1%	Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 3.6V		1.4		W
			Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 4.2V		1.92		
			Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 5.0V		2.7		
		THD+N ≤ 10%	Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 3.6V		1.57		
			Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 4.2V		2.13		

Electrical Characteristics (continued)

(V_{PVDD} = V_{CC} = $V_{\overline{SHDN}}$ = 3.6V, V_{PGND} = V_{GND} = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-. [MAX98307 R_{IN+} = R_{IN-} = 10kΩ, R_{FB+} = R_{FB-} = 20kΩ] C_{IN+} = C_{IN-} = 0.33µF, A_V = 14.5dB, AC measurement bandwidth 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

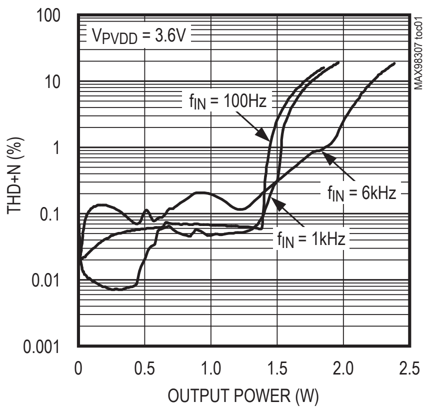
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, P_{OUT} = 1W			0.05		%
Output Offset Voltage	V_{OS}	T_A = +25°C			±1	±5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second (Notes 4, 5)	Into shutdown		-65		dBV
			Out of shutdown		-65		
Output Switching Frequency					340		kHz
Efficiency	η	f_{IN} = 1kHz, P_{OUT} at 500mW, THD+N = 0.02%			84		%
		f_{IN} = 1kHz, P_{OUT} at 1W, THD+N = 0.05%			82		
Current Limit	I_{LIM}				2		A_{RMS}
Output Noise	V_N	A-weighted			52		$µV_{RMS}$
LOGIC INPUT ($\overline{SHDN}$)							
Input Voltage High	V_{IH}			1.4			V
Input Voltage Low	V_{IL}					0.4	V
Input Leakage Current		T_A = +25°C				±10	µA

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Testing performed with a resistive load in series with an inductor to simulate an actual speaker. For R_L = 8Ω, L = 68µH.
Note 4: Amplifier inputs AC-coupled to GND.
Note 5: Specified at room temperature with an 8Ω resistive load in series with a 68µH inductive load connected across the BTL outputs. Mode transitions controlled by $\overline{SHDN}$ active-low shutdown control.

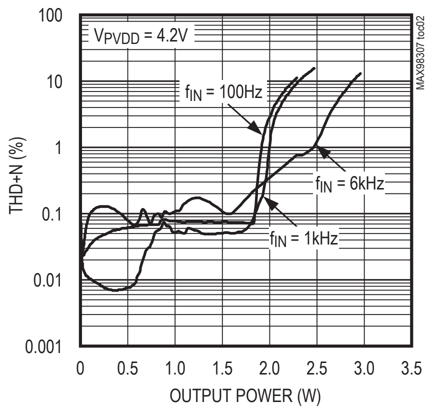
Typical Operating Characteristics

($V_{PVDD} = V_{CC} = V_{\overline{SHDN}}$ = 3.6V, $V_{PGND} = V_{GND}$ = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-, A_V = 14.5dB (MAX98307 $R_{IN+} = R_{IN-}$ = 10kΩ, $R_{FB+} = R_{FB-}$ = 20kΩ), $C_{IN+} = C_{IN-}$ = 0.33µF, AC measurement bandwidth 20Hz to 20kHz.)

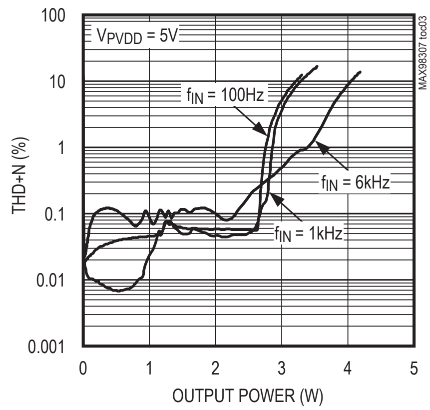
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (MAX98307)



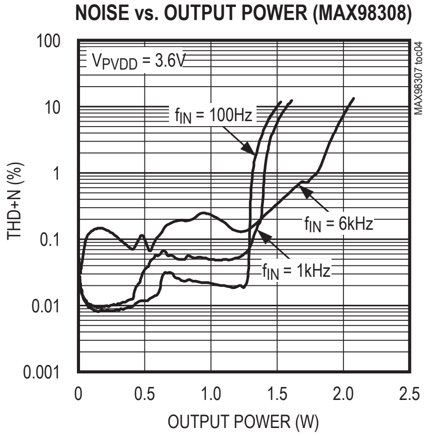
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (MAX98307)



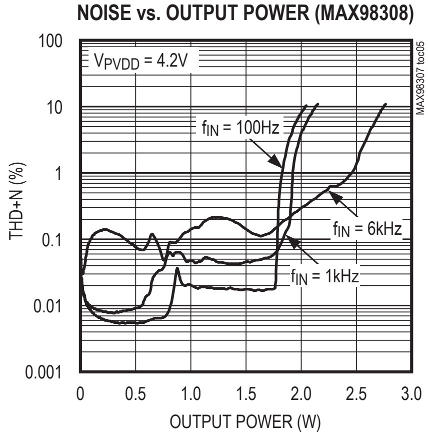
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (MAX98307)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (MAX98308)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (MAX98308)



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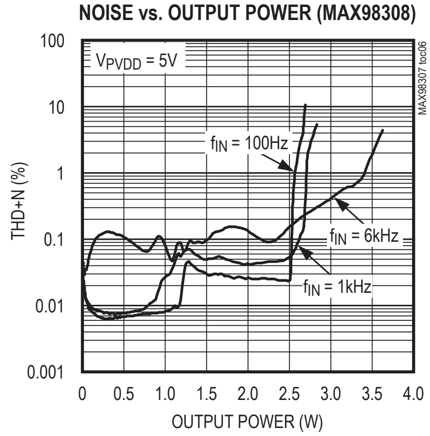
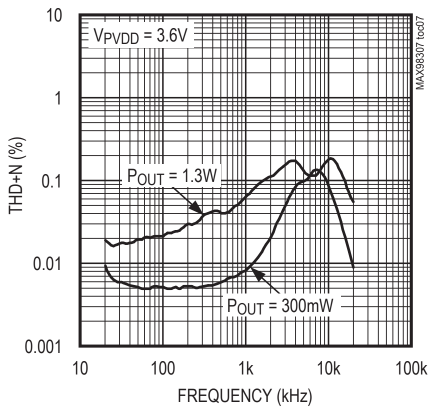


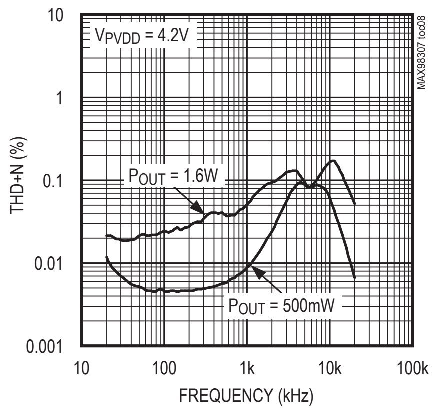
Typical Operating Characteristics (continued)

(V_{PVDD} = V_{CC} = $V_{\overline{SHDN}}$ = 3.6V, V_{PGND} = V_{GND} = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-, A_V = 14.5dB (MAX98307 R_{IN+} = R_{IN-} = 10kΩ, R_{FB+} = R_{FB-} = 20kΩ), C_{IN+} = C_{IN-} = 0.33µF, AC measurement bandwidth 20Hz to 20kHz.)

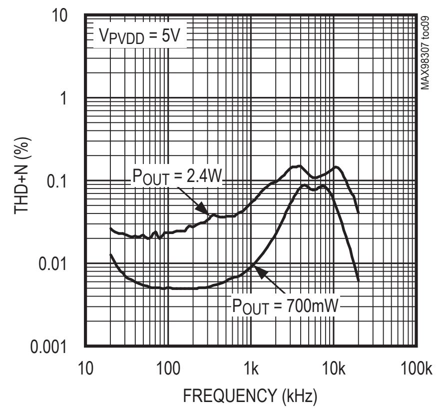
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MAX98307)



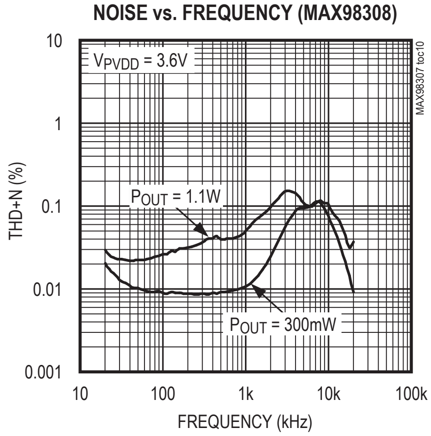
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MAX98307)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MAX98307)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MAX98308)



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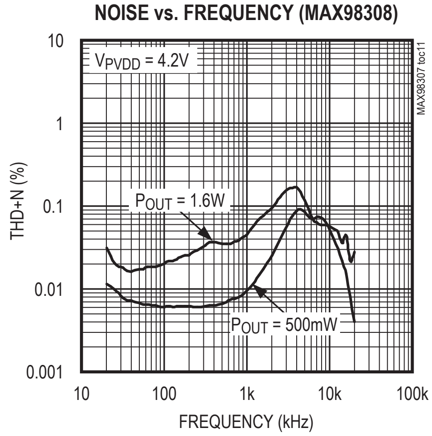

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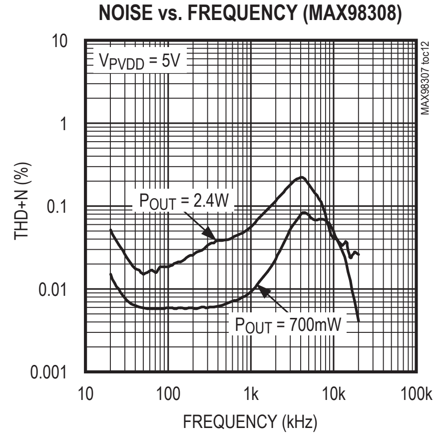
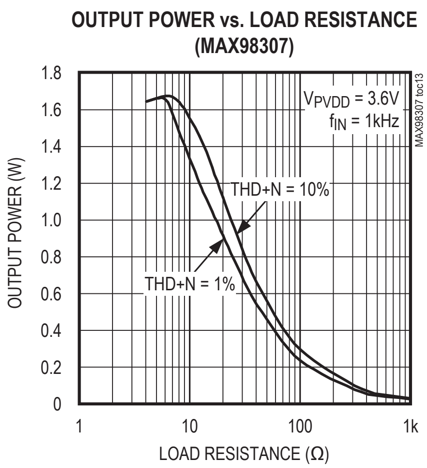
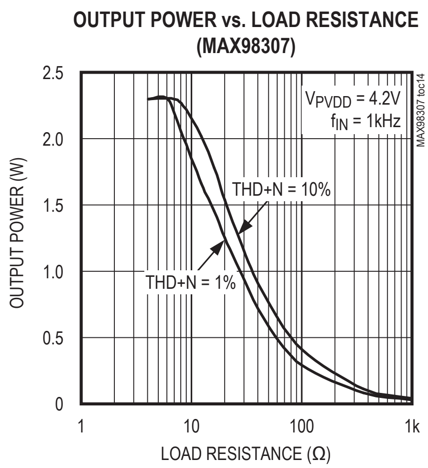
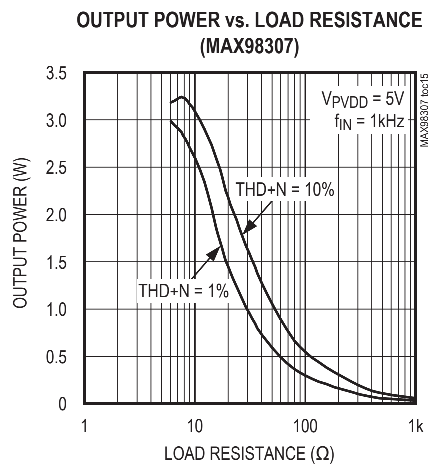


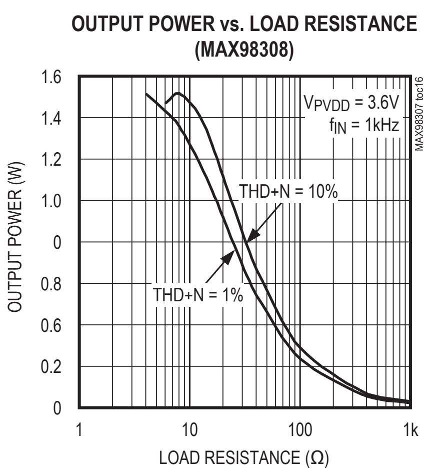
Typical Operating Characteristics (continued)

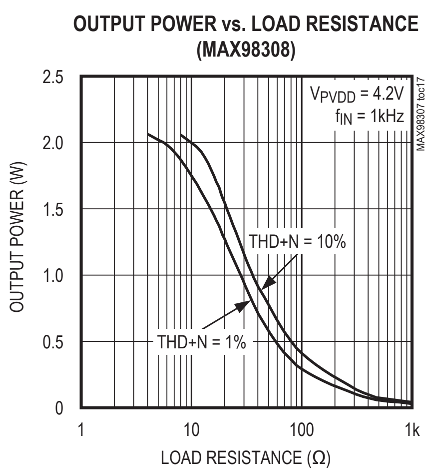
($V_{PVDD} = V_{CC} = V_{\overline{SHDN}}$ = 3.6V, $V_{PGND} = V_{GND}$ = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-, A_V = 14.5dB (MAX98307 $R_{IN+} = R_{IN-}$ = 10kΩ, $R_{FB+} = R_{FB-}$ = 20kΩ), $C_{IN+} = C_{IN-}$ = 0.33µF, AC measurement bandwidth 20Hz to 20kHz.)

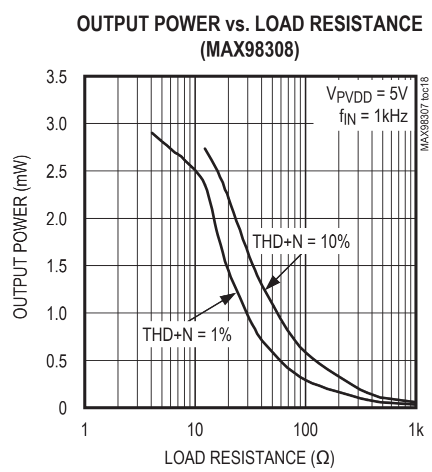






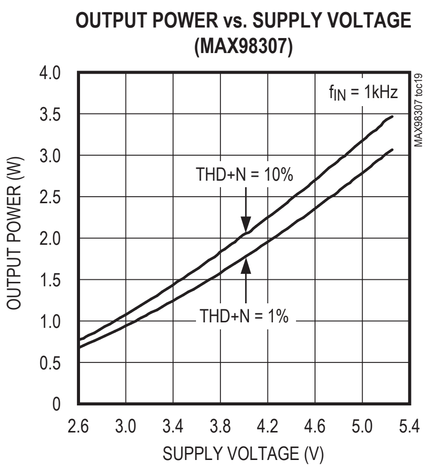


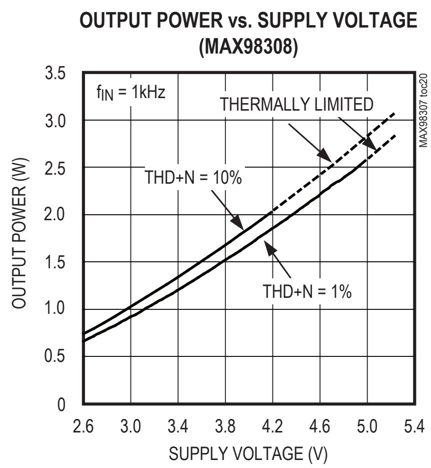


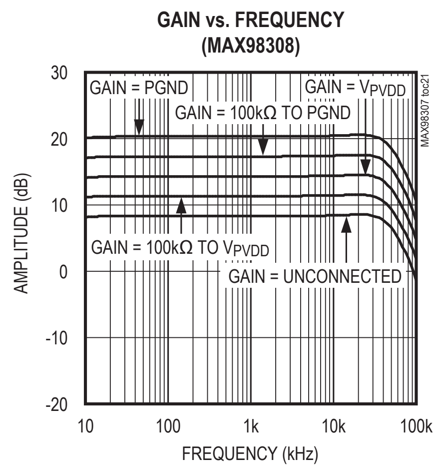


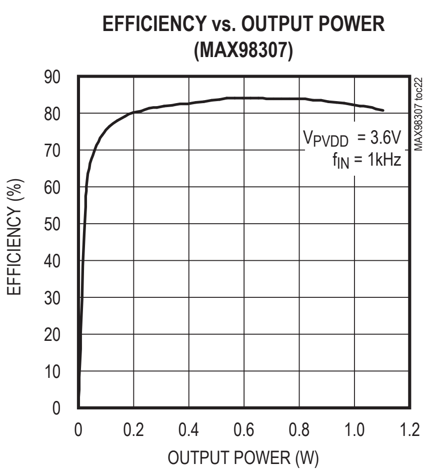
Typical Operating Characteristics (continued)

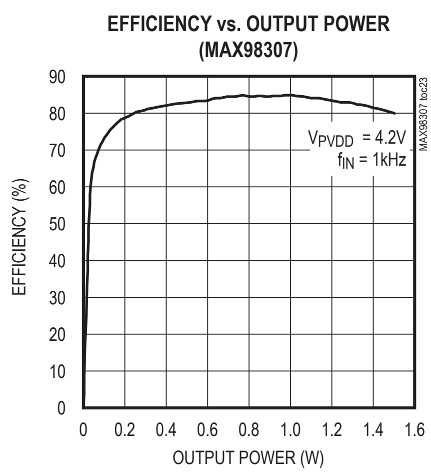
($V_{PVDD} = V_{CC} = V_{\overline{SHDN}}$ = 3.6V, $V_{PGND} = V_{GND}$ = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-, A_V = 14.5dB (MAX98307 $R_{IN+} = R_{IN-}$ = 10kΩ, $R_{FB+} = R_{FB-}$ = 20kΩ), $C_{IN+} = C_{IN-}$ = 0.33µF, AC measurement bandwidth 20Hz to 20kHz.)

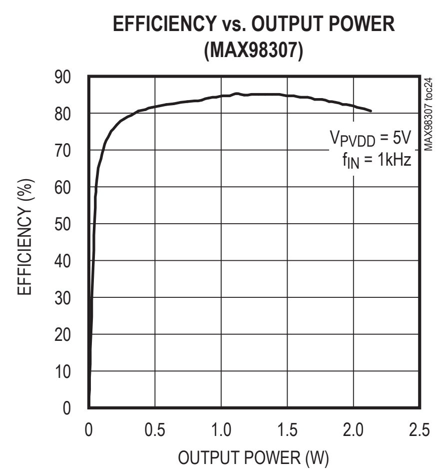








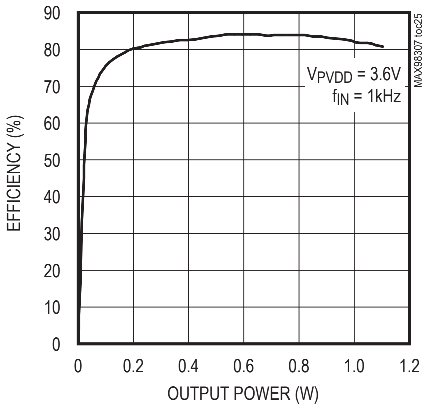




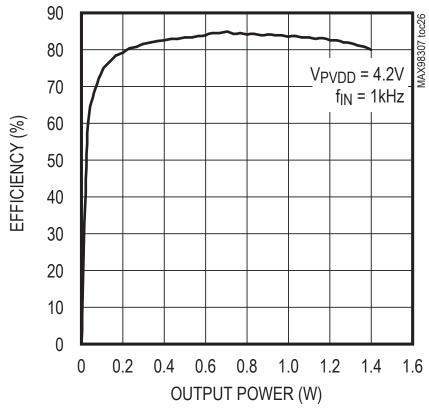
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{CC} = V_{\overline{SHDN}}$ = 3.6V, $V_{PGND} = V_{GND}$ = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-, A_V = 14.5dB (MAX98307 $R_{IN+} = R_{IN-}$ = 10kΩ, $R_{FB+} = R_{FB-}$ = 20kΩ), $C_{IN+} = C_{IN-}$ = 0.33µF, AC measurement bandwidth 20Hz to 20kHz.)

EFFICIENCY vs. OUTPUT POWER (MAX98308)



EFFICIENCY vs. OUTPUT POWER (MAX98308)



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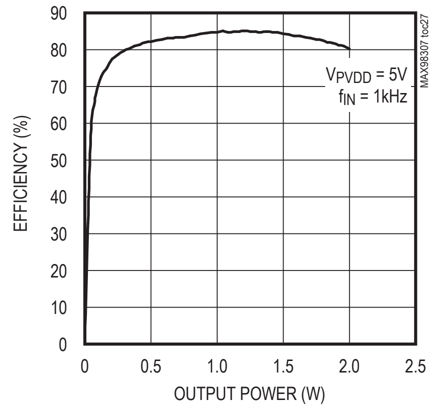
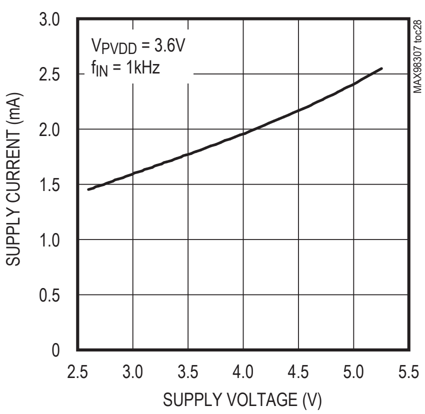
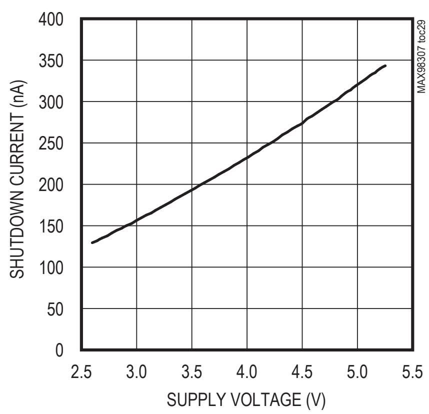


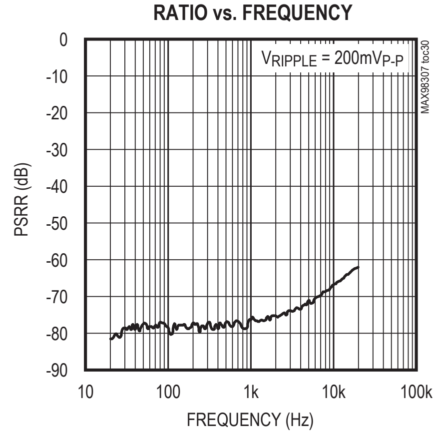
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



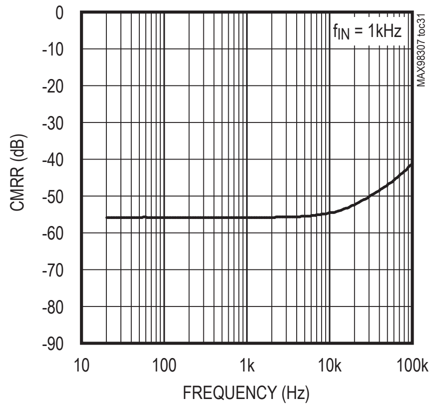
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



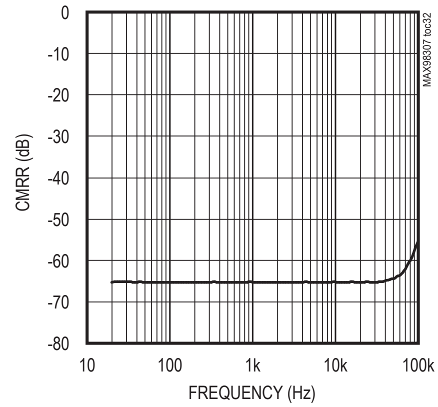
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{CC} = V_{\overline{SHDN}}$ = 3.6V, $V_{PGND} = V_{GND}$ = 0V, Z_L = 8Ω + 68µH between OUT+ and OUT-, A_V = 14.5dB (MAX98307 $R_{IN+} = R_{IN-}$ = 10kΩ, $R_{FB+} = R_{FB-}$ = 20kΩ), $C_{IN+} = C_{IN-}$ = 0.33µF, AC measurement bandwidth 20Hz to 20kHz.)

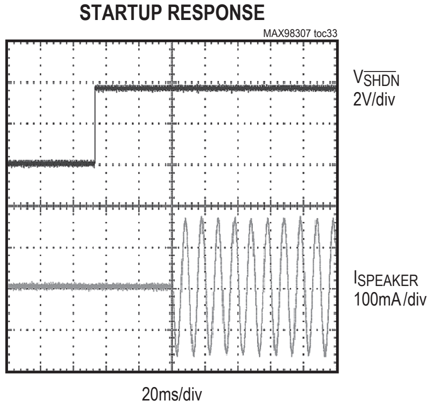
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MAX98307)



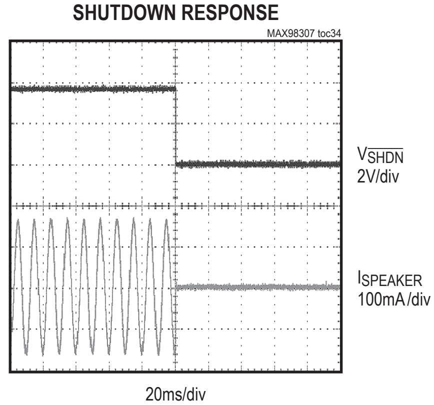
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MAX98308)



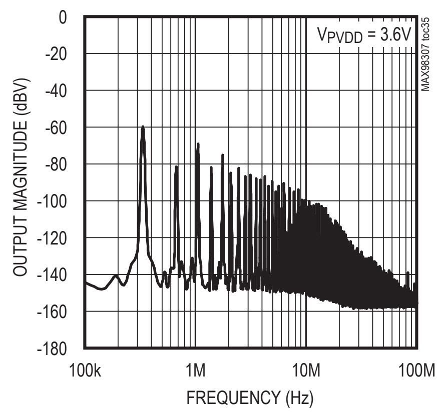
STARTUP RESPONSE



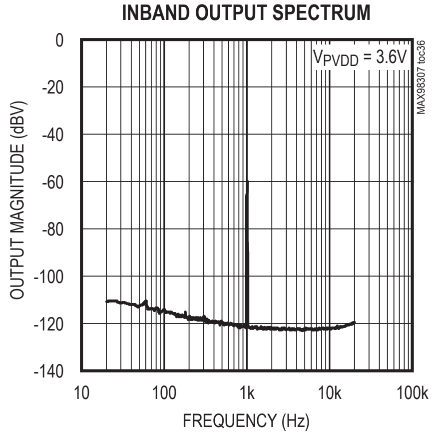
SHUTDOWN RESPONSE



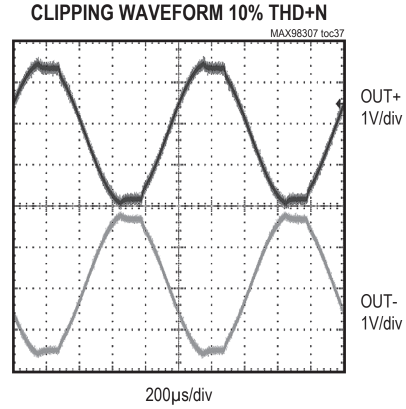
WIDEBAND vs. FREQUENCY



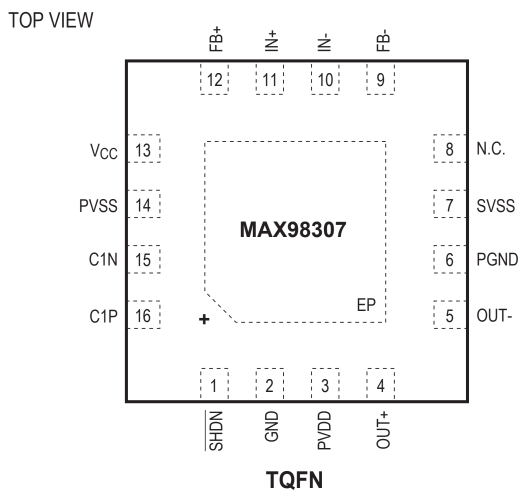
INBAND OUTPUT SPECTRUM

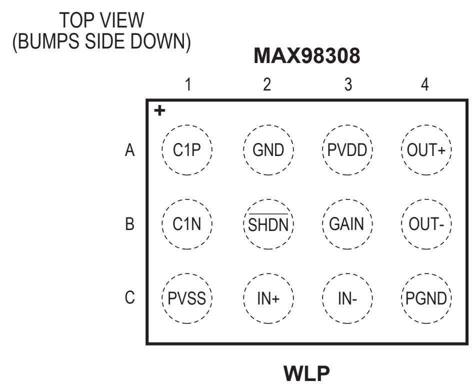


CLIPPING WAVEFORM 10% THD+N



Pin/Bump Configurations





Pin/Bump Description

PIN	BUMP	NAME	FUNCTION
MAX98307	MAX98308		
1	B2	$\overline{\text{SHDN}}$	Active-Low Shutdown. Connect to GND for shutdown. Connect to PVDD for normal operation.
2	A2	GND	Substrate and Signal Ground
3	A3	PVDD	Power and Charge-Pump Supply. Bypass to PGND with a 0.1µF capacitor.
4	A4	OUT+	Positive Amplifier Output
5	B4	OUT-	Negative Amplifier Output
6	C4	PGND	Power Ground
7	—	SVSS	Amplifier Negative Power Supply. Connect to PVSS (MAX98307).
8	—	N.C.	No Connection. Not internally connected. Connect to GND or leave unconnected.
9	—	FB-	Negative Amplifier Feedback
10	C3	IN-	Negative Amplifier Input
11	C2	IN+	Positive Amplifier Input
12	—	FB+	Positive Amplifier Feedback
—	B3	GAIN	See Table 1 MAX98308 Gain Configuration for more information.
13	—	V_{CC}	Signal Supply
14	C1	PVSS	Charge-Pump Output. Connect a 10µF capacitor between PVSS and PGND.
15	B1	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 4.7µF capacitor between C1N and C1P.
16	A1	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 4.7µF capacitor between C1N and C1P.
—	—	EP	Exposed Pad (TQFN Only). Internally connected to GND. Connect to a large ground plane with multiple vias to maximize thermal performance. Not intended as an electrical connection point.

Detailed Description

The MAX98307/MAX98308 fully differential mono Class DG multilevel power amplifiers with integrated inverting charge pumps offer highly efficient, high-power audio solutions for portable applications.

The new Class DG multilevel modulation scheme extends the dynamic range of the output signal by employing a charge-pump-generated negative rail, which is used as needed to extend the supply range. When the negative rail is not needed, the output is drawn entirely from the standard supply. This scheme results in high efficiency over a wide output power range.

The power amplifier incorporates active emissions limiting edge rate and overshoot control circuitry in combination with the multilevel output modulation scheme to greatly reduce EMI. These features eliminate the need for output filtering as compared to traditional Class D amplifiers, which reduces an application's component count.

The MAX98307 has an adjustable gain set by external resistors. The MAX98308 has preset fixed gains of 8.5dB, 11.5dB, 14.5dB, 17.5dB, and 20.5dB set by a gain select input (GAIN).

Class DG Multilevel Operation

The ICs' filterless Class DG multilevel amplifiers feature a proprietary Maxim output stage that offers higher efficiency over a greater output power range than previous amplifiers. The amplifier combines Class D switching output efficiency and Class G supply level shifting with a multilevel output modulation scheme that with a 5V supply has efficiency better than 80% efficiency over the 0.35W to 2.2W output range.

The Class DG multilevel output stage uses pulse-width modulation (PWM), a rail-to-rail digital output signal with variable duty cycle, to approximate an analog input signal as in a Class D amplifier. Rail-to-rail operation ensures that any dissipation at the output is due solely to the $R_{DS(ON)}$ of the power output MOSFETs. The Class DG multilevel output stage also senses the magnitude of the output signal and switches the supply rails as needed to more efficiently supply the required signal power. For a low output signal swing requirement (below the battery supply rail V_{PVDD}), the output range is between V_{PVDD} and ground. When output swing above V_{PVDD} is required, V_{PVSS}, an internal inverting charge-pump-generated negative rail replaces ground as the lower supply. The high output swing range is then V_{PVDD} to V_{PVSS}, approximately double the low swing range. This approach efficiently manages power consumption by switching the operating rails as needed according to the output swing requirements. Additionally, multilevel output modulation is employed in to draw the maximum possible power from the lower impedance battery supply rail, V_{PVDD}, rather than the higher impedance charge-pump-generated rail V_{PVSS}. This is accomplished by generating PWM signals that swing from ground to V_{PVDD} or from ground to V_{PVSS} at either end of the bridge tied load (BTL) rather than continually swinging from V_{PVDD} to V_{PVSS}. The signals are modulated in such a way that V_{PVSS} is used only as necessary to generate low-end signal swing.

These combined operations ensure that power dissipation due to $R_{DS(ON)}$ loss and charge-pump impedance is minimized, and that efficiency and output power is maximized across the audio range. Class DG multilevel operation is shown as Figure 1.

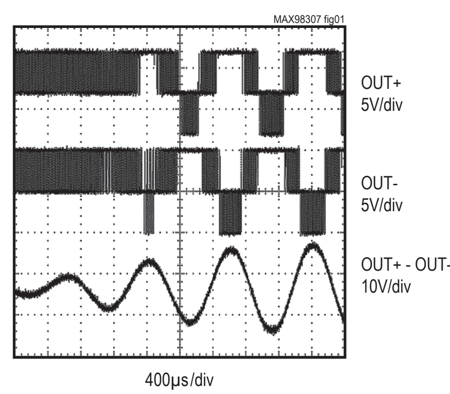


Figure 1. Class DG Multilevel Operation

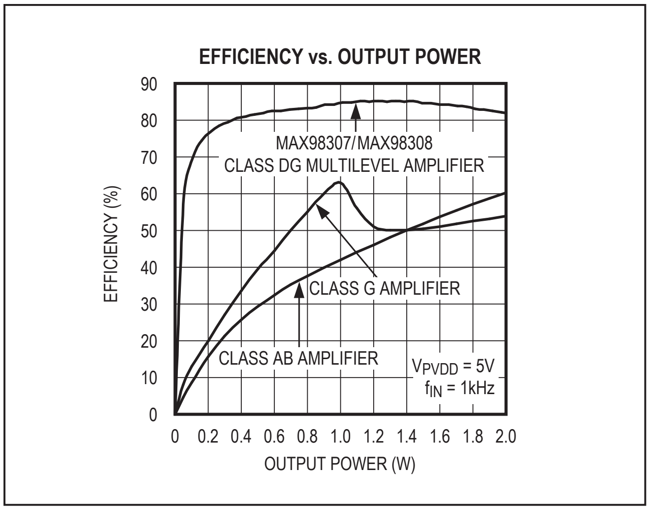


Figure 2. Class DG Multilevel vs. Typical Class G and Class AB Amplifier Efficiency

The Class DG multilevel efficiency compares favorably with Class AB and Class G amplifiers as shown in Figure 2. Note that efficiency at 1W is 85%.

EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet electromagnetic-interference (EMI) regulation standards. The active emissions limiting edge-rate control circuitry and Class DG multilevel modulation scheme reduce EMI emissions without the need for external filtering components, while maintaining high efficiency (see Figure 3).

Amplifier Current Limit

If the output current of the speaker amplifier exceeds the current limit, the ICs disable the outputs for approximately 100µs. After 100µs, the outputs are reenabled. If the fault condition still exists, the ICs continue to disable and reenable the outputs until the fault condition is removed.

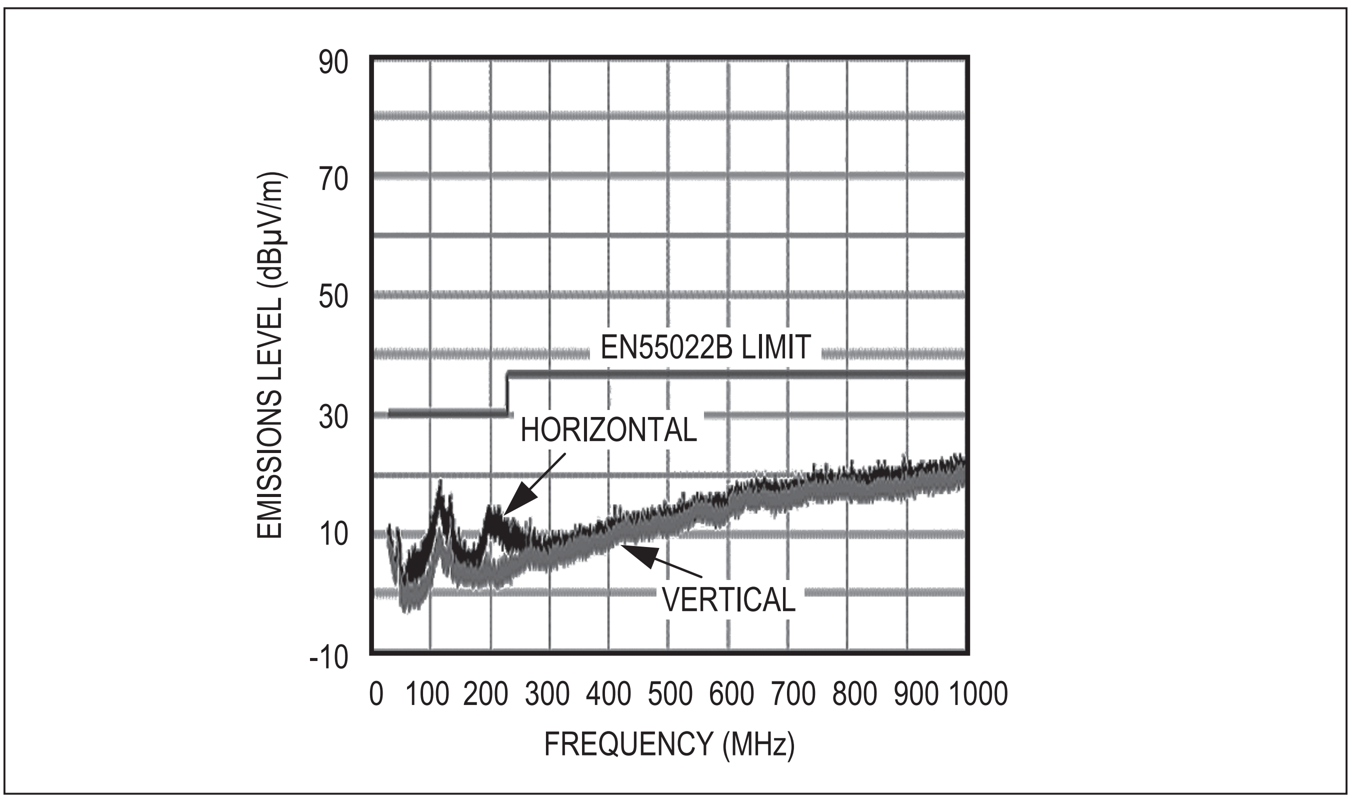


Figure 3. EMI Performance with V_{PVDD} = 5V, 12in of Speaker Cable, No Output Filter

Click-and-Pop Suppression

The speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs quickly and simultaneously ramp down to PGND.

Thermal and Short Circuit Protection

The ICs automatically enter thermal shutdown when the die temperature is greater than +160°C and reactivate at less than +135°C. Additionally, if the outputs are shorted to each other or either rail, the amplifier prevents catastrophic loss by disabling the outputs.

Shutdown

The ICs feature a low-power shutdown mode, drawing less than 0.225µA (typ) supply current. Drive $\overline{SHDN}$ low to put the IC into the shutdown state.

Applications Information

Filterless Class DG Operation

Traditional Class DG amplifiers require an output filter. The filter adds cost and size, as well as decreases efficiency and THD+N performance. The ICs' active emissions limiting and Class DG multilevel output modulation allow for filterless operation while reducing external component count, and thereby, cost.

Because the switching frequency of the ICs is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Differential Input Amplifier

The ICs feature a differential input configuration, making the device compatible with many codecs and offering improved noise immunity as compared to single-ended input amplifiers. In devices such as mobile phones, noisy digital signals can be picked up by an amplifier's input traces. A differential amplifier amplifies the difference of the two inputs, while signals common to both inputs, such as switching noise, are rejected. While both ICs feature differential amplifiers, their voltage gain is set in differing manners.

The MAX98307 employs external feedback resistors as shown in Figure 4. Voltage gain of the input amplifier is set as:

$$A_V = 20\log\left(\frac{R_{FB}}{R_{IN}}\right)(dB) + 8.5\,dB$$

where A_V is the desired voltage gain in decibels. R_{IN+} should be equal to R_{IN-}, and R_{FB+} should be equal to R_{FB-}.

In differential input configurations, the common-mode rejection ratio (CMRR) is primarily limited by the external resistor and capacitor matching. Ideally, to achieve the highest possible CMRR, the following external components should be selected where:

$$\frac{R_{FB+}}{R_{IN+}} = \frac{R_{FB-}}{R_{IN-}}$$

and

$$C_{IN+} = C_{IN-}$$

The gain of the MAX98308 is selectable by connecting the gain-select bump GAIN as described in Table 1.

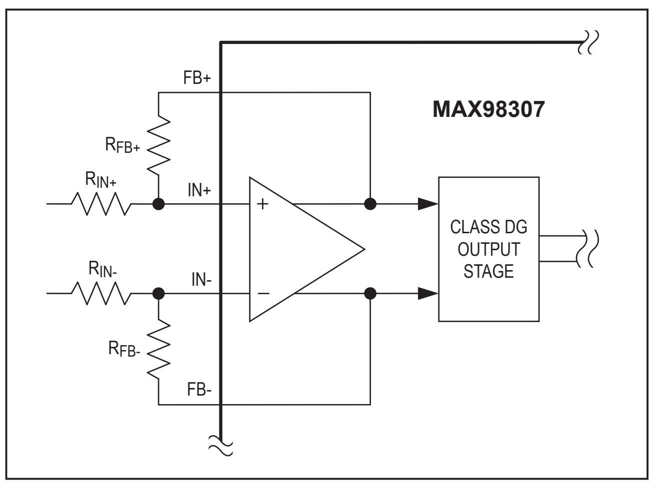


Figure 4. Setting the Voltage Gain of the MAX98307

Table 1. MAX98308 Gain Configuration

GAIN	PREAMPLIFIER GAIN (dB)	OVERALL GAIN (dB)
Unconnected	0	8.5
100kΩ to V_{PVDD}	3	11.5
Short to V_{PVDD}	6	14.5
100kΩ to PGND	9	17.5
Short to PGND	12	20.5

***Note:** For both ICs, the Class DG output stage has a fixed gain of 8.5dB. Any gain or attenuation set by the external input stage resistors adds to or subtracts from this fixed gain.*

Component Selection

Power-Supply Input (PVDD)

PVDD powers the speaker amplifier and has a range of 2.6V to 5.25V. Bypass PVDD with 0.1μF and 10μF capacitors in parallel to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the supply are used.

Input Coupling Capacitors

The AC-coupling capacitors (C_{IN}) and input resistors (R_{IN}) form highpass filters that remove any DC bias from an input signal. See the *MAX98307 Typical Application Circuit* and *MAX98308 Typical Application Circuit*. C_{IN} prevents any DC components from the input signal source appearing at the amplifier outputs. The -3dB point of the highpass filter, assuming zero source impedance due to the input signal source, is given by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors with adequately low voltage coefficient (X5R or X7R recommended) for best low frequency THD+N performance.

Charge-Pump Capacitor Selection

Use capacitors with an equivalent series resistance (ESR) less than 50mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric and a rated voltage of at least 6.3V.

Charge-Pump Flying Capacitor

The value of the charge-pump flying capacitor affects the load regulation and output resistance of the charge pump. A charge-pump flying capacitor value that is too small (less than 1μF) degrades the amplifier's ability to provide sufficient current drive. Increasing the value of this flying capacitor and decreasing the ESR improves load regulation and reduces the charge-pump output impedance, which improves the output power and efficiency of the amplifier. A 4.7μF or greater value, low-ESR capacitor is recommended.

Charge-Pump Hold Capacitor

The charge-pump hold capacitor value and ESR directly affect the ripple at the charge-pump rail, PVSS. Increasing the charge-pump hold capacitor value reduces output ripple. Likewise, decreasing the ESR of this capacitor reduces both ripple and output resistance. A 10μF or greater value, low-ESR capacitor is recommended.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device increases. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the device output to an 8Ω load through 100mΩ of total speaker trace, 1.97W is delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.998W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

The ICs are inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

Thermal Considerations

Class DG multilevel amplifiers provide much better efficiency and thermal performance than a comparable Class AB or Class G amplifier. However, the system's thermal performance must be considered with realistic expectations and include consideration of many parameters. This section examines Class DG multilevel amplifiers using general examples to illustrate good design practices.

MAX98307 (TQFN) Applications Information

The exposed pad is the primary route of keeping heat away from the IC. With a bottom-side exposed pad, the PCB and its copper becomes the primary heatsink for the Class DG multilevel amplifier. Solder the exposed pad to a large copper polygon. Add as much copper as possible from this polygon to any adjacent pin on the amplifier as well as to any adjacent components, provided these connections are at the same potential. These copper paths must be as wide as possible. Each of these paths contributes to the overall thermal capabilities of the system.

The copper polygon to which the exposed pad is attached should have multiple vias to the opposite side of the PCB. Make this polygon as large as possible within the system's constraints for signal routing.

MAX98308 (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*.

Ordering Information

PART	GAIN SET	PIN-PACKAGE
MAX98307ETE+	External	16 TQFN-EP*
MAX98307ETE/V+	External	16 TQFN-EP*
MAX98308EWC+	Internal	12 WLP

Note: *All devices operate over the -40°C to +85°C temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+5	21-0136	90-0032
12 WLP	W121A1+1	21-0542	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	8/11	Updated output power conditions in the *Electrical Characteristics* table	4
2	9/11	Updated *Electrical Characteristics* table and TOC 20	2, 4, 8
3	9/11	Added EP to the *Pin Description* section and removed future product reference for the MAX98308	12, 17
4	3/12	Added R_{IN} typical values for all gains and corrected error on TOCs 1–6	3, 6
5	3/15	Added MAX98307ETE/V+ to *Ordering Information*	17
6	6/16	Updated package code and outline number in *Package Information* table	18
7	4/20	Updated TOC35 in *Typical Operating Characteristics* section	11

