TPS799xxEVM-105

This User's Guide describes the characteristics, operation, and use of the TPS799xxEVM-105 Evaluation Module (EVM). This EVM demonstrates three individual configurations of the Texas Instruments TPS799xx low quiescent current, ultra-low noise, high PSRR, low dropout linear regulator capable of supplying up to 200 mA of output current. This User's Guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

The Texas Instruments TPS799xxEVM-105 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS799xx family of linear regulators. These regulators are low quiescent current, high PSRR, ultra-low noise, low dropout linear regulators.

The EVM contains three independent linear regulator DC/DC converters. The default output voltages of the converters are listed in Table 1.

Table 1. Device and Output Voltage Configurations

Converter	IC	Package	Output Voltage	Type
1	TPS79901DDC	TO/SOT	1.60	Adjustable
2	TPS79918YZU	CSP-5 chipscale	2.80	Fixed
3	TPS79901YZU	CSP-5 chipscale	3.30	Adjustable

If desired, converters 1 and 3 on this EVM can be easily modified to supply higher or lower output voltages. The converter can be adjusted to provide an output voltage between 1.217 V and 6.34 V. Output voltages other than the default values may be evaluated by adjusting the appropriate feedback resistors. Also, other fixed output voltage versions of the devices can be easily evaluated using this EVM. Refer to the TPS799xx data sheet (SBVS056A) for the various fixed output voltage options available in the TPS799xx device family as well as for more information on adjusting the output voltage.

2 Setup

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS799xxEVM-105.

2.1 Input / Output Connector Descriptions

J1, TP1 and TP3 – VIN — This is the positive input connection to the corresponding converter. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission.

J2, TP2 and TP4 – GND — This is the input return connection for the input power supply for the corresponding converter

J3, TP5 and TP7 – VOUT — This is the positive connection from the output of the corresponding converter. Connect this pin to the positive input of the load.

J6, TP6 and TP8 – GND — This is the return connection from the output of the corresponding converter. Connect this pin to the negative input of the load.

JP1, JP2 and JP3 – EN — This jumper enables or disables the corresponding converter. Connect the shorting jumper from the center EN pin to either the ON or OFF position. This pin should never be left floating.

2.2 Setup

There are two different package styles on the TPS799xxEVM-105. The thermal performance of each package style and ambient temperature may limit the input voltage or output current of the converters. Since the converter outputs are set, the power dissipated in the package relates only to the input voltage and output current. Table 2 shows the maximum input voltage at full load current of 200 mA. Above this voltage, the output current must be reduced to keep the power dissipation of the package below the maximums stated in the datasheet. Output voltage or ambient temperature changes affect these values. Table 2 also shows the minimum input voltage required to produce an output for each converter. The minimum input voltage is the output voltage plus the necessary dropout voltage.

Table 2. Minimum and Maximum Input Voltage

Converter	Output Voltage	Minimum Input Voltage	Max Input Voltage Before Current Derate (T_A = 25°C, I_O = 200 mA)
1	1.6	1.775	3.4
2	2.8	2.975	4.7
3	3.3	3.46	5.1

For converters number 1 and 3, the user can replace the factory supplied TPS79901 with other fixed voltage converters in the TPS799xx family. R1 and C5 should be removed and left open and a noise reduction capacitor installed in place of R2 when using a fixed voltage IC in converter 1. R3 and C7 should be removed and left open and a noise reduction capacitor installed in place of R4 for converter 3 when using a fixed voltage IC.

2.3 Operation

JP1, JP2, and JP3 are the enables for the converters and must be configured for proper operation of the converter. Use a shorting block to set JP1, JP2, and JP3 to the desired configurations.

3 Board Layout

This chapter provides the TPS799xxEVM-105 board layout and illustrations.

3.1 Layout

Figure 1, Figure 2, and Figure 3 show the board layout for the TPS799xxEVM-105 PWB.

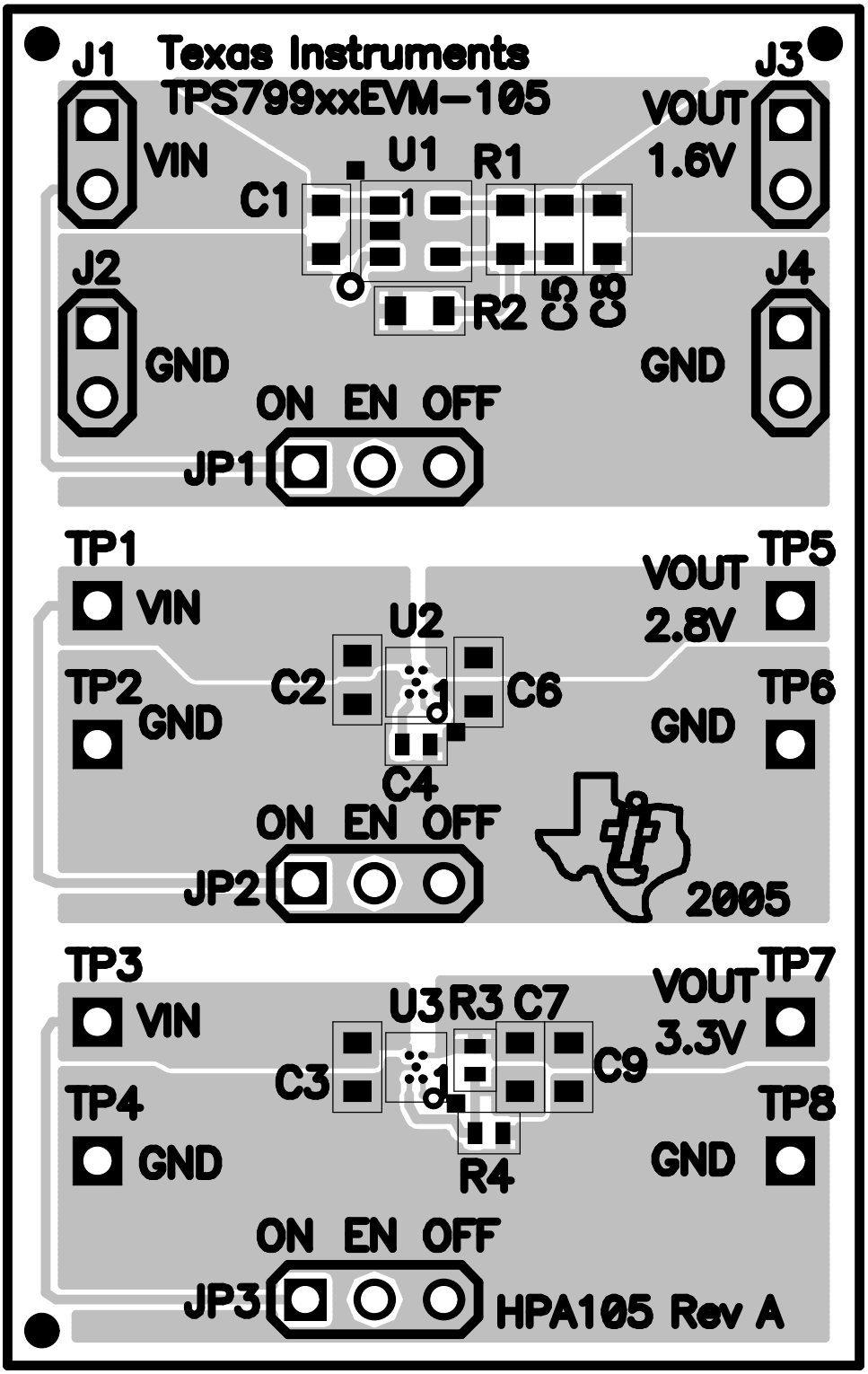

Figure 1. Assembly Layer

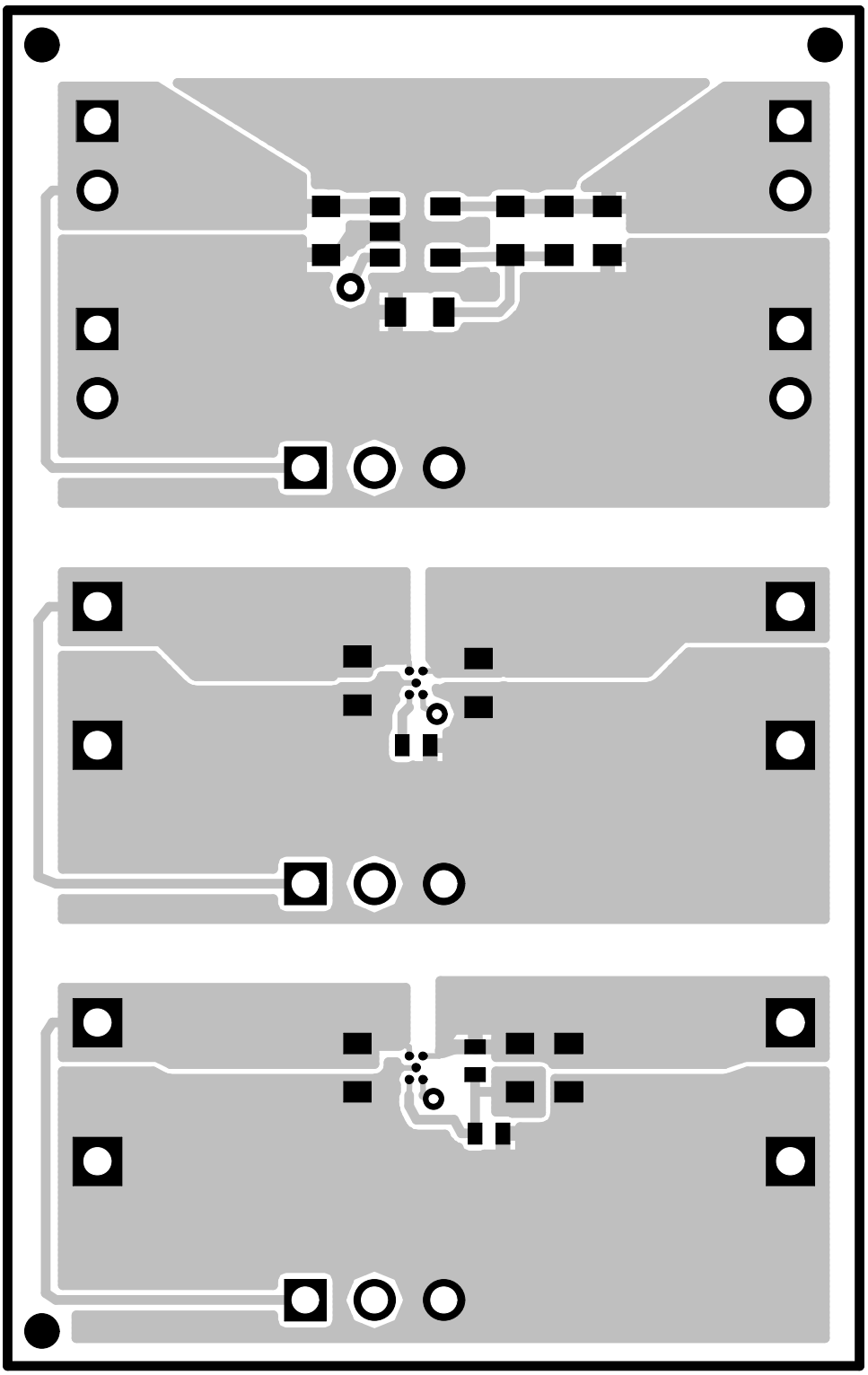

Figure 2. Top Layer Routing

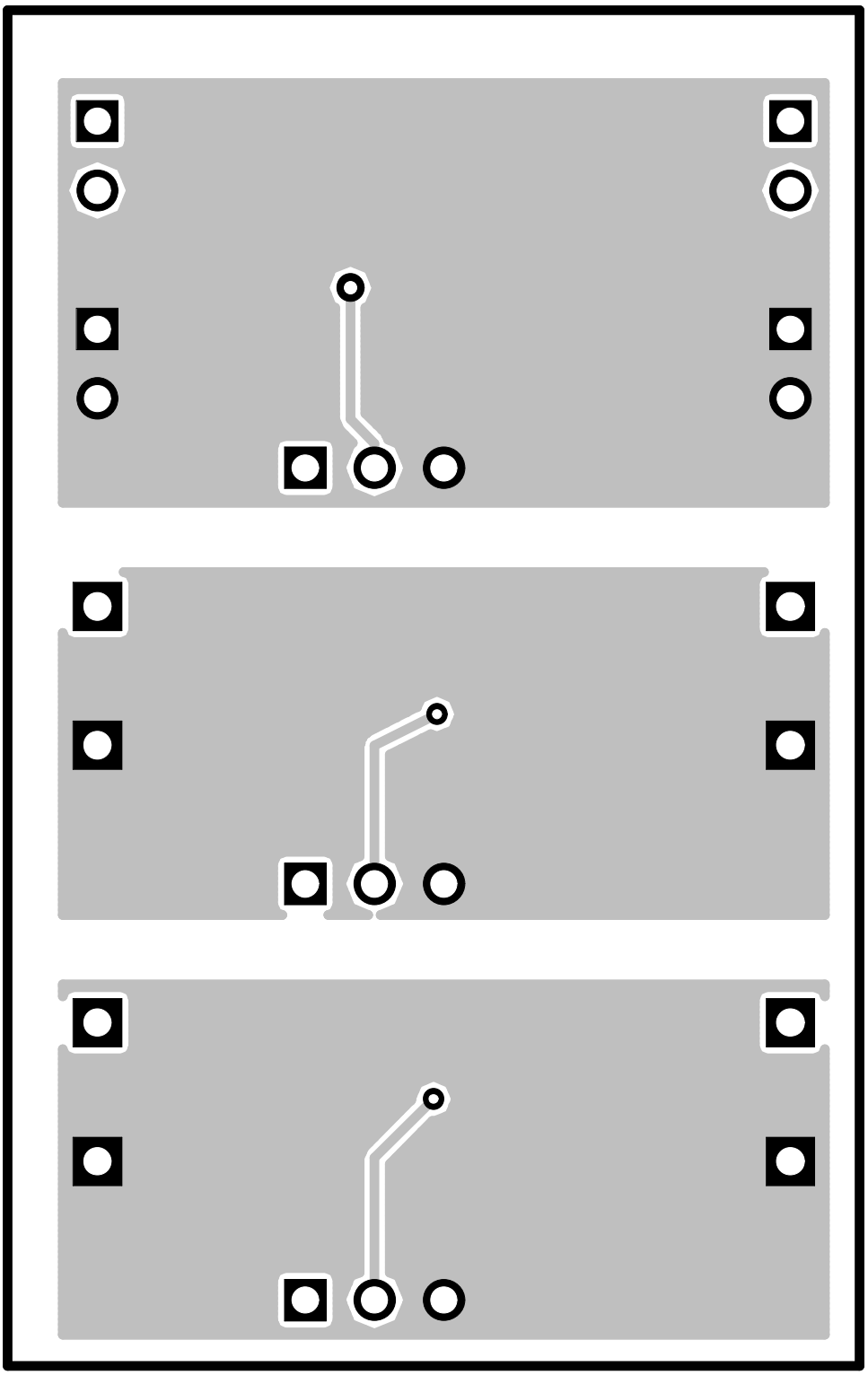

Figure 3. Bottom Layer Routing

4 Schematic and Bill of Materials

This chapter provides the TPS799xxEVM-105 schematic and bill of materials.

4.1 Schematic

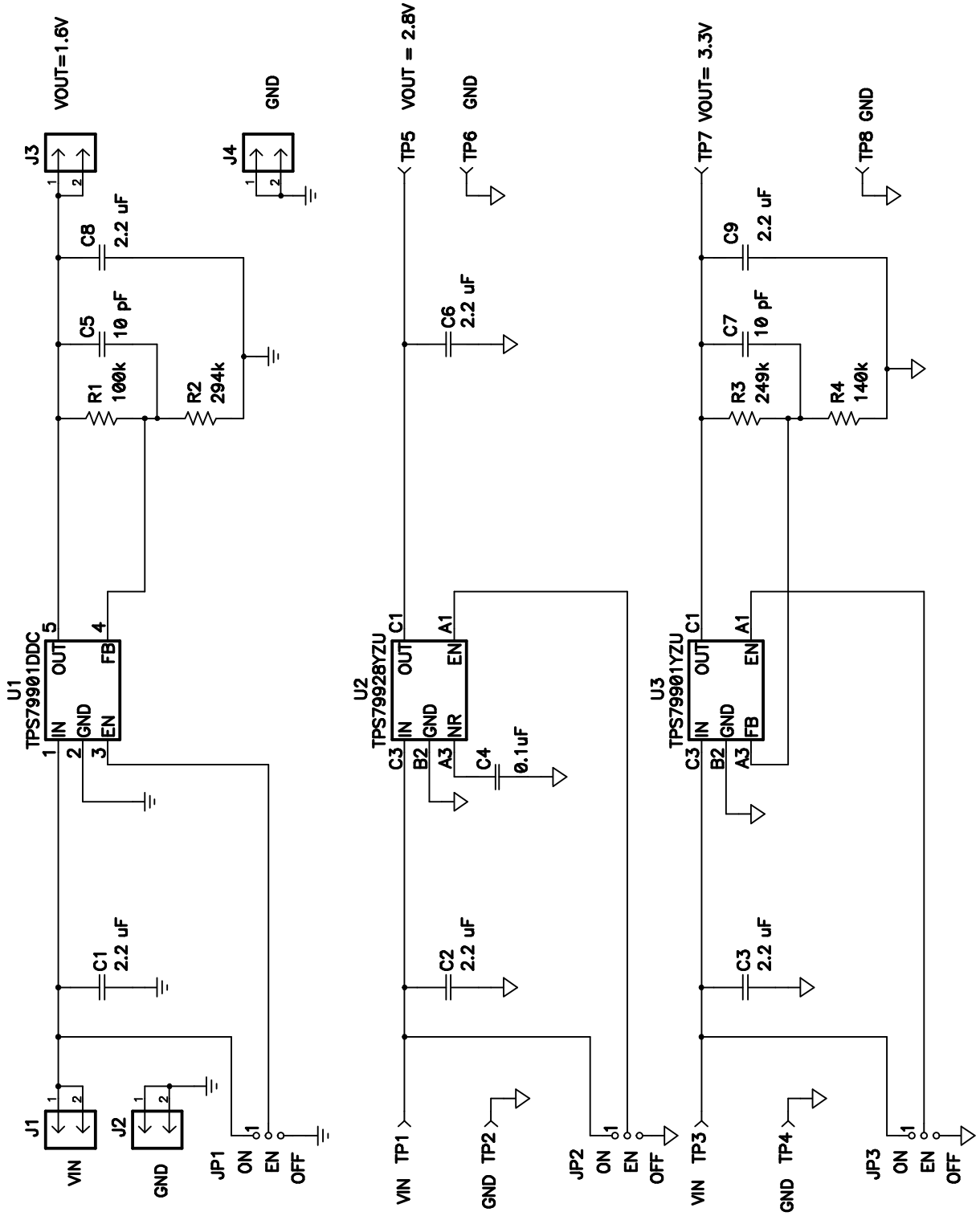

Figure 4. TPS799xxEVM-105 Schematic

4.2 Bill of Materials

Table 3. TPS799xxEVM-105 Bill of Materials

COUNT	Ref Des	Description	Size	Part Number	MFR
6	C1, C2, C3, C6, C8, C9	Capacitor, ceramic, 2.2-µF, 10-V, X5R, ±10%	0603	C1608X5R1A225KT	TDK
1	C4	Capacitor, 0.1-µF, 10-V, X5R, ±10%	0402	C1005X5R1A104K	TDK
2	C5, C7	Capacitor, ceramic, 10-pF, 50-V, C0G, 5%	0603	C1608C0G1H100D	TDK
4	J1, J2, J3, J4	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
3	JP1, JP2, JP3	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	R1	Resistor, chip, 100 kΩ, 1/16-W, 1%	0603	Std	Std
1	R2	Resistor, chip, 294 kΩ, 1/16-W, 1%	0603	Std	Std
1	R3	Resistor, chip, 249 kΩ, 1/16-W, 1%	0402	Std	Std
1	R4	Resistor, chip, 140 kΩ, 1/16-W, 1%	0402	Std	Std
4	TP1, TP3, TP5, TP7	Test point, red, 1 mm	0.038	240-345	Farnell
4	TP2, TP4, TP6, TP8	Test point, black, 1 mm	0.038	240-333	Farnell
1	U1	IC, Ultra-low noise, high PSRR 200 mA, LDO regulators	SOT23-5	TPS79901DDC	TI
1	U2	IC, Ultra-low noise, high PSRR 200 mA, LDO regulators	WCSP-05	TPS79928YZU	TI
1	U3	IC, Ultra-low noise, high PSRR 200 mA, LDO regulators	WCSP-05	TPS79901YZU	TI
1	–	PCB, 1.955 In x 1.23 In x 0.062 In		HPA105	Any
3	–	Shunt, 100-mil, black	0.100	929950-00	3M

4.3 Related Documentation From Texas Instruments

TPS799xx data sheet (SBVS056A)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.775 V to 5.10 V and the output voltage range of 1.60 V to 3.30 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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