

LTC6957-3/LTC6957-4 Low Phase Noise, Dual CMOS Output Buffer/Driver/Logic Converter

DESCRIPTION

Demonstration Circuit 1766A features the [LTC®6957-3/LTC6957-4](#), a low phase noise, dual CMOS output buffer/driver/logic converter.

The DC1766A provides SMA connectors for the differential inputs and the CMOS outputs. The inputs are terminated to on-board 50Ω resistors and the outputs present similar impedance. The DC1766A allows the user to take advantage of the shutdown and bandwidth selection features of the LTC6957. The DC1766A can operate with a single-ended or

differential sine wave or square-wave input signal. Supply the DC1766A with 3.3V and it is ready to function. Or, the output can be powered from a lower voltage supply if a lower voltage CMOS driver is desired. The DC1766A gives extra component population options to make it compatible with different logic signal types.

Design files for this circuit board are available at <http://www.linear.com/demo>

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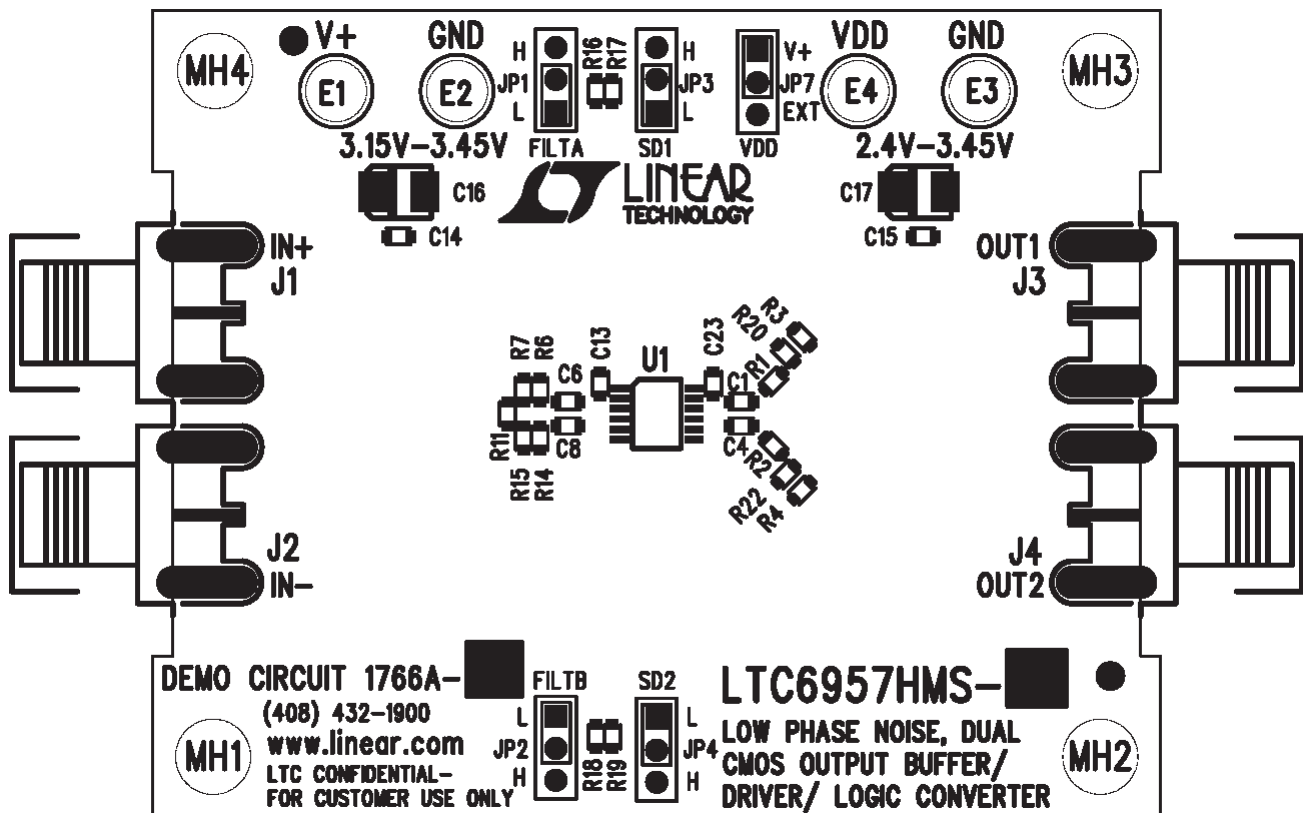


Figure 1. DC1766A Inputs and Outputs

QUICK START PROCEDURE

The DC1766A is very straightforward to operate. Refer to Figure 1 for the following discussion.

DC1766A Configuration

1. Apply a low-noise and low-spurious 3.3V supply between the V+ (E1) and GND (E2) turrets.
2. Make sure that jumper VDD (JP7) is at the V+ position if 3.3V CMOS output operation is desired. Otherwise, apply a voltage that is between 2.4V and 3.3V between the VDD (E4) and GND (E3) turrets, and move jumper VDD (JP7) to EXT position to operate the CMOS outputs at the voltage level supplied at the VDD turret.
3. Connect a low phase noise (or jitter) single-ended or differential input signal to IN+ (J1) and/or IN- (J2) SMA connectors. Refer to the LTC6957 data sheet for appropriate input signal types and levels.
4. Connect either of the outputs (OUT1, J3 or OUT2, J4) to a high-speed scope, spectrum analyzer or a signal analyzer to start the evaluation of the LTC6957.

NOTE: The CMOS outputs of the DC1766A are AC-coupled and attenuated through two 100 Ω resistors as shown in the DC1766A schematic diagram to present a 50 Ω source impedance appropriate to connect to a 50 Ω input impedance instrument.

5. Configure the input bandwidth of the LTC6957 with the use of FILTA (JP1) and FILTB (JP2) jumpers. Follow the instructions given in the LTC6957 data sheet to choose the correct bandwidth given an input signal.
6. Shut down an unused output by using jumper SD1 (JP3) to shutdown OUT1 or jumper SD2 (JP4) to shutdown OUT2.

DC1766A Reconfiguration

The DC1766A is flexible and allows the connectivity of a variety of input and output signal types. The DC1766A is configured as shown in the schematic diagram. However, the DC1766A allows the installation of different input and output configurations to adapt to a variety of logic signals. Refer to the Applications Information section of the LTC6957 data sheet for all possible connectivity options that can be implemented by modifying the DC1766A.

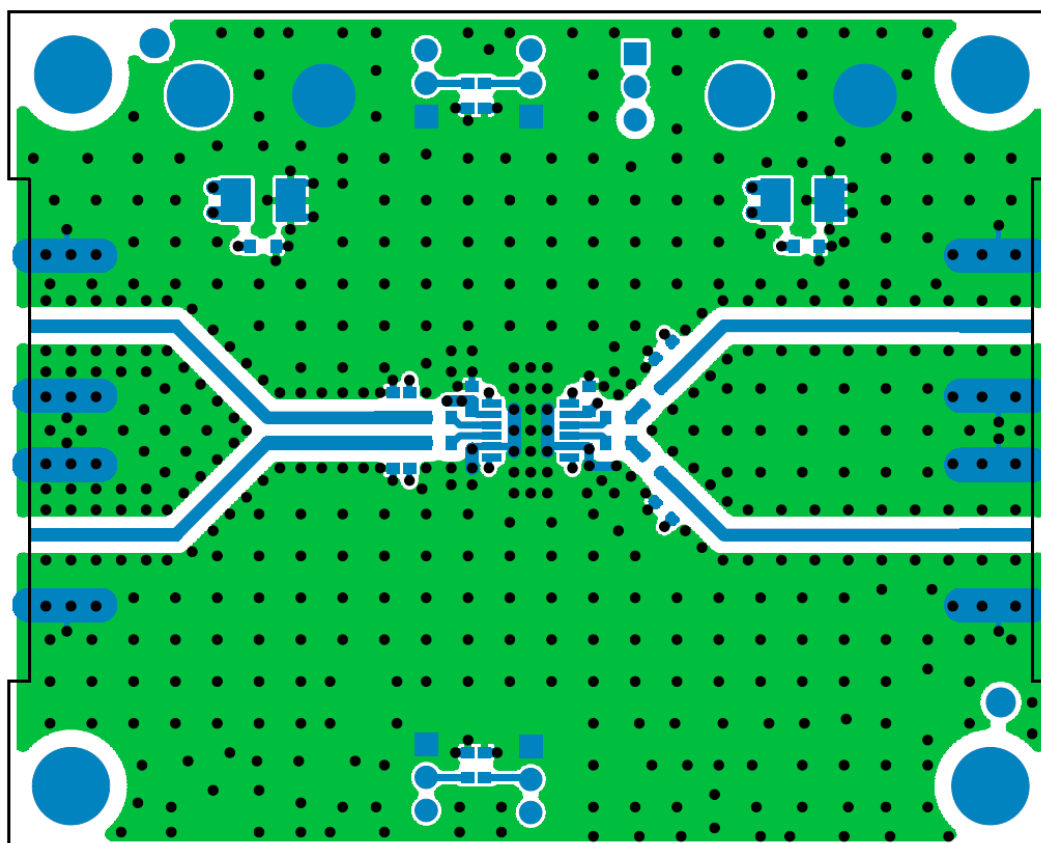
ASSEMBLY OPTIONS

Table 1. DC1766A Assembly Options

ASSEMBLY VERSION	PART NUMBER	OUTPUT TYPE
DC1766A-A	LTC6957HMS-3	In-Phase CMOS
DC1766A-B	LTC6957HMS-4	Complementary CMOS

LAYOUT TOP LAYER

The top metal layer of the DC1766A is shown here as an example of good PCB layout for the LTC6957-3/LTC6957-4.

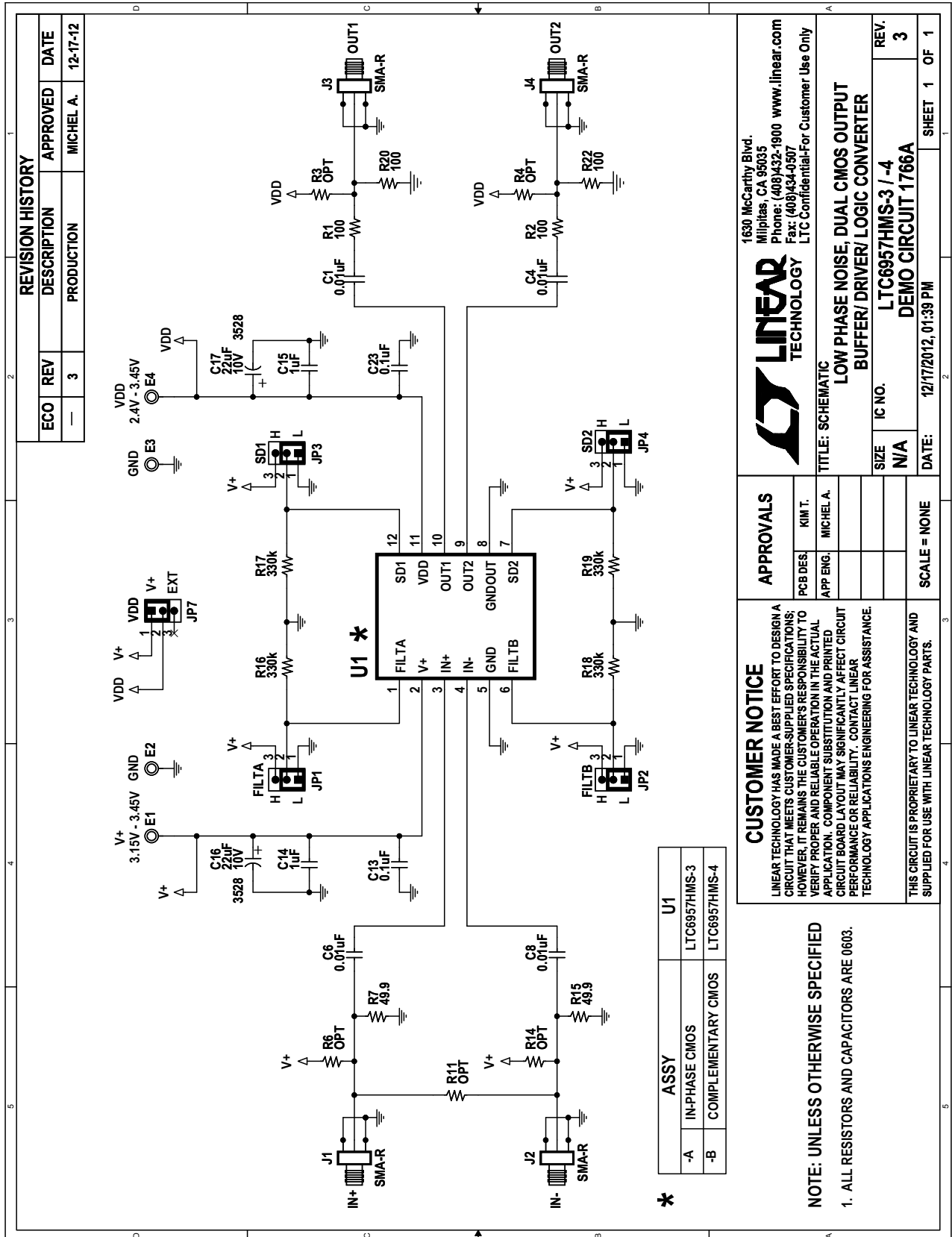


DEMO MANUAL DC1766A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1766A General BOM				
1	4	C1, C4, C6, C8	CAP., X7R, 0.01 μ F 50V 10%, 0603	NIC, NMC0603X7R103K50TRP
2	2	C13, C23	CAP., X7R, 0.1 μ F 50V 10%, 0603	TDK, C1608X7R1H104K
3	2	C14, C15	CAP., X5R, 1 μ F 25V 10%, 0603	TDK, C1608X5R1E105K
4	2	C16, C17	CAP., TANT, 22 μ F 10V, 3528	AVX, TPSB226K010R0400
5	4	E1, E2, E3, E4	TESTPOINT, TURRET 0.094"	MILLMAX, 2501-2-00-80-00-00-07-0
6	5	JP1, JP2, JP3, JP4, JP7	JMP, HD1X3-079	SAMTEC, TMM-103-02-L-S
7	4	J1, J2, J3, J4	CONN., SMA 50 Ω EDGE-LAUNCH	E.F. JOHNSON, 142-0701-851
8	4	R1, R2, R20, R22	RES., CHIP, 100 Ω 1% 0603	VISHAY, CRCW0603100RFKEA
9	0	R3, R4, R6, R11, R14	RES., OPT 0603	OPT
10	2	R7, R15	RES., CHIP, 49.9 Ω 1% 0603	VISHAY, CRCW060349R9FKEA
11	4	R16, R17, R18, R19	RES., CHIP, 330k 1% 0603	VISHAY, CRCW0603330KFKEA
12	4		STAND-OFF, NYLON 0.500	KEYSTONE, 8833 (SNAP ON)
13	5		SHUNT, .079" CENTER	SAMTEC, 2SN-BK-G
DC1766A-A				
1	1		DC1766A General BOM	DC1766A
2	1	U1	IC, LTC6957HMS-3, MS12	LINEAR TECH., LTC6957HMS-3
DC1766A-B				
1	1		DC1766A GENERAL BOM	DC1766A
2	1	U1	IC, LTC6957HMS-4, MS12	LINEAR TECH., LTC6957HMS-4

SCHEMATIC DIAGRAM



REVISION HISTORY				
ECO	REV	DESCRIPTION	APPROVED	DATE
—	3	PRODUCTION	MICHEL A.	12-17-12

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TITLE: SCHEMATIC
LOW PHASE NOISE, DUAL CMOS OUTPUT BUFFER/ DRIVER/ LOGIC CONVERTER

SIZE: N/A IC NO.: LTC6957HMS-3 / -4 REV.: 3
 DATE: 12/17/2012, 01:39 PM SHEET 1 OF 1

APPROVALS	
PCB DES.	KIM T.
APP ENG.	MICHEL A.
SCALE = NONE	

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ASSY	U1
-A	IN-PHASE CMOS
-B	COMPLEMENTARY CMOS

NOTE: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS AND CAPACITORS ARE 0603.



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