



MFRC522

Standard performance MIFARE and NTAG frontend

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112139

Product data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC522.

Remark: The MFRC522 supports all variants of the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus RF identification protocols. To aid readability throughout this data sheet, the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus products and protocols have the generic name MIFARE.

1.1 Differences between version 1.0 and 2.0

The MFRC522 is available in two versions:

- MFRC52201HN1, hereafter referred to version 1.0 and
- MFRC52202HN1, hereafter referred to version 2.0.

The MFRC522 version 2.0 is fully compatible to version 1.0 and offers in addition the following features and improvements:

- Increased stability of the reader IC in rough conditions
- An additional timer prescaler, see [Section 8.5](#).
- A corrected CRC handling when RX Multiple is set to 1

This data sheet version covers both versions of the MFRC522 and describes the differences between the versions if applicable.

2. General description

The MFRC522 is a highly integrated reader/writer IC for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO/IEC 14443 A/MIFARE and NTAG.

The MFRC522's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The MFRC522 supports MF1xxS20, MF1xxS70 and MF1xxS50 products. The MFRC522 supports contactless communication and uses MIFARE higher transfer speeds up to 848 kBd in both directions.



The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependant on pin voltage supply)
- I²C-bus interface

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE and NTAG
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MF1xxS20, MF1xxS70 and MF1xxS50 encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication up to 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces
 - ◆ SPI up to 10 Mbit/s
 - ◆ I²C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
 - ◆ RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|------------------------|--|--------|-----|-----|-----|------|
| V _{DDA} | analog supply voltage | V _{DD(PVDD)} ≤ V _{DDA} = V _{DDD} = V _{DD(TVDD)} ; V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | [1][2] | 2.5 | 3.3 | 3.6 | V |
| V _{DDD} | digital supply voltage | | | 2.5 | 3.3 | 3.6 | V |
| V _{DD(TVDD)} | TVDD supply voltage | | | 2.5 | 3.3 | 3.6 | V |
| V _{DD(PVDD)} | PVDD supply voltage | | [3] | 1.6 | 1.8 | 3.6 | V |
| V _{DD(SVDD)} | SVDD supply voltage | V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | | 1.6 | - | 3.6 | V |

Table 1. Quick reference data ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|----------------------------------|------------------------|---|-----------|-----|-----|------|----|
| I _{pd} | power-down current | V _{D_{DA}} = V _{D_{DD}} = V _{D_D(TVDD)} = V _{D_D(PVDD)} = 3 V | | | | | |
| | | hard power-down; pin NRSTPD set LOW | [4] | - | - | 5 | μA |
| | | soft power-down; RF level detector on | [4] | - | - | 10 | μA |
| I _{DDD} | digital supply current | pin DVDD; V _{D_{DD}} = 3 V | - | 6.5 | 9 | mA | |
| I _{D_{DA}} | analog supply current | pin AVDD; V _{D_{DA}} = 3 V, CommandReg register's RcvOff bit = 0 | - | 7 | 10 | mA | |
| | | pin AVDD; receiver switched off; V _{D_{DA}} = 3 V, CommandReg register's RcvOff bit = 1 | - | 3 | 5 | mA | |
| I _{D_D(PVDD)} | PVDD supply current | pin PVDD | [5] | - | 40 | mA | |
| I _{D_D(TVDD)} | TVDD supply current | pin TVDD; continuous wave | [6][7][8] | - | 60 | 100 | mA |
| T _{amb} | ambient temperature | HVQFN32 | -25 | - | +85 | °C | |

- [1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.
- [2] V_{D_{DA}}, V_{D_{DD}} and V_{D_D(TVDD)} must always be the same voltage.
- [3] V_{D_D(PVDD)} must always be the same or lower voltage than V_{D_{DD}}.
- [4] I_{pd} is the total current for all supplies.
- [5] I_{D_D(PVDD)} depends on the overall load at the digital pins.
- [6] I_{D_D(TVDD)} depends on V_{D_D(TVDD)} and the external circuit connected to pins TX1 and TX2.
- [7] During typical circuit operation, the overall current is below 100 mA.
- [8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

| Type number | Package | | |
|------------------------|---------|---|----------|
| | Name | Description | Version |
| MFRC52201HN1/TRAYB[1] | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm | SOT617-1 |
| MFRC52201HN1/TRAYBM[2] | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm | SOT617-1 |
| MFRC52202HN1/TRAYB[1] | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm | SOT617-1 |
| MFRC52202HN1/TRAYBM[2] | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm | SOT617-1 |

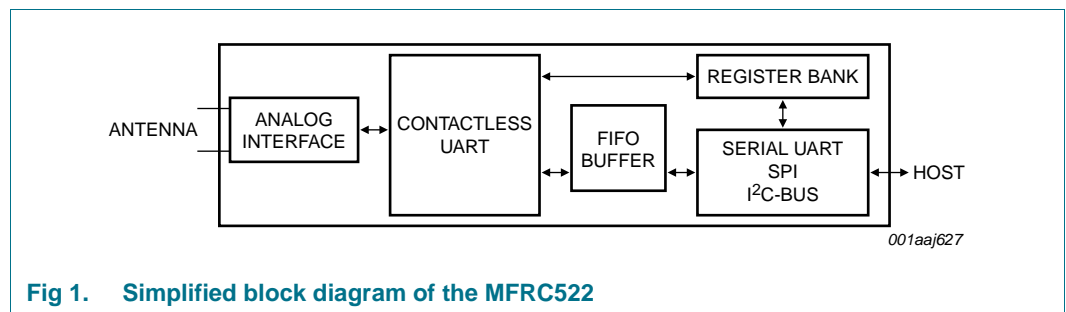
- [1] Delivered in one tray.
- [2] Delivered in five trays.

6. Block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.



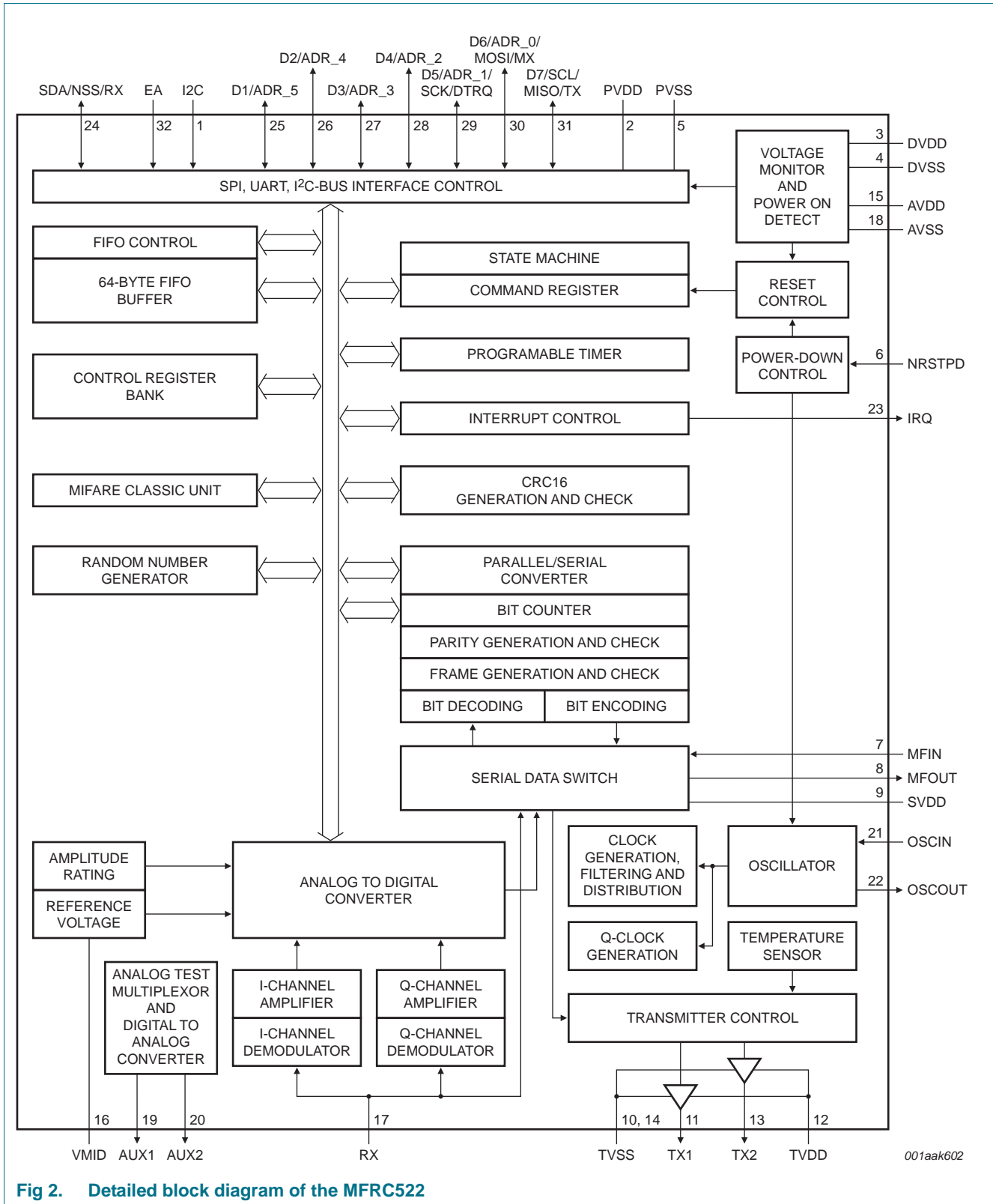


Fig 2. Detailed block diagram of the MFRC522

7. Pinning information

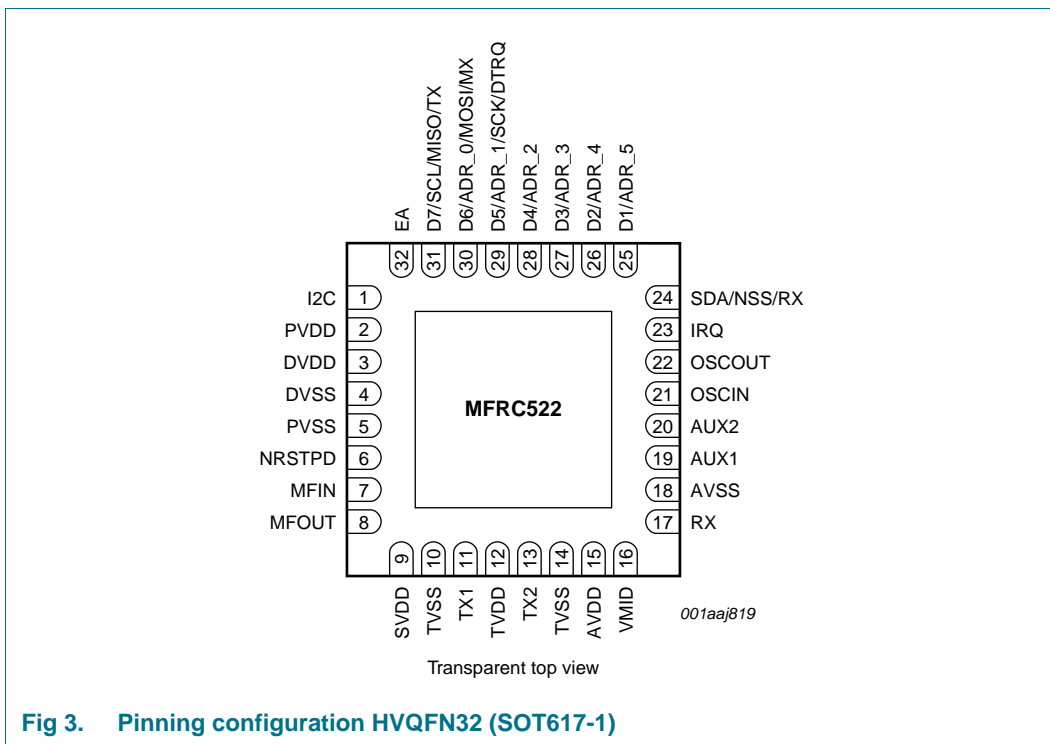


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

| Pin | Symbol | Type ^[1] | Description |
|-----|--------|---------------------|---|
| 1 | I2C | I | I2C-bus enable input ^[2] |
| 2 | PVDD | P | pin power supply |
| 3 | DVDD | P | digital power supply |
| 4 | DVSS | G | digital ground ^[3] |
| 5 | PVSS | G | pin power supply ground |
| 6 | NRSTPD | I | reset and power-down input: power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world reset: enabled by a positive edge |
| 7 | MFIN | I | MIFARE signal input |
| 8 | MFOUT | O | MIFARE signal output |
| 9 | SVDD | P | MFIN and MFOUT pin power supply |
| 10 | TVSS | G | transmitter output stage 1 ground |
| 11 | TX1 | O | transmitter 1 modulated 13.56 MHz energy carrier output |
| 12 | TVDD | P | transmitter power supply: supplies the output stage of transmitters 1 and 2 |
| 13 | TX2 | O | transmitter 2 modulated 13.56 MHz energy carrier output |
| 14 | TVSS | G | transmitter output stage 2 ground |
| 15 | AVDD | P | analog power supply |

Table 3. Pin description ...continued

| Pin | Symbol | Type ^[1] | Description |
|-----|--------|---------------------|---|
| 16 | VMID | P | internal reference voltage |
| 17 | RX | I | RF signal input |
| 18 | AVSS | G | analog ground |
| 19 | AUX1 | O | auxiliary outputs for test purposes |
| 20 | AUX2 | O | auxiliary outputs for test purposes |
| 21 | OSCIN | I | crystal oscillator inverting amplifier input; also the input for an externally generated clock ($f_{clk} = 27.12$ MHz) |
| 22 | OSCOUT | O | crystal oscillator inverting amplifier output |
| 23 | IRQ | O | interrupt request output: indicates an interrupt event |
| 24 | SDA | I/O | I ² C-bus serial data line input/output ^[2] |
| | NSS | I | SPI signal input ^[2] |
| | RX | I | UART address input ^[2] |
| 25 | D1 | I/O | test port ^[2] |
| | ADR_5 | I/O | I ² C-bus address 5 input ^[2] |
| 26 | D2 | I/O | test port |
| | ADR_4 | I | I ² C-bus address 4 input ^[2] |
| 27 | D3 | I/O | test port |
| | ADR_3 | I | I ² C-bus address 3 input ^[2] |
| 28 | D4 | I/O | test port |
| | ADR_2 | I | I ² C-bus address 2 input ^[2] |
| 29 | D5 | I/O | test port |
| | ADR_1 | I | I ² C-bus address 1 input ^[2] |
| | SCK | I | SPI serial clock input ^[2] |
| | DTRQ | O | UART request to send output to microcontroller ^[2] |
| 30 | D6 | I/O | test port |
| | ADR_0 | I | I ² C-bus address 0 input ^[2] |
| | MOSI | I/O | SPI master out, slave in ^[2] |
| | MX | O | UART output to microcontroller ^[2] |
| 31 | D7 | I/O | test port |
| | SCL | I/O | I ² C-bus clock input/output ^[2] |
| | MISO | I/O | SPI master in, slave out ^[2] |
| | TX | O | UART data output to microcontroller ^[2] |
| 32 | EA | I | external address input for coding I ² C-bus address ^[2] |

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in [Section 8.1 "Digital interfaces"](#).

[3] Connection of heatsink pad on package bottom side is not necessary. Optional connection to pin DVSS is possible.

8. Functional description

The MFRC522 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE using various transfer speeds and modulation protocols.



Fig 4. MFRC522 Read/Write mode

The physical level communication is shown in [Figure 5](#).

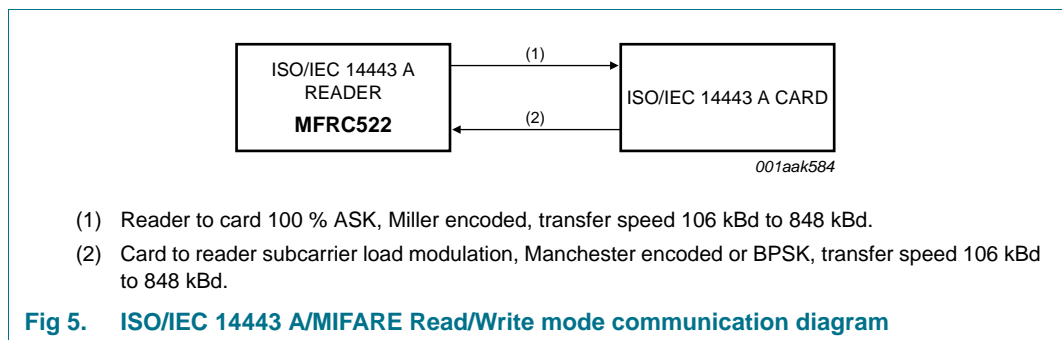


Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in [Table 4](#).

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

| Communication direction | Signal type | Transfer speed | | | |
|---|------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| | | 106 kBd | 212 kBd | 424 kBd | 848 kBd |
| Reader to card (send data from the MFRC522 to a card) | reader side modulation | 100 % ASK | 100 % ASK | 100 % ASK | 100 % ASK |
| | bit encoding | modified Miller encoding | modified Miller encoding | modified Miller encoding | modified Miller encoding |
| | bit length | 128 (13.56 μs) | 64 (13.56 μs) | 32 (13.56 μs) | 16 (13.56 μs) |
| Card to reader (MFRC522 receives data from a card) | card side modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation |
| | subcarrier frequency | 13.56 MHz / 16 | 13.56 MHz / 16 | 13.56 MHz / 16 | 13.56 MHz / 16 |
| | bit encoding | Manchester encoding | BPSK | BPSK | BPSK |

The MFRC522's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. [Figure 6](#) shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.



The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the MfRxReg register's ParityDisable bit.

8.1 Digital interfaces

8.1.1 Automatic microcontroller interface detection

The MFRC522 supports direct interfacing of hosts using SPI, I²C-bus or serial UART interfaces. The MFRC522 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The MFRC522 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. [Table 5](#) shows the different connection configurations.

Table 5. Connection protocol for detecting different interface types

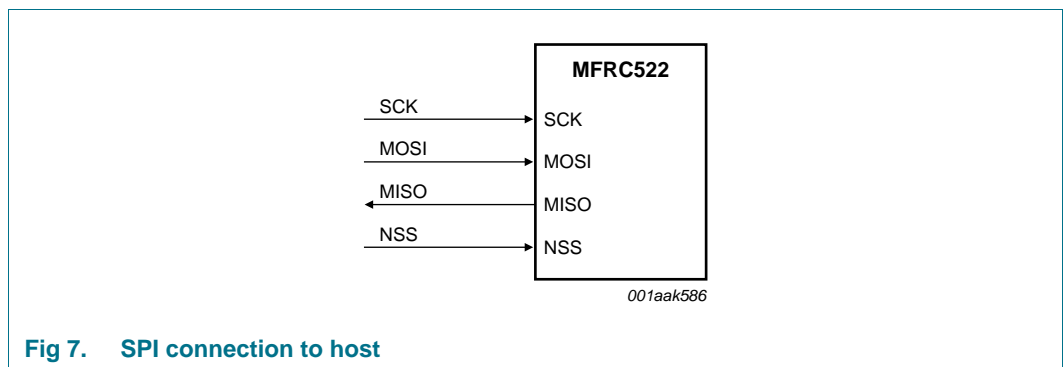
| Pin | Interface type | | |
|-----|----------------|--------------|----------------------------|
| | UART (input) | SPI (output) | I ² C-bus (I/O) |
| SDA | RX | NSS | SDA |
| I2C | 0 | 0 | 1 |
| EA | 0 | 1 | EA |
| D7 | TX | MISO | SCL |
| D6 | MX | MOSI | ADR_0 |
| D5 | DTRQ | SCK | ADR_1 |
| D4 | - | - | ADR_2 |
| D3 | - | - | ADR_3 |
| D2 | - | - | ADR_4 |
| D1 | - | - | ADR_5 |

8.1.2 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the MFRC522 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC522 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in [Section 14.1 on page 78](#).



The MFRC522 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC522 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the MFRC522 on the falling clock edge and is stable during the rising clock edge.

8.1.2.1 SPI read data

Reading data using SPI requires the byte order shown in [Table 6](#) to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

| Line | Byte 0 | Byte 1 | Byte 2 | To | Byte n | Byte n + 1 |
|------|------------------|-----------|-----------|-----|------------|------------|
| MOSI | address 0 | address 1 | address 2 | ... | address n | 00 |
| MISO | X ^[1] | data 0 | data 1 | ... | data n – 1 | data n |

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.2 SPI write data

To write data to the MFRC522 using SPI requires the byte order shown in [Table 7](#). It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

| Line | Byte 0 | Byte 1 | Byte 2 | To | Byte n | Byte n + 1 |
|------|------------------|------------------|------------------|-----|------------------|------------------|
| MOSI | address 0 | data 0 | data 1 | ... | data n – 1 | data n |
| MISO | X ^[1] | X ^[1] | X ^[1] | ... | X ^[1] | X ^[1] |

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.3 SPI address byte

The address byte must meet the following format.

The MSB of the first byte defines the mode used. To read data from the MFRC522 the MSB is set to logic 1. To write data to the MFRC522 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

Table 8. Address byte 0 register; address MOSI

| 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|-----------------------|---------|---|---|---|---|---|---------|
| 1 = read 0 = write | address | | | | | | 0 |

8.1.3 UART interface

8.1.3.1 Connection to a host

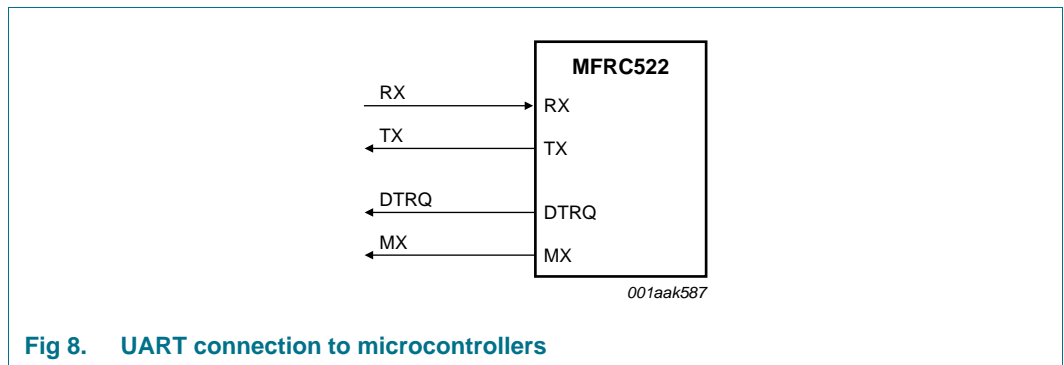


Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.1.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in [Table 9](#). Examples of different transfer speeds and the relevant register settings are given in [Table 10](#).

Table 9. BR_T0 and BR_T1 settings

| BR_Tn | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
|--------------|---------|----------|----------|----------|----------|----------|----------|----------|
| BR_T0 factor | 1 | 1 | 2 | 4 | 8 | 16 | 32 | 64 |
| BR_T1 range | 1 to 32 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 | 33 to 64 |

Table 10. Selectable UART transfer speeds

| Transfer speed (kBd) | SerialSpeedReg value | | Transfer speed accuracy (%) ^[1] |
|----------------------|----------------------|-------------|--|
| | Decimal | Hexadecimal | |
| 7.2 | 250 | FAh | -0.25 |
| 9.6 | 235 | EBh | 0.32 |
| 14.4 | 218 | DAh | -0.25 |
| 19.2 | 203 | CBh | 0.32 |
| 38.4 | 171 | ABh | 0.32 |
| 57.6 | 154 | 9Ah | -0.25 |
| 115.2 | 122 | 7Ah | -0.25 |
| 128 | 116 | 74h | -0.06 |
| 230.4 | 90 | 5Ah | -0.25 |
| 460.8 | 58 | 3Ah | -0.25 |
| 921.6 | 28 | 1Ch | 1.45 |
| 1228.8 | 21 | 15h | 0.32 |

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in [Table 10](#) are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR_T0 + 1)} \tag{1}$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{\frac{(BR_T1 + 33)}{2^{(BR_T0 - 1)}}} \right) \tag{2}$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

8.1.3.3 UART framing

Table 11. UART framing

| Bit | Length | Value |
|-------|--------|-------|
| Start | 1-bit | 0 |
| Data | 8 bits | data |
| Stop | 1-bit | 1 |

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

Read data: To read data using the UART interface, the flow shown in Table 12 must be used. The first byte sent defines both the mode and the address.

Table 12. Read data byte order

| Pin | Byte 0 | Byte 1 |
|-------------|---------|--------|
| RX (pin 24) | address | - |
| TX (pin 31) | - | data 0 |

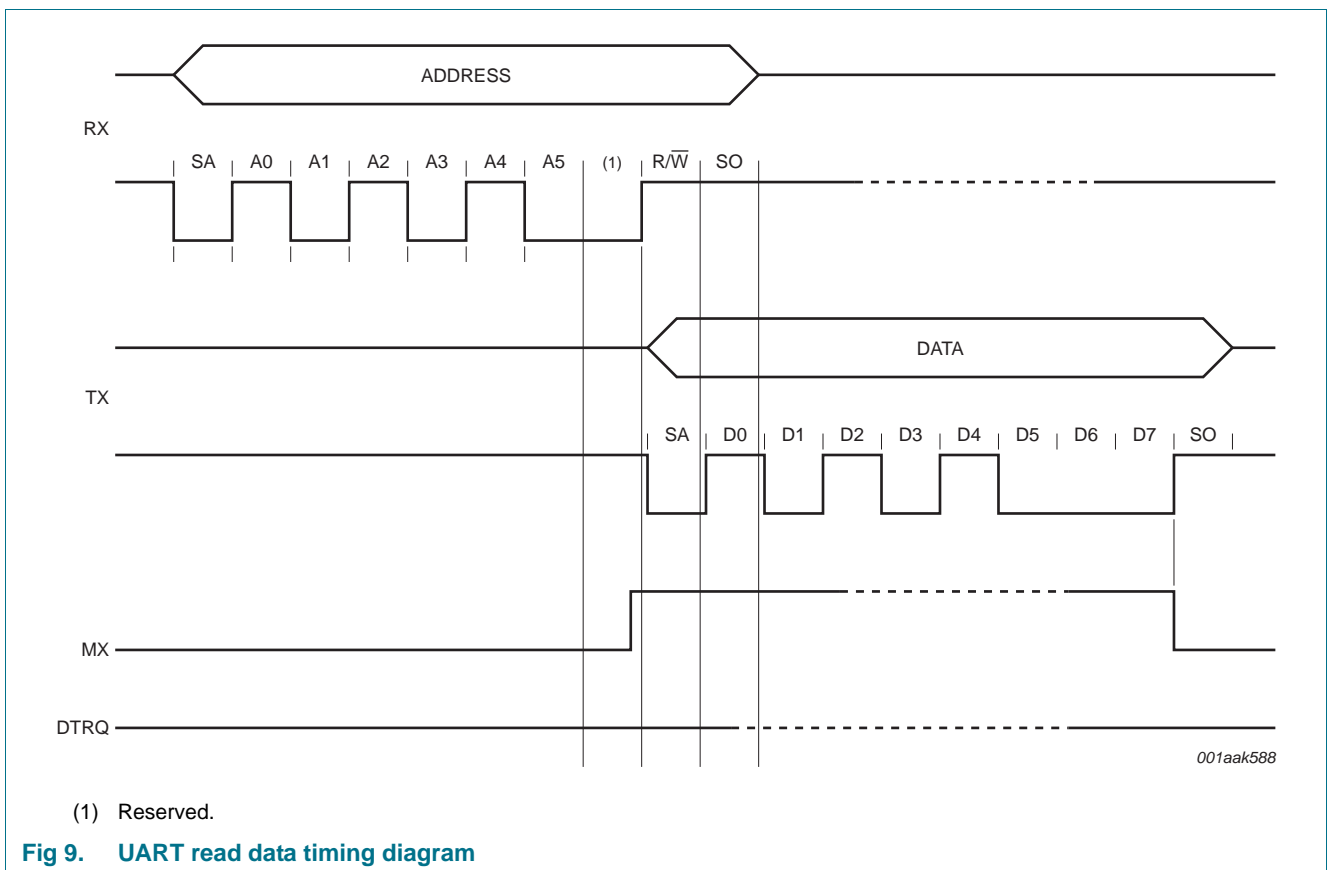


Fig 9. UART read data timing diagram

Write data: To write data to the MFRC522 using the UART interface, the structure shown in Table 13 must be used.

The first byte sent defines both the mode and the address.

Table 13. Write data byte order

| Pin | Byte 0 | Byte 1 |
|-------------|-----------|-----------|
| RX (pin 24) | address 0 | data 0 |
| TX (pin 31) | - | address 0 |

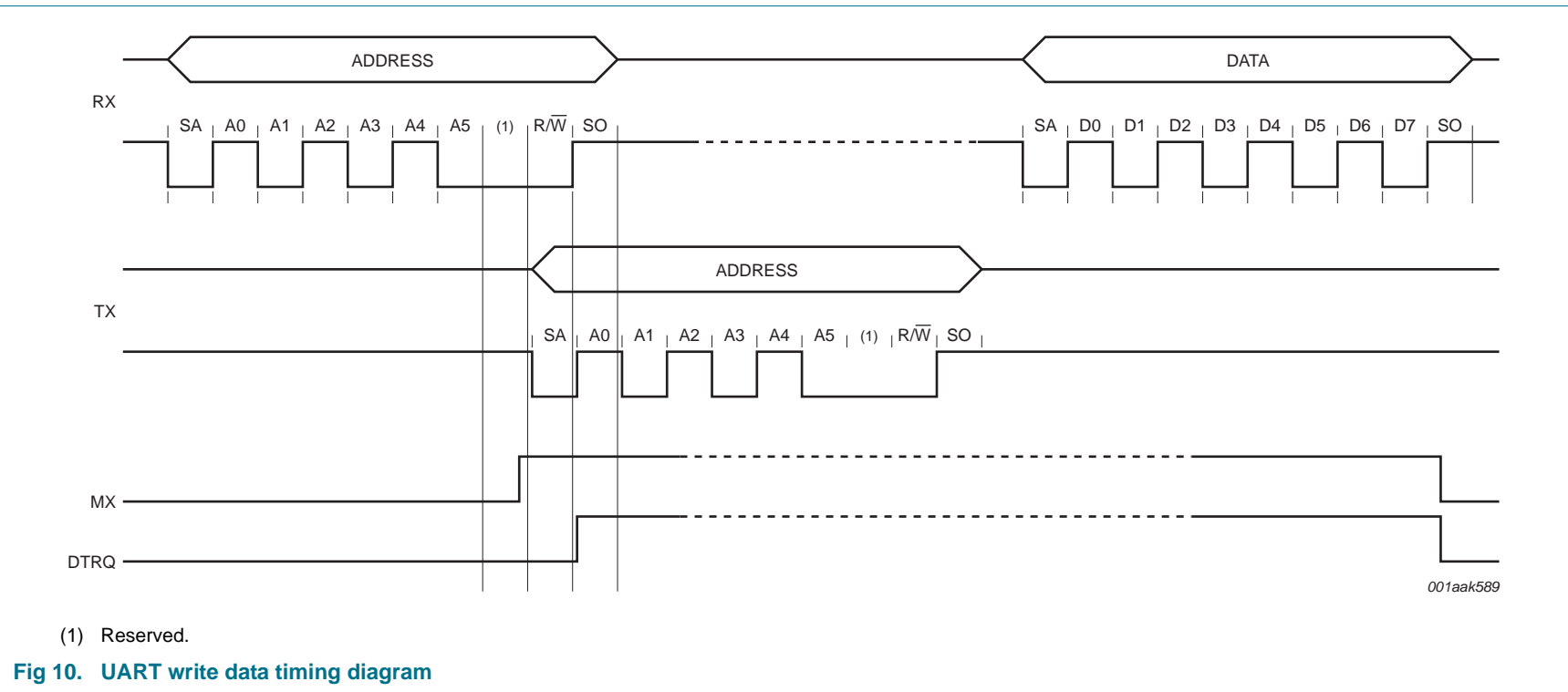


Fig 10. UART write data timing diagram

Remark: The data byte can be sent directly after the address byte on pin RX.

Address byte: The address byte has to meet the following format:

The MSB of the first byte sets the mode used. To read data from the MFRC522, the MSB is set to logic 1. To write data to the MFRC522 the MSB is set to logic 0. Bit 6 is reserved for future use, and bits 5 to 0 define the address; see [Table 14](#).

Table 14. Address byte 0 register; address MOSI

| 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|-----------------------|----------|---------|---|---|---|---|---------|
| 1 = read 0 = write | reserved | address | | | | | |

8.1.4 I²C-bus interface

An I²C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented according to NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in Slave mode. Therefore the MFRC522 does not implement clock generation or access arbitration.

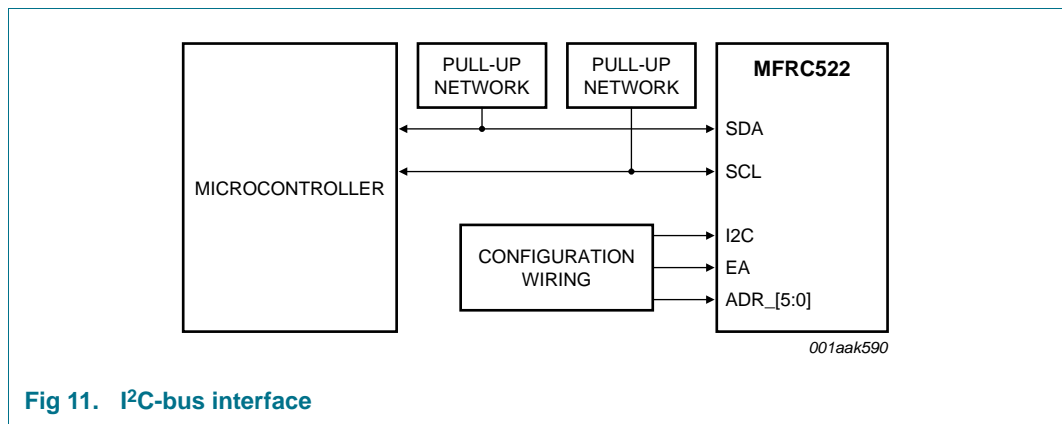


Fig 11. I²C-bus interface

The MFRC522 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC522 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See [Table 155 on page 79](#) for timing requirements.

8.1.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

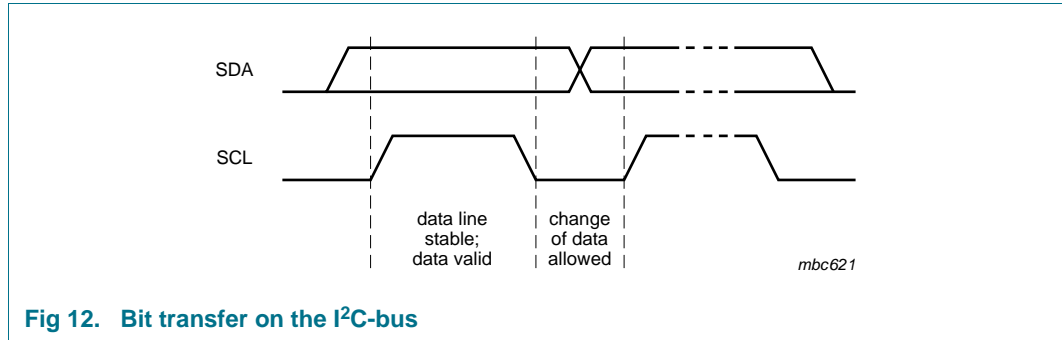


Fig 12. Bit transfer on the I²C-bus

8.1.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

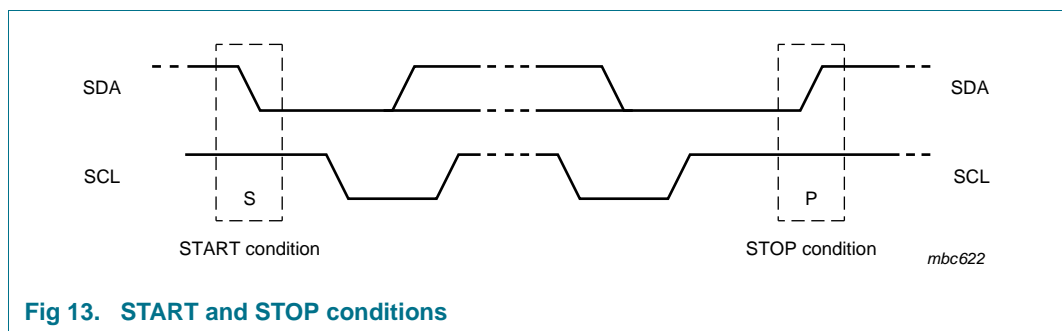


Fig 13. START and STOP conditions

8.1.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see [Figure 16](#). The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

8.1.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

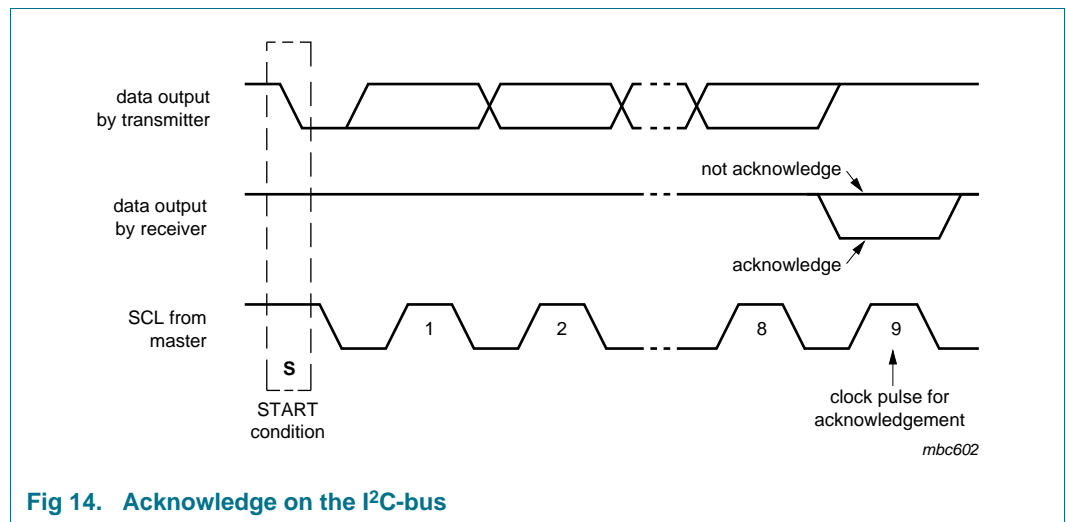


Fig 14. Acknowledge on the I²C-bus



Fig 15. Data transfer on the I²C-bus

8.1.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all MFRC522 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to [Table 5 on page 9](#). ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.



Fig 16. First byte following the START procedure

8.1.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the MFRC522 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/W) bit is set to logic 0.

8.1.4.7 Register read access

To read out data from a specific register address in the MFRC522, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I²C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the MFRC522. In response, the MFRC522 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to logic 1.



Fig 17. Register read and write access

8.1.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard mode (F/S mode) for bidirectional communication in a mixed-speed bus system.

8.1.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I²C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.1.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I²C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXXb)
3. Not-acknowledge bit (\bar{A})

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected MFRC522.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

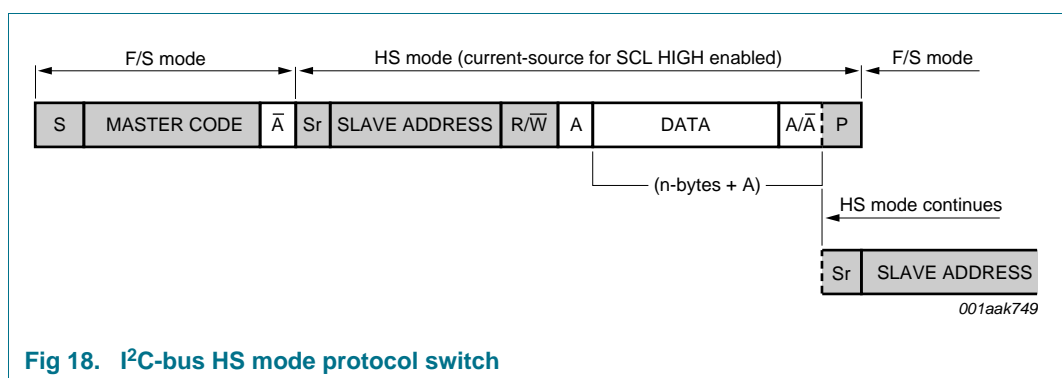


Fig 18. I²C-bus HS mode protocol switch

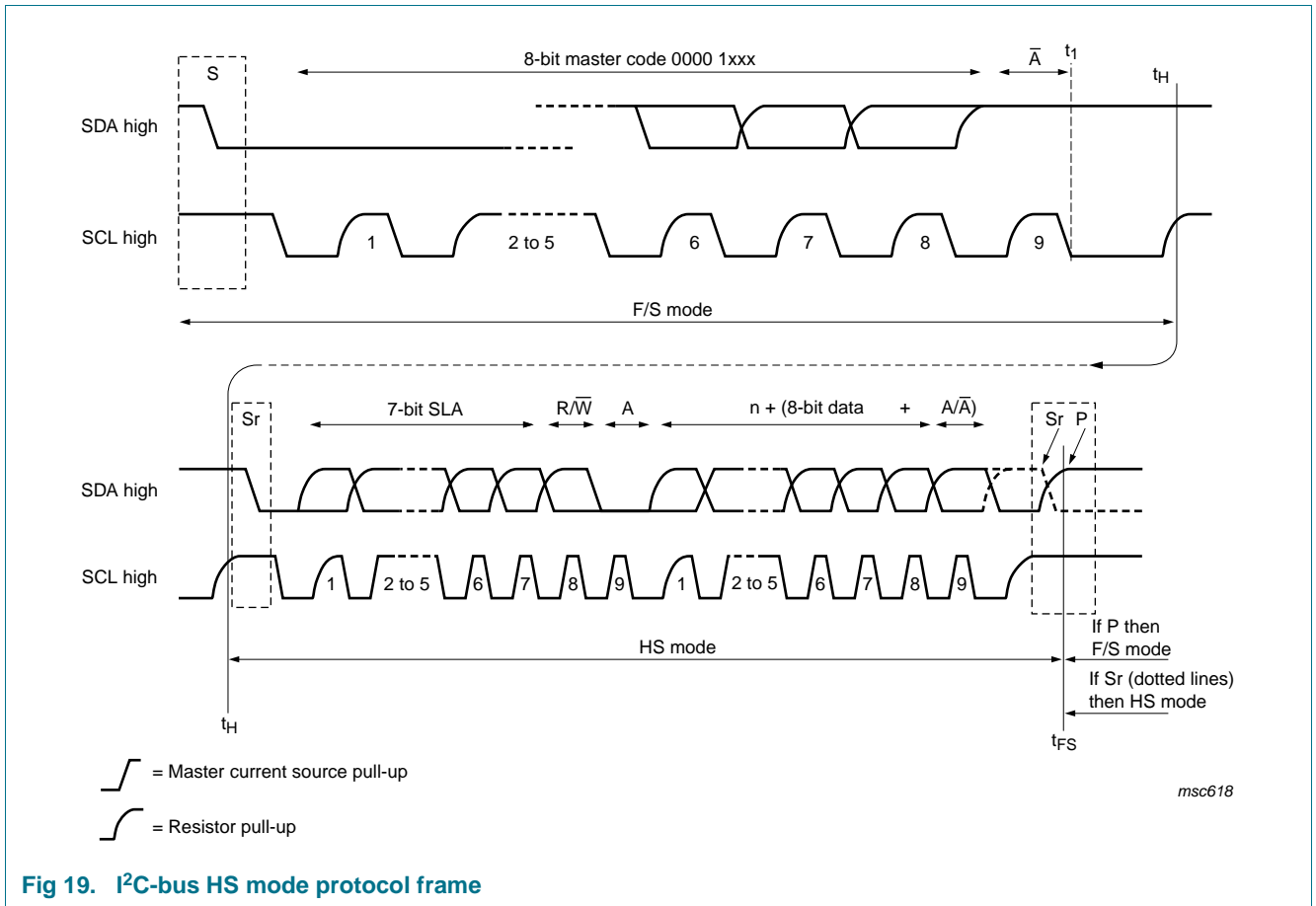


Fig 19. I²C-bus HS mode protocol frame

8.1.4.11 Switching between F/S mode and HS mode

After reset and initialization, the MFRC522 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected MFRC522 recognizes the "S 00001XXX A" sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I²C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register's I²CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I²C-bus lines must be avoided because of the reduced spike suppression.

8.1.4.12 MFRC522 at lower speed modes

MFRC522 is fully downward-compatible and can be connected to an F/S mode I²C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

8.2 Analog interface and contactless UART

8.2.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

8.2.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see [Section 15 on page 81](#). The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see [Section 9.3.2.5 on page 50](#).

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 15. Register and bit settings controlling the signal on pin TX1

| Bit Tx1RFEn | Bit Force 100ASK | Bit InvTx1RFOn | Bit InvTx1RFOff | Envelope | Pin TX1 | GSPMos | GSNMos | Remarks |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--|
| 0 | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | not specified if RF is switched off |
| 1 | 0 | 0 | X ^[1] | 0 | RF | pMod | nMod | 100 % ASK: pin TX1 pulled to logic 0, independent of the InvTx1RFOff bit |
| | | | | 1 | RF | pCW | nCW | |
| | 0 | 1 | X ^[1] | 0 | RF | pMod | nMod | |
| | | | | 1 | RF | pCW | nCW | |
| | 1 | 1 | X ^[1] | 0 | 0 | pMod | nMod | |
| | | | | 1 | RF_n | pCW | nCW | |

[1] X = Do not care.

Table 16. Register and bit settings controlling the signal on pin TX2

| Bit Tx1RFEn | Bit Force 100ASK | Bit Tx2CW | Bit InvTx2RFOOn | Bit InvTx2RFOff | Envelope | Pin TX2 | GSPMos | GSNMos | Remarks | | | |
|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---|-------------------------------------|--|------|------|
| 0 | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | X ^[1] | not specified if RF is switched off | | | |
| 1 | 0 | 0 | 0 | X ^[1] | 0 | RF | pMod | nMod | - | | | |
| | | | | | 1 | RF | pCW | nCW | | | | |
| | | | 1 | X ^[1] | 0 | RF_n | pMod | nMod | | | | |
| | | | | | 1 | RF_n | pCW | nCW | | | | |
| | 1 | 0 | X ^[1] | X ^[1] | RF | pCW | nCW | conductance always CW for the Tx2CW bit | | | | |
| | | | | | RF_n | pCW | nCW | | | | | |
| | 1 | 0 | 0 | X ^[1] | X ^[1] | 0 | 0 | pMod | nMod | 100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOOn/InvTx2RFOff bits) | | |
| | | | | | | 1 | RF | pCW | nCW | | | |
| | | | | | | 1 | X ^[1] | 0 | 0 | | pMod | nMod |
| | | | | | | | | 1 | RF_n | | pCW | nCW |
| 1 | | | | | | 0 | X ^[1] | X ^[1] | RF | | pCW | nCW |
| | | | | | | | | | RF_n | | pCW | nCW |

[1] X = Do not care.

The following abbreviations have been used in [Table 15](#) and [Table 16](#):

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = do not care.

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

8.2.3 Serial data switch

Two main blocks are implemented in the MFRC522. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT.

This topology allows the analog block of the MFRC522 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for p-driver TX1 and TX2.

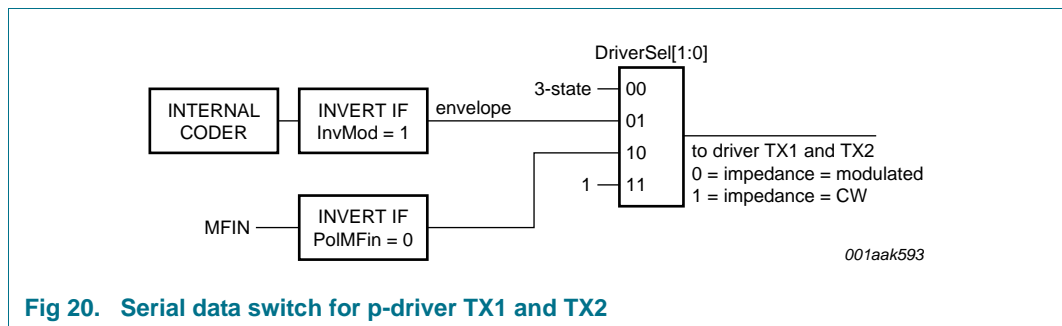


Fig 20. Serial data switch for p-driver TX1 and TX2

8.2.4 MFIN and MFOUT interface support

The MFRC522 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic and so on. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured so that the interfacing signals can be routed to pins MFIN and MFOUT; see Figure 21 on page 28. This configuration is implemented using TxSelReg register’s MFOutSel[3:0] and DriverSel[1:0] bits and RxSelReg register’s UARTSel[1:0] bits.

This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for test purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MFRC522’s digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

Remark: Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS. If pin MFIN is not used it must be connected to either pin SVDD or pin PVSS. If pin SVDD is not used it must be connected to either pin DVDD, pin PVDD or any other voltage supply pin.



Fig 21. Overview of MFIN and MFOUT signal routing

8.2.5 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register’s CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register’s MSBFirst bit indicates that data will be loaded with the MSB first.

Table 17. CRC coprocessor parameters

| Parameter | Value |
|---------------------|---|
| CRC register length | 16-bit CRC |
| CRC algorithm | algorithm according to ISO/IEC 14443 A and ITU-T |
| CRC preset value | 0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register’s CRCPreset[1:0] bits |

8.3 FIFO buffer

An 8 × 64 bit FIFO buffer is used in the MFRC522. It buffers the input and output data stream between the host and the MFRC522’s internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

8.3.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the MFRC522 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

8.3.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register’s FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register’s BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

8.3.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register’s FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register’s HiAlert bit

- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The MFRC522 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. It is generated according to [Equation 3](#):

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (3)$$

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1. It is generated according to [Equation 4](#):

$$LoAlert = FIFOLength \leq WaterLevel \quad (4)$$

8.4 Interrupt request system

The MFRC522 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

8.4.1 Interrupt sources overview

[Table 18](#) shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see [Table 149 on page 70](#)).

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

Table 18. Interrupt sources

| Interrupt flag | Interrupt source | Trigger action |
|----------------|--------------------|--|
| IRq | timer unit | the timer counts from 1 to 0 |
| TxIRq | transmitter | a transmitted data stream ends |
| CRCIRq | CRC coprocessor | all data from the FIFO buffer has been processed |
| RxIRq | receiver | a received data stream ends |
| IdleIRq | ComIrqReg register | command execution finishes |
| HiAlertIRq | FIFO buffer | the FIFO buffer is almost full |
| LoAlertIRq | FIFO buffer | the FIFO buffer is almost empty |
| ErrIRq | contactless UART | an error is detected |

8.5 Timer unit

The MFRC522A has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. Furthermore, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter. The reload values (TReloadVal_Hi[7:0] and TReloadVal_Lo[7:0]) for TPrescaler can be set between 0 and 4095 in the TModeReg register's TPrescaler_Hi[3:0] bits and TPrescalerReg register's TPrescaler_Lo[7:0] bits.

The reload value for the counter is defined by 16 bits between 0 and 65535 in the TReloadReg register.

The current value of the timer is indicated in the TCounterValReg register.

When the counter reaches 0, an interrupt is automatically generated, indicated by the ComIrqReg register's TimerIRq bit setting. If enabled, this event can be indicated on pin IRQ. The TimerIRq bit can be set and reset by the host. Depending on the configuration, the timer will stop at 0 or restart with the value set in the TReloadReg register.

The timer status is indicated by the Status1Reg register's TRunning bit.

The timer can be started manually using the ControlReg register's TStartNow bit and stopped using the ControlReg register's TStopNow bit.

The timer can also be activated automatically to meet any dedicated protocol requirements by setting the TModeReg register's TAuto bit to logic 1.

The delay time of a timer stage is set by the reload value + 1. The total delay time (t_{d1}) is calculated using [Equation 5](#):

$$t_{d1} = \frac{(TPrescaler \times 2 + 1) \times (TReloadVal + 1)}{13.56 \text{ MHz}} \quad (5)$$

An example of calculating total delay time (t_d) is shown in [Equation 6](#), where the TPrescaler value = 4095 and TReloadVal = 65535:

$$39.59 \text{ s} = \frac{(4095 \times 2 + 1) \times (65535 + 1)}{13.56 \text{ MHz}} \quad (6)$$

Example: To give a delay time of 25 μs requires 339 clock cycles to be counted and a TPrescaler value of 169. This configures the timer to count up to 65535 time-slots for every 25 μs period.

The MFRC522 version 2.0 offers in addition a second prescaler timer. Due to the fact that the prescaler counts down to 0 the prescaler period always count an odd number of clocks (1, 3, 5, ..). This may lead to inaccuracy. The second available prescaler timer implements the possibility to change the prescaler reload value to odd numbers, which results in an even prescaler period. This new prescaler can be enabled only in version 2.0 using the register bit DemodeReg, see [Table 72](#). Within this option, the total delay time (t_{d2}) is calculated using [Equation 5](#):

$$t_{d2} = \frac{(TPrescaler \times 2 + 2) \times (TReloadVal + 1)}{13.56 \text{ MHz}} \quad (7)$$

8.6 Power reduction modes

8.6.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

8.6.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the MFRC522 when Soft power-down mode is exited.

Remark: If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time (t_{osc}) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the MFRC522. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the MFRC522 answers to the last read command with the register content of address 0. This indicates that the MFRC522 is ready.

8.6.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

8.7 Oscillator circuit

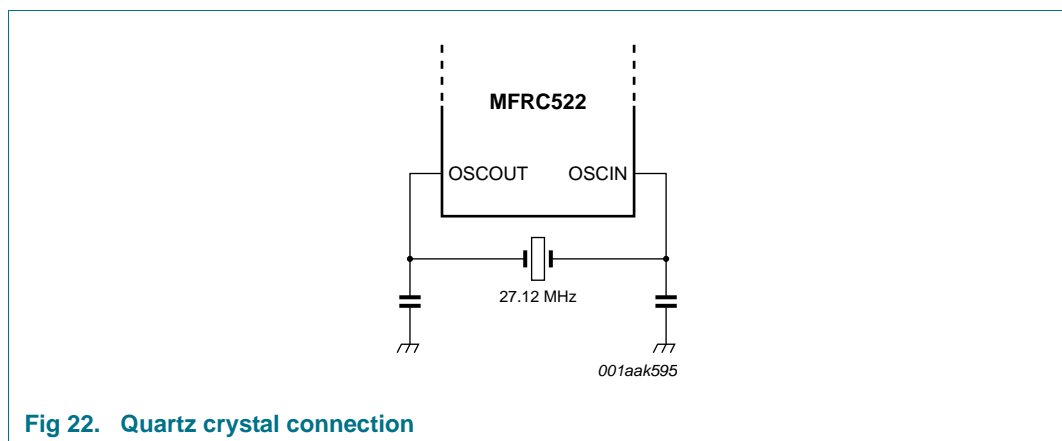


Fig 22. Quartz crystal connection

The clock applied to the MFRC522 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

8.8 Reset and oscillator start-up time

8.8.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

8.8.2 Oscillator start-up time

If the MFRC522 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the MFRC522 depends on the oscillator used and is shown in [Figure 23](#).

The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (t_d) is the internal delay time of the MFRC522 when the clock signal is stable before the MFRC522 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27 \mu s} = 37.74 \mu s \tag{8}$$

The time (t_{osc}) is the sum of t_d and $t_{startup}$.

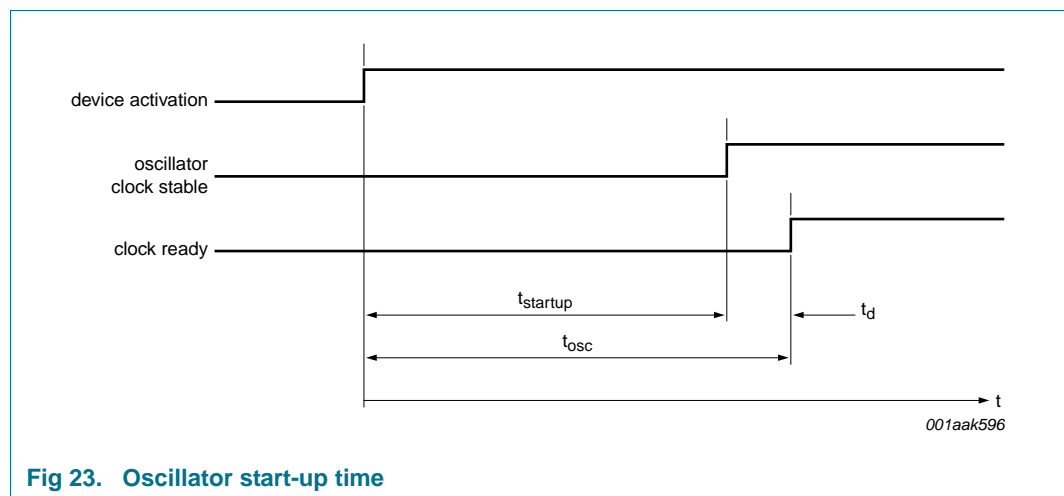


Fig 23. Oscillator start-up time

9. MFRC522 registers

9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in [Table 19](#).

Table 19. Behavior of register bits and their designation

| Abbreviation | Behavior | Description |
|--------------|----------------|---|
| R/W | read and write | These bits can be written and read by the microcontroller. Since they are used only for control purposes, their content is not influenced by internal state machines, for example the ComIEnReg register can be written and read by the microcontroller. It will also be read by internal state machines but never changed by them. |
| D | dynamic | These bits can be written and read by the microcontroller. Nevertheless, they can also be written automatically by internal state machines, for example the CommandReg register changes its value automatically after the execution of the command. |
| R | read only | These register bits hold values which are determined by internal states only, for example the CRCReady bit cannot be written externally but shows internal states. |
| W | write only | Reading these register bits always returns zero. |
| reserved | - | These registers are reserved for future use and must not be changed. In case of a write access, it is recommended to always write the value "0". |
| RFT | - | These register bits are reserved for future use or are for production tests and must not be changed. |

9.2 Register overview

Table 20. MFRC522 register overview

| Address (hex) | Register name | Function | Refer to |
|-----------------------------------|----------------|--|-------------------------------------|
| Page 0: Command and status | | | |
| 00h | Reserved | reserved for future use | Table 21 on page 38 |
| 01h | CommandReg | starts and stops command execution | Table 23 on page 38 |
| 02h | ComlEnReg | enable and disable interrupt request control bits | Table 25 on page 38 |
| 03h | DivlEnReg | enable and disable interrupt request control bits | Table 27 on page 39 |
| 04h | ComlIrqReg | interrupt request bits | Table 29 on page 39 |
| 05h | DivlIrqReg | interrupt request bits | Table 31 on page 40 |
| 06h | ErrorReg | error bits showing the error status of the last command executed | Table 33 on page 41 |
| 07h | Status1Reg | communication status bits | Table 35 on page 42 |
| 08h | Status2Reg | receiver and transmitter status bits | Table 37 on page 43 |
| 09h | FIFODataReg | input and output of 64 byte FIFO buffer | Table 39 on page 44 |
| 0Ah | FIFOLevelReg | number of bytes stored in the FIFO buffer | Table 41 on page 44 |
| 0Bh | WaterLevelReg | level for FIFO underflow and overflow warning | Table 43 on page 44 |
| 0Ch | ControlReg | miscellaneous control registers | Table 45 on page 45 |
| 0Dh | BitFramingReg | adjustments for bit-oriented frames | Table 47 on page 46 |
| 0Eh | CollReg | bit position of the first bit-collision detected on the RF interface | Table 49 on page 46 |
| 0Fh | Reserved | reserved for future use | Table 51 on page 47 |
| Page 1: Command | | | |
| 10h | Reserved | reserved for future use | Table 53 on page 47 |
| 11h | ModeReg | defines general modes for transmitting and receiving | Table 55 on page 48 |
| 12h | TxModeReg | defines transmission data rate and framing | Table 57 on page 48 |
| 13h | RxModeReg | defines reception data rate and framing | Table 59 on page 49 |
| 14h | TxControlReg | controls the logical behavior of the antenna driver pins TX1 and TX2 | Table 61 on page 50 |
| 15h | TxASKReg | controls the setting of the transmission modulation | Table 63 on page 51 |
| 16h | TxSelReg | selects the internal sources for the antenna driver | Table 65 on page 51 |
| 17h | RxSelReg | selects internal receiver settings | Table 67 on page 52 |
| 18h | RxThresholdReg | selects thresholds for the bit decoder | Table 69 on page 53 |
| 19h | DemodReg | defines demodulator settings | Table 71 on page 53 |
| 1Ah | Reserved | reserved for future use | Table 73 on page 54 |
| 1Bh | Reserved | reserved for future use | Table 75 on page 54 |
| 1Ch | MfTxReg | controls some MIFARE communication transmit parameters | Table 77 on page 55 |
| 1Dh | MfRxReg | controls some MIFARE communication receive parameters | Table 79 on page 55 |
| 1Eh | Reserved | reserved for future use | Table 81 on page 55 |
| 1Fh | SerialSpeedReg | selects the speed of the serial UART interface | Table 83 on page 55 |
| Page 2: Configuration | | | |
| 20h | Reserved | reserved for future use | Table 85 on page 57 |

Table 20. MFRC522 register overview ...continued

| Address (hex) | Register name | Function | Refer to |
|------------------------------|-----------------|--|---|
| 21h | CRCResultReg | shows the MSB and LSB values of the CRC calculation | Table 87 on page 57 |
| 22h | | | Table 89 on page 57 |
| 23h | Reserved | reserved for future use | Table 91 on page 58 |
| 24h | ModWidthReg | controls the ModWidth setting | Table 93 on page 58 |
| 25h | Reserved | reserved for future use | Table 95 on page 58 |
| 26h | RFCfgReg | configures the receiver gain | Table 97 on page 59 |
| 27h | GsNReg | selects the conductance of the antenna driver pins TX1 and TX2 for modulation | Table 99 on page 59 |
| 28h | CWGsPReg | defines the conductance of the p-driver output during periods of no modulation | Table 101 on page 60 |
| 29h | ModGsPReg | defines the conductance of the p-driver output during periods of modulation | Table 103 on page 60 |
| 2Ah | TModeReg | defines settings for the internal timer | Table 105 on page 60 |
| 2Bh | TPrescalerReg | | Table 107 on page 61 |
| 2Ch | TReloadReg | defines the 16-bit timer reload value | Table 109 on page 62 |
| 2Dh | | | Table 111 on page 62 |
| 2Eh | TCounterValReg | shows the 16-bit timer value | Table 113 on page 63 |
| 2Fh | | | Table 115 on page 63 |
| Page 3: Test register | | | |
| 30h | Reserved | reserved for future use | Table 117 on page 63 |
| 31h | TestSel1Reg | general test signal configuration | Table 119 on page 63 |
| 32h | TestSel2Reg | general test signal configuration and PRBS control | Table 121 on page 64 |
| 33h | TestPinEnReg | enables pin output driver on pins D1 to D7 | Table 123 on page 64 |
| 34h | TestPinValueReg | defines the values for D1 to D7 when it is used as an I/O bus | Table 125 on page 65 |
| 35h | TestBusReg | shows the status of the internal test bus | Table 127 on page 65 |
| 36h | AutoTestReg | controls the digital self test | Table 129 on page 66 |
| 37h | VersionReg | shows the software version | Table 131 on page 66 |
| 38h | AnalogTestReg | controls the pins AUX1 and AUX2 | Table 133 on page 67 |
| 39h | TestDAC1Reg | defines the test value for TestDAC1 | Table 135 on page 68 |
| 3Ah | TestDAC2Reg | defines the test value for TestDAC2 | Table 137 on page 68 |
| 3Bh | TestADCReg | shows the value of ADC I and Q channels | Table 139 on page 68 |
| 3Ch to 3Fh | Reserved | reserved for production tests | Table 141 to Table 147 on page 69 |

9.3 Register descriptions

9.3.1 Page 0: Command and status

9.3.1.1 Reserved register 00h

Functionality is reserved for future use.

Table 21. Reserved register (address 00h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 22. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|--------|-------------|
| 7 to 0 | - | reserved |

9.3.1.2 CommandReg register

Starts and stops command execution.

Table 23. CommandReg register (address 01h); reset value: 20h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|---|--------|-----------|--------------|---|---|---|
| Symbol: | reserved | | RcvOff | PowerDown | Command[3:0] | | | |
| Access: | - | | R/W | D | D | | | |

Table 24. CommandReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--------------|-------|--|
| 7 to 6 | reserved | - | reserved for future use |
| 5 | RcvOff | 1 | analog part of the receiver is switched off |
| 4 | PowerDown | 1 | Soft power-down mode entered |
| | | 0 | MFRC522 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the MFRC522 is ready; see Section 8.6.2 on page 33 Remark: The PowerDown bit cannot be set when the SoftReset command is activated |
| 3 to 0 | Command[3:0] | - | activates a command based on the Command value; reading this register shows which command is executed; see Section 10.3 on page 70 |

9.3.1.3 ComIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 25. ComIEnReg register (address 02h); reset value: 80h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|-------|-------|---------|------------|------------|--------|----------|
| Symbol | IRqInv | TxIEn | RxIEn | IdleIEn | HiAlertIEn | LoAlertIEn | ErrIEn | TimerIEn |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Table 26. ComIEnReg register bit descriptions

| Bit | Symbol | Value | Description |
|-----|------------|-------|---|
| 7 | IRqInv | 1 | signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit |
| | | 0 | signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state |
| 6 | TxIEn | - | allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ |
| 5 | RxIEn | - | allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ |
| 4 | IdleIEn | - | allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ |
| 3 | HiAlertIEn | - | allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ |
| 2 | LoAlertIEn | - | allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ |
| 1 | ErrIEn | - | allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ |
| 0 | TimerIEn | - | allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ |

9.3.1.4 DivIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 27. DivIEnReg register (address 03h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------------|----------|------------|----------|--------|----------|---|---|
| Symbol | IRQPushPull | reserved | MfinActIEn | reserved | CRCIEn | reserved | | |
| Access | R/W | - | R/W | - | R/W | - | | |

Table 28. DivIEnReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-------------|-------|---|
| 7 | IRQPushPull | 1 | pin IRQ is a standard CMOS output pin |
| | | 0 | pin IRQ is an open-drain output pin |
| 6 to 5 | reserved | - | reserved for future use |
| 4 | MfinActIEn | - | allows the MFIN active interrupt request to be propagated to pin IRQ |
| 3 | reserved | - | reserved for future use |
| 2 | CRCIEn | - | allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ |
| 1 to 0 | reserved | - | reserved for future use |

9.3.1.5 ComIrqReg register

Interrupt request bits.

Table 29. ComIrqReg register (address 04h); reset value: 14h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------|-------|-------|---------|------------|------------|--------|----------|
| Symbol | Set1 | TxIRq | RxIRq | IdleIRq | HiAlertIRq | LoAlertIRq | ErrIRq | TimerIRq |
| Access | W | D | D | D | D | D | D | D |

Table 30. ComIrqReg register bit descriptions

All bits in the ComIrqReg register are cleared by software.

| Bit | Symbol | Value | Description |
|-----|------------|-------|---|
| 7 | Set1 | 1 | indicates that the marked bits in the ComIrqReg register are set |
| | | 0 | indicates that the marked bits in the ComIrqReg register are cleared |
| 6 | TxIRq | 1 | set immediately after the last bit of the transmitted data was sent out |
| 5 | RxIRq | 1 | receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO |
| 4 | IdleIRq | 1 | If a command terminates, for example, when the CommandReg changes its value from any command to the Idle command (see Table 149 on page 70) if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set The microcontroller starting the Idle command does not set the IdleIRq bit |
| 3 | HiAlertIRq | 1 | the Status1Reg register's HiAlert bit is set in opposition to the HiAlert bit, the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register |
| 2 | LoAlertIRq | 1 | Status1Reg register's LoAlert bit is set in opposition to the LoAlert bit, the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register |
| 1 | ErrIRq | 1 | any error bit in the ErrorReg register is set |
| 0 | TimerIRq | 1 | the timer decrements the timer value in register TCounterValReg to zero |

9.3.1.6 DivIrqReg register

Interrupt request bits.

Table 31. DivIrqReg register (address 05h); reset value: x0h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------|----------|---|------------|----------|--------|----------|---|
| Symbol | Set2 | reserved | | MfinActIRq | reserved | CRCIRq | reserved | |
| Access | W | - | | D | - | D | - | |

Table 32. DivIrqReg register bit descriptions

All bits in the DivIrqReg register are cleared by software.

| Bit | Symbol | Value | Description |
|--------|------------|-------|---|
| 7 | Set2 | 1 | indicates that the marked bits in the DivIrqReg register are set |
| | | 0 | indicates that the marked bits in the DivIrqReg register are cleared |
| 6 to 5 | reserved | - | reserved for future use |
| 4 | MfinActIRq | 1 | MFIN is active this interrupt is set when either a rising or falling signal edge is detected |
| 3 | reserved | - | reserved for future use |
| 2 | CRCIRq | 1 | the CalcCRC command is active and all data is processed |
| 1 to 0 | reserved | - | reserved for future use |

9.3.1.7 ErrorReg register

Error bit register showing the error status of the last command executed.

Table 33. ErrorReg register (address 06h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------|---------|----------|------------|---------|--------|-----------|-------------|
| Symbol | WrErr | TempErr | reserved | BufferOvfl | CollErr | CRCErr | ParityErr | ProtocolErr |
| Access | R | R | - | R | R | R | R | R |

Table 34. ErrorReg register bit descriptions

| Bit | Symbol | Value | Description |
|-----|------------------------|-------|--|
| 7 | WrErr | 1 | data is written into the FIFO buffer by the host during the MFAuthent command or if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface |
| 6 | TempErr ^[1] | 1 | internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off |
| 5 | reserved | - | reserved for future use |
| 4 | BufferOvfl | 1 | the host or a MFRC522's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full |
| 3 | CollErr | 1 | a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd |
| 2 | CRCErr | 1 | the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase |
| 1 | ParityErr | 1 | parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A/MIFARE communication at 106 kBd |
| 0 | ProtocolErr | 1 | set to logic 1 if the SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd during the MFAuthent command, the ProtocolErr bit is set to logic 1 if the number of bytes received in one data stream is incorrect |

[1] Command execution clears all error bits except the TempErr bit. Cannot be set by software.

9.3.1.8 Status1Reg register

Contains status bits of the CRC, interrupt and FIFO buffer.

Table 35. Status1Reg register (address 07h); reset value: 21h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-------|----------|-----|----------|----------|---------|---------|
| Symbol | reserved | CRCOk | CRCReady | IRq | TRunning | reserved | HiAlert | LoAlert |
| Access | - | R | R | R | R | - | R | R |

Table 36. Status1Reg register bit descriptions

| Bit | Symbol | Value | Description |
|-----|----------|-------|--|
| 7 | reserved | - | reserved for future use |
| 6 | CRCOk | 1 | the CRC result is zero for data transmission and reception, the CRCOk bit is undefined: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1 |
| 5 | CRCReady | 1 | the CRC calculation has finished only valid for the CRC coprocessor calculation using the CalcCRC command |
| 4 | IRq | - | indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers |
| 3 | TRunning | 1 | MFRC522's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock Remark: in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal |
| 2 | reserved | - | reserved for future use |
| 1 | HiAlert | 1 | the number of bytes stored in the FIFO buffer corresponds to equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ example: FIFO length = 60, WaterLevel = 4 → HiAlert = 1 FIFO length = 59, WaterLevel = 4 → HiAlert = 0 |
| 0 | LoAlert | 1 | the number of bytes stored in the FIFO buffer corresponds to equation: $LoAlert = FIFOLength \leq WaterLevel$ example: FIFO length = 4, WaterLevel = 4 → LoAlert = 1 FIFO length = 5, WaterLevel = 4 → LoAlert = 0 |

9.3.1.9 Status2Reg register

Contains status bits of the receiver, transmitter and data mode detector.

Table 37. Status2Reg register (address 08h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|------------|----------|---|-------------|-----------------|---|---|
| Symbol | TempSensClear | I2CForceHS | reserved | | MFCrypto1On | ModemState[2:0] | | |
| Access | R/W | R/W | - | | D | R | | |

Table 38. Status2Reg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|---|
| 7 | TempSensClear | 1 | clears the temperature error if the temperature is below the alarm limit of 125 °C |
| 6 | I2CForceHS | | I2C-bus input filter settings: |
| | | 1 | the I2C-bus input filter is set to the High-speed mode independent of the I2C-bus protocol |
| | | 0 | the I2C-bus input filter is set to the I2C-bus protocol used |
| 5 to 4 | reserved | - | reserved |
| 3 | MFCrypto1On | - | indicates that the MIFARE Crypto1 unit is switched on and therefore all data communication with the card is encrypted can only be set to logic 1 by a successful execution of the MFAuthent command only valid in Read/Write mode for MIFARE standard cards this bit is cleared by software |
| 2 to 0 | ModemState[2:0] | - | shows the state of the transmitter and receiver state machines: |
| | | 000 | idle |
| | | 001 | wait for the BitFramingReg register's StartSend bit |
| | | 010 | TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for TxWait is defined by the TxWaitReg register |
| | | 011 | transmitting |
| | | 100 | RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for RxWait is defined by the RxWaitReg register |
| | | 101 | wait for data |
| 110 | receiving | | |

9.3.1.10 FIFODataReg register

Input and output of 64 byte FIFO buffer.

Table 39. FIFODataReg register (address 09h); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|---|---|---|---|---|---|---|
| Symbol | FIFOData[7:0] | | | | | | | |
| Access | D | | | | | | | |

Table 40. FIFODataReg register bit descriptions

| Bit | Symbol | Description |
|--------|---------------|---|
| 7 to 0 | FIFOData[7:0] | data input and output port for the internal 64-byte FIFO buffer FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs |

9.3.1.11 FIFOLevelReg register

Indicates the number of bytes stored in the FIFO.

Table 41. FIFOLevelReg register (address 0Ah); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------------|----------------|---|---|---|---|---|---|
| Symbol | FlushBuffer | FIFOLevel[6:0] | | | | | | |
| Access | W | R | | | | | | |

Table 42. FIFOLevelReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|--|
| 7 | FlushBuffer | 1 | immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit reading this bit always returns 0 |
| 6 to 0 | FIFOLevel [6:0] | - | indicates the number of bytes stored in the FIFO buffer writing to the FIFODataReg register increments and reading decrements the FIFOLevel value |

9.3.1.12 WaterLevelReg register

Defines the level for FIFO under- and overflow warning.

Table 43. WaterLevelReg register (address 0Bh); reset value: 08h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|-----------------|---|---|---|---|
| Symbol | reserved | | | WaterLevel[5:0] | | | | |
| Access | - | | | R/W | | | | |

Table 44. WaterLevelReg register bit descriptions

| Bit | Symbol | Description |
|--------|------------------|--|
| 7 to 6 | reserved | reserved for future use |
| 5 to 0 | WaterLevel [5:0] | <p>defines a warning level to indicate a FIFO buffer overflow or underflow:</p> <p>Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel bytes</p> <p>Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel bytes in the FIFO buffer</p> <p>Remark: to calculate values for HiAlert and LoAlert see Section 9.3.1.8 on page 42.</p> |

9.3.1.13 ControlReg register

Miscellaneous control bits.

Table 45. ControlReg register (address 0Ch); reset value: 10h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-----------|----------|---|---|-----------------|---|---|
| Symbol | TStopNow | TStartNow | reserved | | | RxLastBits[2:0] | | |
| Access | W | W | - | | | R | | |

Table 46. ControlReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|--|
| 7 | TStopNow | 1 | timer stops immediately reading this bit always returns it to logic0 |
| 6 | TStartNow | 1 | timer starts immediately reading this bit always returns it to logic 0 |
| 5 to 3 | reserved | - | reserved for future use |
| 2 to 0 | RxLastBits[2:0] | - | indicates the number of valid bits in the last received byte if this value is 000b, the whole byte is valid |

9.3.1.14 BitFramingReg register

Adjustments for bit-oriented frames.

Table 47. BitFramingReg register (address 0Dh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|--------------|---|---|----------|-----------------|---|---|
| Symbol | StartSend | RxAlign[2:0] | | | reserved | TxLastBits[2:0] | | |
| Access | W | R/W | | | - | R/W | | |

Table 48. BitFramingReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|--|
| 7 | StartSend | 1 | starts the transmission of data only valid in combination with the Transceive command |
| 6 to 4 | RxAlign[2:0] | | used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example: |
| | | 0 | LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1 |
| | | 1 | LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2 |
| | | 7 | LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0 These bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0 |
| 3 | reserved | - | reserved for future use |
| 2 to 0 | TxLastBits[2:0] | - | used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted 000b indicates that all bits of the last byte will be transmitted |

9.3.1.15 CollReg register

Defines the first bit-collision detected on the RF interface.

Table 49. CollReg register (address 0Eh); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------------|----------|-----------------|--------------|---|---|---|---|
| Symbol | ValuesAfterColl | reserved | CollPosNotValid | CollPos[4:0] | | | | |
| Access | R/W | - | R | R | | | | |

Table 50. CollReg register bit descriptions

| Bit | Symbol | Value | Description |
|-----|-----------------|-------|--|
| 7 | ValuesAfterColl | 0 | all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1 |
| 6 | reserved | - | reserved for future use |
| 5 | CollPosNotValid | 1 | no collision detected or the position of the collision is out of the range of CollPos[4:0] |

Table 50. CollReg register bit descriptions ...continued

| Bit | Symbol | Value | Description |
|--------|--------------|-------|--|
| 4 to 0 | CollPos[4:0] | - | shows the bit position of the first detected collision in a received frame only data bits are interpreted example: |
| | | 00h | indicates a bit-collision in the 32 nd bit |
| | | 01h | indicates a bit-collision in the 1 st bit |
| | | 08h | indicates a bit-collision in the 8 th bit These bits will only be interpreted if the CollPosNotValid bit is set to logic 0 |

9.3.1.16 Reserved register 0Fh

Functionality is reserved for future use.

Table 51. Reserved register (address 0Fh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 52. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.2 Page 1: Communication

9.3.2.1 Reserved register 10h

Functionality is reserved for future use.

Table 53. Reserved register (address 10h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 54. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.2.2 ModeReg register

Defines general mode settings for transmitting and receiving.

Table 55. ModeReg register (address 11h); reset value: 3Fh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|----------|----------|----------|---------|----------|----------------|---|
| Symbol | MSBFirst | reserved | TxWaitRF | reserved | PolMFin | reserved | CRCPreset[1:0] | |
| Access | R/W | - | R/W | - | R/W | - | R/W | |

Table 56. ModeReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|--|
| 7 | MSBFirst | 1 | CRC coprocessor calculates the CRC with MSB first in the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed Remark: during RF communication this bit is ignored |
| 6 | reserved | - | reserved for future use |
| 5 | TxWaitRF | 1 | transmitter can only be started if an RF field is generated |
| 4 | reserved | - | reserved for future use |
| 3 | PolMFin | | defines the polarity of pin MFIN Remark: the internal envelope signal is encoded active LOW, changing this bit generates a MFinActIRq event |
| | | 1 | polarity of pin MFIN is active HIGH |
| | | 0 | polarity of pin MFIN is active LOW |
| 2 | reserved | - | reserved for future use |
| 1 to 0 | CRCPreset [1:0] | | defines the preset value for the CRC coprocessor for the CalcCRC command Remark: during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers |
| | | 00 | 0000h |
| | | 01 | 6363h |
| | | 10 | A671h |
| | | 11 | FFFFh |

9.3.2.3 TxModeReg register

Defines the data rate during transmission.

Table 57. TxModeReg register (address 12h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|--------------|---|---|--------|----------|---|---|
| Symbol | TxCRCEn | TxSpeed[2:0] | | | InvMod | reserved | | |
| Access | R/W | D | | | R/W | - | | |

Table 58. TxModeReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--------------|-------|---|
| 7 | TxCRCEn | 1 | enables CRC generation during data transmission Remark: can only be set to logic 0 at 106 kBd |
| 6 to 4 | TxSpeed[2:0] | | defines the bit rate during data transmission the MFRC522 handles transfer speeds up to 848 kBd |
| | | 000 | 106 kBd |
| | | 001 | 212 kBd |
| | | 010 | 424 kBd |
| | | 011 | 848 kBd |
| | | 100 | reserved |
| | | 101 | reserved |
| | | 110 | reserved |
| 3 | InvMod | 1 | modulation of transmitted data is inverted |
| 2 to 0 | reserved | - | reserved for future use |

9.3.2.4 RxModeReg register

Defines the data rate during reception.

Table 59. RxModeReg register (address 13h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------|--------------|---|---|---------|------------|----------|---|
| Symbol | RxCRCEn | RxSpeed[2:0] | | | RxNoErr | RxMultiple | reserved | |
| Access | R/W | D | | | R/W | R/W | - | |

Table 60. RxModeReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--------------|-------|---|
| 7 | RxCRCEn | 1 | enables the CRC calculation during reception Remark: can only be set to logic 0 at 106 kBd |
| 6 to 4 | RxSpeed[2:0] | | defines the bit rate while receiving data the MFRC522 handles transfer speeds up to 848 kBd |
| | | 000 | 106 kBd |
| | | 001 | 212 kBd |
| | | 010 | 424 kBd |
| | | 011 | 848 kBd |
| | | 100 | reserved |
| | | 101 | reserved |
| | | 110 | reserved |
| 3 | RxNoErr | 1 | an invalid received data stream (less than 4 bits received) will be ignored and the receiver remains active |

Table 60. RxModeReg register bit descriptions ...continued

| Bit | Symbol | Value | Description |
|--------|------------|-------|---|
| 2 | RxMultiple | 0 | receiver is deactivated after receiving a data frame |
| | | 1 | able to receive more than one data frame only valid for data rates above 106 kBd in order to handle the polling command after setting this bit the Receive and Transceive commands will not terminate automatically. Multiple reception can only be deactivated by writing any command (except the Receive command) to the CommandReg register, or by the host clearing the bit if set to logic 1, an error byte is added to the FIFO buffer at the end of a received data stream which is a copy of the ErrorReg register value. For the MFRC522 version 2.0 the CRC status is reflected in the signal CRCOK, which indicates the actual status of the CRC coprocessor. For the MFRC522 version 1.0 the CRC status is reflected in the signal CRCErr. |
| 1 to 0 | reserved | - | reserved for future use |

9.3.2.5 TxControlReg register

Controls the logical behavior of the antenna driver pins TX1 and TX2.

Table 61. TxControlReg register (address 14h); reset value: 80h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------------|----------------|-----------------|-----------------|-------|----------|---------|---------|
| Symbol | InvTx2RF On | InvTx1RF On | InvTx2RF Off | InvTx1RF Off | Tx2CW | reserved | Tx2RFEn | Tx1RFEn |
| Access | R/W | R/W | R/W | R/W | R/W | - | R/W | R/W |

Table 62. TxControlReg register bit descriptions

| Bit | Symbol | Value | Description |
|-----|-------------|-------|---|
| 7 | InvTx2RFOn | 1 | output signal on pin TX2 inverted when driver TX2 is enabled |
| 6 | InvTx1RFOn | 1 | output signal on pin TX1 inverted when driver TX1 is enabled |
| 5 | InvTx2RFOff | 1 | output signal on pin TX2 inverted when driver TX2 is disabled |
| 4 | InvTx1RFOff | 1 | output signal on pin TX1 inverted when driver TX1 is disabled |
| 3 | Tx2CW | 1 | output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier |
| | | 0 | Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier |
| 2 | reserved | - | reserved for future use |
| 1 | Tx2RFEn | 1 | output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data |
| 0 | Tx1RFEn | 1 | output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data |

9.3.2.6 TxASKReg register

Controls transmit modulation settings.

Table 63. TxASKReg register (address 15h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-------------|----------|---|---|---|---|---|
| Symbol | reserved | Force100ASK | reserved | | | | | |
| Access | - | R/W | - | | | | | |

Table 64. TxASKReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-------------|-------|---|
| 7 | reserved | - | reserved for future use |
| 6 | Force100ASK | 1 | forces a 100 % ASK modulation independent of the ModGsPReg register setting |
| 5 to 0 | reserved | - | reserved for future use |

9.3.2.7 TxSelReg register

Selects the internal sources for the analog module.

Table 65. TxSelReg register (address 16h); reset value: 10h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|---|----------------|---|---------------|---|---|---|
| Symbol: | reserved | | DriverSel[1:0] | | MFOutSel[3:0] | | | |
| Access: | - | | R/W | | R/W | | | |

Table 66. TxSelReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|---|
| 7 to 6 | reserved | - | reserved for future use |
| 5 to 4 | DriverSel [1:0] | - | selects the input of drivers TX1 and TX2 |
| | | 00 | 3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode |
| | | 01 | modulation signal (envelope) from the internal encoder, Miller pulse encoded |
| | | 10 | modulation signal (envelope) from pin MFIN |
| | | 11 | HIGH; the HIGH level depends on the setting of bits InvTx1RFOOn/InvTx1RFOff and InvTx2RFOOn/InvTx2RFOff |

Table 66. TxSelReg register bit descriptions ...continued

| Bit | Symbol | Value | Description |
|--------------|----------------|----------|--|
| 3 to 0 | MFOutSel [3:0] | | selects the input for pin MFOUT |
| | | 0000 | 3-state |
| | | 0001 | LOW |
| | | 0010 | HIGH |
| | | 0011 | test bus signal as defined by the TestSel1Reg register's TstBusBitSel[2:0] value |
| | | 0100 | modulation signal (envelope) from the internal encoder, Miller pulse encoded |
| | | 0101 | serial data stream to be transmitted, data stream before Miller encoder |
| | | 0110 | reserved |
| | | 0111 | serial data stream received, data stream after Manchester decoder |
| 1000 to 1111 | | reserved | |

9.3.2.8 RxSelReg register

Selects internal receiver settings.

Table 67. RxSelReg register (address 17h); reset value: 84h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|---|---|-------------|---|---|---|---|
| Symbol | UARTSel[1:0] | | | RxWait[5:0] | | | | |
| Access | R/W | | | R/W | | | | |

Table 68. RxSelReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|---------------|-------|--|
| 7 to 6 | UARTSel [1:0] | 00 | selects the input of the contactless UART constant LOW |
| | | 01 | Manchester with subcarrier from pin MFIN |
| | | 10 | modulated signal from the internal analog module, default |
| | | 11 | NRZ coding without subcarrier from pin MFIN which is only valid for transfer speeds above 106 kBd |
| 5 to 0 | RxWait [5:0] | - | after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this 'frame guard time' any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive, MFAuthent use this parameter the counter starts immediately after the external RF field is switched on |

9.3.2.9 RxThresholdReg register

Selects thresholds for the bit decoder.

Table 69. RxThresholdReg register (address 18h); reset value: 84h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|---|---|---|----------|----------------|---|---|
| Symbol | MinLevel[3:0] | | | | reserved | CollLevel[2:0] | | |
| Access | R/W | | | | - | R/W | | |

Table 70. RxThresholdReg register bit descriptions

| Bit | Symbol | Description |
|--------|-----------------|--|
| 7 to 4 | MinLevel [3:0] | defines the minimum signal strength at the decoder input that will be accepted if the signal strength is below this level it is not evaluated |
| 3 | reserved | reserved for future use |
| 2 to 0 | CollLevel [2:0] | defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit |

9.3.2.10 DemodReg register

Defines demodulator settings.

Table 71. DemodReg register (address 19h); reset value: 4Dh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---|-------|---------------|-------------|---|--------------|---|
| Symbol | AddIQ[1:0] | | FixIQ | TPrescal Even | TauRcv[1:0] | | TauSync[1:0] | |
| Access | R/W | | R/W | R/W | R/W | | R/W | |

Table 72. DemodReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-------------|-------|--|
| 7 to 6 | AddIQ [1:0] | - | defines the use of I and Q channel during reception Remark: the FixIQ bit must be set to logic 0 to enable the following settings: |
| | | 00 | selects the stronger channel |
| | | 01 | selects the stronger channel and freezes the selected channel during communication |
| | | 10 | reserved |
| | | 11 | reserved |
| 5 | FixIQ | 1 | if AddIQ[1:0] are set to X0b, the reception is fixed to I channel if AddIQ[1:0] are set to X1b, the reception is fixed to Q channel |

Table 72. DemodReg register bit descriptions ...continued

| Bit | Symbol | Value | Description |
|--------|--------------|-------|---|
| 4 | TPrescalEven | R/W | Available on RC522 version 1.0 and version 2.0: If set to logic 0 the following formula is used to calculate the timer frequency of the prescaler: $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 1)$. Only available on version 2.0: If set to logic 1 the following formula is used to calculate the timer frequency of the prescaler: $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 2)$. Default TPrescalEven bit is logic 0, find more information on the prescaler in Section 8.5 . |
| 3 to 2 | TauRcv[1:0] | - | changes the time-constant of the internal PLL during data reception Remark: if set to 00b the PLL is frozen during data reception |
| 1 to 0 | TauSync[1:0] | - | changes the time-constant of the internal PLL during burst |

9.3.2.11 Reserved register 1Ah

Functionality is reserved for future use.

Table 73. Reserved register (address 1Ah); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 74. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.2.12 Reserved register 1Bh

Functionality is reserved for future use.

Table 75. Reserved register (address 1Bh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 76. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.2.13 MfTxReg register

Controls some MIFARE communication transmit parameters.

Table 77. MfTxReg register (address 1Ch); reset value: 62h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|-------------|---|
| Symbol | reserved | | | | | | TxWait[1:0] | |
| Access | - | | | | | | R/W | |

Table 78. MfTxReg register bit descriptions

| Bit | Symbol | Description |
|--------|----------|--|
| 7 to 2 | reserved | reserved for future use |
| 1 to 0 | TxWait | defines the additional response time 7 bits are added to the value of the register bit by default |

9.3.2.14 MfRxReg register

Table 79. MfRxReg register (address 1Dh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---------------|----------|---|---|---|
| Symbol | reserved | | | ParityDisable | reserved | | | |
| Access | - | | | R/W | - | | | |

Table 80. MfRxReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|---------------|-------|--|
| 7 to 5 | reserved | - | reserved for future use |
| 4 | ParityDisable | 1 | generation of the parity bit for transmission and the parity check for receiving is switched off the received parity bit is handled like a data bit |
| 3 to 0 | reserved | - | reserved for future use |

9.3.2.15 Reserved register 1Eh

Functionality is reserved for future use.

Table 81. Reserved register (address 1Eh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 82. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.2.16 SerialSpeedReg register

Selects the speed of the serial UART interface.

Table 83. SerialSpeedReg register (address 1Fh); reset value: EBh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---|---|---|------------|---|---|---|
| Symbol | BR_T0[2:0] | | | | BR_T1[4:0] | | | |
| Access | R/W | | | | R/W | | | |

Table 84. SerialSpeedReg register bit descriptions

| Bit | Symbol | Description |
|--------|------------|--|
| 7 to 5 | BR_T0[2:0] | factor BR_T0 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 12 |
| 4 to 0 | BR_T1[4:0] | factor BR_T1 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 12 |

9.3.3 Page 2: Configuration

9.3.3.1 Reserved register 20h

Functionality is reserved for future use.

Table 85. Reserved register (address 20h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | - | | | | | | | |
| Access | reserved | | | | | | | |

Table 86. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.3.2 CRCResultReg registers

Shows the MSB and LSB values of the CRC calculation.

Remark: The CRC is split into two 8-bit registers.

Table 87. CRCResultReg (higher bits) register (address 21h); reset value: FFh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------------------|---|---|---|---|---|---|---|
| Symbol | CRCResultMSB[7:0] | | | | | | | |
| Access | R | | | | | | | |

Table 88. CRCResultReg register higher bit descriptions

| Bit | Symbol | Description |
|--------|--------------------|--|
| 7 to 0 | CRCResultMSB [7:0] | shows the value of the CRCResultReg register's most significant byte only valid if Status1Reg register's CRCReady bit is set to logic 1 |

Table 89. CRCResultReg (lower bits) register (address 22h); reset value: FFh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------------------|---|---|---|---|---|---|---|
| Symbol | CRCResultLSB[7:0] | | | | | | | |
| Access | R | | | | | | | |

Table 90. CRCResultReg register lower bit descriptions

| Bit | Symbol | Description |
|--------|--------------------|--|
| 7 to 0 | CRCResultLSB [7:0] | shows the value of the least significant byte of the CRCResultReg register only valid if Status1Reg register's CRCReady bit is set to logic 1 |

9.3.3.3 Reserved register 23h

Functionality is reserved for future use.

Table 91. Reserved register (address 23h); reset value: 88h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 92. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.3.4 ModWidthReg register

Sets the modulation width.

Table 93. ModWidthReg register (address 24h); reset value: 26h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|---|---|---|---|---|---|---|
| Symbol | ModWidth[7:0] | | | | | | | |
| Access | R/W | | | | | | | |

Table 94. ModWidthReg register bit descriptions

| Bit | Symbol | Description |
|--------|---------------|---|
| 7 to 0 | ModWidth[7:0] | defines the width of the Miller modulation as multiples of the carrier frequency ($\text{ModWidth} + 1 / f_{\text{clk}}$) the maximum value is half the bit period |

9.3.3.5 Reserved register 25h

Functionality is reserved for future use.

Table 95. Reserved register (address 25h); reset value: 87h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 96. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.3.6 RFCfgReg register

Configures the receiver gain.

Table 97. RFCfgReg register (address 26h); reset value: 48h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-------------|---|---|----------|---|---|---|
| Symbol | reserved | RxGain[2:0] | | | reserved | | | |
| Access | - | R/W | | | - | | | |

Table 98. RFCfgReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--------------|-------|--|
| 7 | reserved | - | reserved for future use |
| 6 to 4 | RxGain [2:0] | | defines the receiver's signal voltage gain factor: |
| | | 000 | 18 dB |
| | | 001 | 23 dB |
| | | 010 | 18 dB |
| | | 011 | 23 dB |
| | | 100 | 33 dB |
| | | 101 | 38 dB |
| | | 110 | 43 dB |
| 111 | 48 dB | | |
| 3 to 0 | reserved | - | reserved for future use |

9.3.3.7 GsNReg register

Defines the conductance of the antenna driver pins TX1 and TX2 for the n-driver when the driver is switched on.

Table 99. GsNReg register (address 27h); reset value: 88h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---|---|---|-------------|---|---|---|
| Symbol | CWGsN[3:0] | | | | ModGsN[3:0] | | | |
| Access | R/W | | | | R/W | | | |

Table 100. GsNReg register bit descriptions

| Bit | Symbol | Description |
|--------|--------------|---|
| 7 to 4 | CWGsn [3:0] | <p>defines the conductance of the output n-driver during periods without modulation which can be used to regulate the output power and subsequently current consumption and operating distance</p> <p>Remark: the conductance value is binary-weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on</p> |
| 3 to 0 | ModGsN [3:0] | <p>defines the conductance of the output n-driver during periods without modulation which can be used to regulate the modulation index</p> <p>Remark: the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on</p> |

9.3.3.8 CWGsPReg register

Defines the conductance of the p-driver output during periods of no modulation.

Table 101. CWGsPReg register (address 28h); reset value: 20h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|------------|---|---|---|---|---|
| Symbol | reserved | | CWGsP[5:0] | | | | | |
| Access | - | | R/W | | | | | |

Table 102. CWGsPReg register bit descriptions

| Bit | Symbol | Description |
|--------|------------|---|
| 7 to 6 | reserved | reserved for future use |
| 5 to 0 | CWGsP[5:0] | defines the conductance of the p-driver output which can be used to regulate the output power and subsequently current consumption and operating distance Remark: the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 |

9.3.3.9 ModGsPReg register

Defines the conductance of the p-driver output during modulation.

Table 103. ModGsPReg register (address 29h); reset value: 20h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|-------------|---|---|---|---|---|
| Symbol | reserved | | ModGsP[5:0] | | | | | |
| Access | - | | R/W | | | | | |

Table 104. ModGsPReg register bit descriptions

| Bit | Symbol | Description |
|--------|-------------|--|
| 7 to 6 | reserved | reserved for future use |
| 5 to 0 | ModGsP[5:0] | defines the conductance of the p-driver output during modulation which can be used to regulate the modulation index Remark: the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 if the TxASKReg register's Force100ASK bit is set to logic 1 the value of ModGsP has no effect |

9.3.3.10 TModeReg and TPrescalerReg registers

These registers define the timer settings.

Remark: The TPrescaler setting higher 4 bits are in the TModeReg register and the lower 8 bits are in the TPrescalerReg register.

Table 105. TModeReg register (address 2Ah); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------|-------------|---|--------------|--------------------|---|---|---|
| Symbol | TAuto | TGated[1:0] | | TAutoRestart | TPrescaler_Hi[3:0] | | | |
| Access | R/W | R/W | | R/W | R/W | | | |

Table 106. TModeReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--------------------|-------|---|
| 7 | TAuto | 1 | timer starts automatically at the end of the transmission in all communication modes at all speeds if the RxModeReg register's RxMultiple bit is not set, the timer stops immediately after receiving the 5th bit (1 start bit, 4 data bits) if the RxMultiple bit is set to logic 1 the timer never stops, in which case the timer can be stopped by setting the ControlReg register's TStopNow bit to logic 1 |
| | | 0 | indicates that the timer is not influenced by the protocol |
| 6 to 5 | TGated[1:0] | | internal timer is running in gated mode Remark: in gated mode, the Status1Reg register's TRunning bit is logic 1 when the timer is enabled by the TModeReg register's TGated[1:0] bits this bit does not influence the gating signal |
| | | 00 | non-gated mode |
| | | 01 | gated by pin MFIN |
| | | 10 | gated by pin AUX1 |
| 4 | TAutoRestart | 1 | timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero |
| | | 0 | timer decrements to 0 and the ComlRqReg register's TimerlRq bit is set to logic 1 |
| 3 to 0 | TPrescaler_Hi[3:0] | - | defines the higher 4 bits of the TPrescaler value The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit in Demot Regis set to logic 0: $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 1).$ Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0) The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 1: $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 2).$ See Section 8.5 "Timer unit" . |

Table 107. TPrescalerReg register (address 2Bh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------------|---|---|---|---|---|---|---|
| Symbol | TPrescaler_Lo[7:0] | | | | | | | |
| Access | R/W | | | | | | | |

Table 108. TPrescalerReg register bit descriptions

| Bit | Symbol | Description |
|--------|--------------------|---|
| 7 to 0 | TPrescaler_Lo[7:0] | <p>defines the lower 8 bits of the TPrescaler value</p> <p>The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 0:</p> $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 1).$ <p>Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0)</p> <p>The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit in DemoReg is set to logic 1:</p> $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 2).$ <p>See Section 8.5 "Timer unit".</p> |

9.3.3.11 TReloadReg register

Defines the 16-bit timer reload value.

Remark: The reload value bits are contained in two 8-bit registers.

Table 109. TReloadReg (higher bits) register (address 2Ch); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------------|---|---|---|---|---|---|---|
| Symbol | TReloadVal_Hi[7:0] | | | | | | | |
| Access | R/W | | | | | | | |

Table 110. TReloadReg register higher bit descriptions

| Bit | Symbol | Description |
|--------|--------------------|--|
| 7 to 0 | TReloadVal_Hi[7:0] | <p>defines the higher 8 bits of the 16-bit timer reload value</p> <p>on a start event, the timer loads the timer reload value</p> <p>changing this register affects the timer only at the next start event</p> |

Table 111. TReloadReg (lower bits) register (address 2Dh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------------|---|---|---|---|---|---|---|
| Symbol | TReloadVal_Lo[7:0] | | | | | | | |
| Access | R/W | | | | | | | |

Table 112. TReloadReg register lower bit descriptions

| Bit | Symbol | Description |
|--------|--------------------|---|
| 7 to 0 | TReloadVal_Lo[7:0] | <p>defines the lower 8 bits of the 16-bit timer reload value</p> <p>on a start event, the timer loads the timer reload value</p> <p>changing this register affects the timer only at the next start event</p> |

9.3.3.12 TCounterValReg register

Contains the timer value.

Remark: The timer value bits are contained in two 8-bit registers.

Table 113. TCounterValReg (higher bits) register (address 2Eh); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------------|---|---|---|---|---|---|---|
| Symbol | TCounterVal_Hi[7:0] | | | | | | | |
| Access | R | | | | | | | |

Table 114. TCounterValReg register higher bit descriptions

| Bit | Symbol | Description |
|--------|----------------------|---------------------------|
| 7 to 0 | TCounterVal_Hi [7:0] | timer value higher 8 bits |

Table 115. TCounterValReg (lower bits) register (address 2Fh); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------------|---|---|---|---|---|---|---|
| Symbol | TCounterVal_Lo[7:0] | | | | | | | |
| Access | R | | | | | | | |

Table 116. TCounterValReg register lower bit descriptions

| Bit | Symbol | Description |
|--------|----------------------|--------------------------|
| 7 to 0 | TCounterVal_Lo [7:0] | timer value lower 8 bits |

9.3.4 Page 3: Test

9.3.4.1 Reserved register 30h

Functionality is reserved for future use.

Table 117. Reserved register (address 30h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 118. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------|
| 7 to 0 | reserved | reserved for future use |

9.3.4.2 TestSel1Reg register

General test signal configuration.

Table 119. TestSel1Reg register (address 31h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|-------------------|---|---|
| Symbol | reserved | | | | | TstBusBitSel[2:0] | | |
| Access | - | | | | | R/W | | |

Table 120. TestSel1Reg register bit descriptions

| Bit | Symbol | Description |
|--------|--------------------|--|
| 7 to 3 | reserved | reserved for future use |
| 2 to 0 | TstBusBitSel [2:0] | selects a test bus signal which is output at pin MFOUT if AnalogSelAux2[3:0] = FFh in AnalogTestReg register, test bus signal is also output at pins AUX1 or AUX2 |

9.3.4.3 TestSel2Reg register

General test signal configuration and PRBS control.

Table 121. TestSel2Reg register (address 32h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|-------|--------|-----------------|---|---|---|---|
| Symbol | TstBusFlip | PRBS9 | PRBS15 | TestBusSel[4:0] | | | | |
| Access | R/W | R/W | R/W | R/W | | | | |

Table 122. TestSel2Reg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|--|
| 7 | TstBusFlip | 1 | test bus is mapped to the parallel port in the following order: TstBusBit4, TstBusBit3, TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0; see Section 16.1 on page 82 |
| 6 | PRBS9 | - | starts and enables the PRBS9 sequence according to ITU-TO150 Remark: all relevant registers to transmit data must be configured before entering PRBS9 mode the data transmission of the defined sequence is started by the Transmit command |
| 5 | PRBS15 | - | starts and enables the PRBS15 sequence according to ITU-TO150 Remark: all relevant registers to transmit data must be configured before entering PRBS15 mode the data transmission of the defined sequence is started by the Transmit command |
| 4 to 0 | TestBusSel[4:0] | - | selects the test bus; see Section 16.1 "Test signals" |

9.3.4.4 TestPinEnReg register

Enables the test bus pin output driver.

Table 123. TestPinEnReg register (address 33h); reset value: 80h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------------|----------------|---|---|---|---|---|----------|
| Symbol | RS232LineEn | TestPinEn[5:0] | | | | | | reserved |
| Access | R/W | R/W | | | | | | - |

Table 124. TestPinEnReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|-----------------|-------|--|
| 7 | RS232LineEn | 0 | serial UART lines MX and DTRQ are disabled |
| 6 to 1 | TestPinEn [5:0] | - | enables the output driver on one of the data pins D1 to D7 which outputs a test signal Example: setting bit 1 to logic 1 enables pin D1 output setting bit 5 to logic 1 enables pin D5 output Remark: If the SPI is used, only pins D1 to D4 can be used. If the serial UART interface is used and the RS232LineEn bit is set to logic 1 only pins D1 to D4 can be used. |
| 0 | reserved | - | reserved for future use |

9.3.4.5 TestPinValueReg register

Defines the HIGH and LOW values for the test port D1 to D7 when it is used as I/O.

Table 125. TestPinValueReg register (address 34h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------|-------------------|---|---|---|---|---|----------|
| Symbol | UseIO | TestPinValue[5:0] | | | | | | reserved |
| Access | R/W | R/W | | | | | | - |

Table 126. TestPinValueReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--------------------|-------|---|
| 7 | UseIO | 1 | enables the I/O functionality for the test port when one of the serial interfaces is used the input/output behavior is defined by value TestPinEn[5:0] in the TestPinEnReg register the value for the output behavior is defined by TestPinValue[5:0] |
| 6 to 1 | TestPinValue [5:0] | - | defines the value of the test port when it is used as I/O and each output must be enabled by TestPinEn[5:0] in the TestPinEnReg register Remark: Reading the register indicates the status of pins D6 to D1 if the UseIO bit is set to logic 1. If the UseIO bit is set to logic 0, the value of the TestPinValueReg register is read back. |
| 0 | reserved | - | reserved for future use |

9.3.4.6 TestBusReg register

Shows the status of the internal test bus.

Table 127. TestBusReg register (address 35h); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|---|---|---|---|---|---|---|
| Symbol | TestBus[7:0] | | | | | | | |
| Access | R | | | | | | | |

Table 128. TestBusReg register bit descriptions

| Bit | Symbol | Description |
|--------|--------------|---|
| 7 to 0 | TestBus[7:0] | shows the status of the internal test bus the test bus is selected using the TestSel2Reg register; see Section 16.1 on page 82 |

9.3.4.7 AutoTestReg register

Controls the digital self-test.

Table 129. AutoTestReg register (address 36h); reset value: 40h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|--------|-----|---|---------------|---|---|---|
| Symbol | reserved | AmpRcv | RFT | | SelfTest[3:0] | | | |
| Access | - | R/W | - | | R/W | | | |

Table 130. AutoTestReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|---------------|-------|--|
| 7 | reserved | - | reserved for production tests |
| 6 | AmpRcv | 1 | internal signal processing in the receiver chain is performed non-linearly which increases the operating distance in communication modes at 106 kBd Remark: due to non-linearity, the effect of the RxThresholdReg register's MinLevel[3:0] and the CollLevel[2:0] values is also non-linear |
| 5 to 4 | RFT | - | reserved for production tests |
| 3 to 0 | SelfTest[3:0] | - | enables the digital self test the self test can also be started by the CalcCRC command; see Section 10.3.1.4 on page 71 the self test is enabled by value 1001b Remark: for default operation the self test must be disabled by value 0000b |

9.3.4.8 VersionReg register

Shows the MFRC522 software version.

Table 131. VersionReg register (address 37h); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|---|---|---|---|---|---|---|
| Symbol | Version[7:0] | | | | | | | |
| Access | R | | | | | | | |

Table 132. VersionReg register bit descriptions

| Bit | Symbol | Description |
|--------|----------|--|
| 7 to 4 | Chiptype | '9' stands for MFRC522 |
| 3 to 0 | Version | '1' stands for MFRC522 version 1.0 and '2' stands for MFRC522 version 2.0. |

MFRC522 version 1.0 software version is: 91h.

MFRC522 version 2.0 software version is: 92h.

9.3.4.9 AnalogTestReg register

Determines the analog output test signal at, and status of, pins AUX1 and AUX2.

Table 133. AnalogTestReg register (address 38h); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------------|---|---|---|--------------------|---|---|---|
| Symbol | AnalogSelAux1[3:0] | | | | AnalogSelAux2[3:0] | | | |
| Access | R/W | | | | R/W | | | |

Table 134. AnalogTestReg register bit descriptions

| Bit | Symbol | Value | Description |
|--------|--|-------|---|
| 7 to 4 | AnalogSelAux1 [3:0] | | controls pin AUX1 |
| | | 0000 | 3-state |
| | | 0001 | output of TestDAC1 (AUX1), output of TestDAC2 (AUX2) ^[1] |
| | | 0010 | test signal Corr1 ^[1] |
| | | 0011 | reserved |
| | | 0100 | DAC: test signal MinLevel ^[1] |
| | | 0101 | DAC: test signal ADC_I ^[1] |
| | | 0110 | DAC: test signal ADC_Q ^[1] |
| | | 0111 | reserved |
| | | 1000 | reserved, test signal for production test ^[1] |
| | | 1001 | reserved |
| | | 1010 | HIGH |
| | | 1011 | LOW |
| | | 1100 | TxActive: at 106 kBd: HIGH during Start bit, Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC |
| 1101 | RxActive: at 106 kBd: HIGH during Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC | | |
| 1110 | subcarrier detected: 106 kBd: not applicable 212 kBd: 424 kBd and 848 kBd: HIGH during last part of data and CRC | | |
| 1111 | test bus bit as defined by the TestSel1Reg register's TstBusBitSel[2:0] bits Remark: all test signals are described in Section 16.1 on page 82 | | |
| 3 to 0 | AnalogSelAux2 [3:0] | - | controls pin AUX2 (see bit descriptions for AUX1) |

[1] **Remark:** Current source output; the use of 1 kΩ pull-down resistor on AUXn is recommended.

9.3.4.10 TestDAC1Reg register

Defines the test value for TestDAC1.

Table 135. TestDAC1Reg register (address 39h); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---------------|---|---|---|---|---|
| Symbol | reserved | | TestDAC1[5:0] | | | | | |
| Access | - | | R/W | | | | | |

Table 136. TestDAC1Reg register bit descriptions

| Bit | Symbol | Description |
|--------|---------------|--|
| 7 | reserved | reserved for production tests |
| 6 | reserved | reserved for future use |
| 5 to 0 | TestDAC1[5:0] | defines the test value for TestDAC1 output of DAC1 can be routed to AUX1 by setting value AnalogSelAux1[3:0] to 0001b in the AnalogTestReg register |

9.3.4.11 TestDAC2Reg register

Defines the test value for TestDAC2.

Table 137. TestDAC2Reg register (address 3Ah); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---------------|---|---|---|---|---|
| Symbol | reserved | | TestDAC2[5:0] | | | | | |
| Access | - | | R/W | | | | | |

Table 138. TestDAC2Reg register bit descriptions

| Bit | Symbol | Description |
|--------|---------------|--|
| 7 to 6 | reserved | reserved for future use |
| 5 to 0 | TestDAC2[5:0] | defines the test value for TestDAC2 output of DAC2 can be routed to AUX2 by setting value AnalogSelAux2[3:0] to 0001b in the AnalogTestReg register |

9.3.4.12 TestADCReg register

Shows the values of ADC I and Q channels.

Table 139. TestADCReg register (address 3Bh); reset value: xxh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---|---|---|------------|---|---|---|
| Symbol | ADC_I[3:0] | | | | ADC_Q[3:0] | | | |
| Access | R | | | | R | | | |

Table 140. TestADCReg register bit descriptions

| Bit | Symbol | Description |
|--------|------------|---------------------|
| 7 to 4 | ADC_I[3:0] | ADC I channel value |
| 3 to 0 | ADC_Q[3:0] | ADC Q channel value |

9.3.4.13 Reserved register 3Ch

Functionality reserved for production test.

Table 141. Reserved register (address 3Ch); reset value: FFh bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----|---|---|---|---|---|---|---|
| Symbol | RFT | | | | | | | |
| Access | - | | | | | | | |

Table 142. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------------|
| 7 to 0 | reserved | reserved for production tests |

Table 143. Reserved register (address 3Dh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----|---|---|---|---|---|---|---|
| Symbol | RFT | | | | | | | |
| Access | - | | | | | | | |

Table 144. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------------|
| 7 to 0 | reserved | reserved for production tests |

Table 145. Reserved register (address 3Eh); reset value: 03h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----|---|---|---|---|---|---|---|
| Symbol | RFT | | | | | | | |
| Access | - | | | | | | | |

Table 146. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------------|
| 7 to 0 | reserved | reserved for production tests |

Table 147. Reserved register (address 3Fh); reset value: 00h bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---|---|---|---|---|---|---|
| Symbol | reserved | | | | | | | |
| Access | - | | | | | | | |

Table 148. Reserved register bit descriptions

| Bit | Symbol | Description |
|--------|----------|-------------------------------|
| 7 to 0 | reserved | reserved for production tests |

10. MFRC522 command set

10.1 General description

The MFRC522 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see [Table 149](#)) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

10.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

10.3 MFRC522 command overview

Table 149. Command overview

| Command | Command code | Action |
|-------------------|--------------|---|
| Idle | 0000 | no action, cancels current command execution |
| Mem | 0001 | stores 25 bytes into the internal buffer |
| Generate RandomID | 0010 | generates a 10-byte random ID number |
| CalcCRC | 0011 | activates the CRC coprocessor or performs a self test |
| Transmit | 0100 | transmits data from the FIFO buffer |
| NoCmdChange | 0111 | no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit |
| Receive | 1000 | activates the receiver circuits |
| Transceive | 1100 | transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission |
| - | 1101 | reserved for future use |
| MFAuthent | 1110 | performs the MIFARE standard authentication as a reader |
| SoftReset | 1111 | resets the MFRC522 |

10.3.1 MFRC522 command descriptions

10.3.1.1 Idle

Places the MFRC522 in Idle mode. The Idle command also terminates itself.

10.3.1.2 Mem

Transfers 25 bytes from the FIFO buffer to the internal buffer.

To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power-down (using pin NRSTPD), the 25 bytes in the internal buffer remain unchanged and are only lost if the power supply is removed from the MFRC522.

This command automatically terminates when finished and the Idle command becomes active.

10.3.1.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the MFRC522 returns to Idle mode.

10.3.1.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the MFRC522 enters Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

10.3.1.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

10.3.1.6 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

10.3.1.7 Receive

The MFRC522 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

10.3.1.8 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

10.3.1.9 MFAuthent

This command manages MIFARE authentication to enable a secure communication to any MIFARE Mini, MIFARE 1K and MIFARE 4K card. The following data is written to the FIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes are written to the FIFO.

Remark: When the MFAuthent command is active all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.

This command automatically terminates when the MIFARE card is authenticated and the Status2Reg register's MFCrypto1On bit is set to logic 1.

This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, the TimerIRq bit can be used as the termination criteria. During authentication processing, the RxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination of the MFAuthent command, either after processing the protocol or writing Idle to the CommandReg register.

If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set to logic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

10.3.1.10 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

Remark: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

11. Limiting values

Table 150. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------|---------------------------------|--|-----------------------------|-----------------------------|------|
| V _{DDA} | analog supply voltage | | -0.5 | +4.0 | V |
| V _{DDD} | digital supply voltage | | -0.5 | +4.0 | V |
| V _{DD(PVDD)} | PVDD supply voltage | | -0.5 | +4.0 | V |
| V _{DD(TVDD)} | TVDD supply voltage | | -0.5 | +4.0 | V |
| V _{DD(SVDD)} | SVDD supply voltage | | -0.5 | +4.0 | V |
| V _i | input voltage | all input pins except pins MFIN and RX | V _{SS(PVSS)} - 0.5 | V _{DD(PVDD)} + 0.5 | V |
| | | pin MFIN | V _{SS(PVSS)} - 0.5 | V _{DD(SVDD)} + 0.5 | V |
| P _{tot} | total power dissipation | per package; and V _{DDD} in shortcut mode | - | 200 | mW |
| T _j | junction temperature | | - | 100 | °C |
| V _{ESD} | electrostatic discharge voltage | HBM; 1500 Ω, 100 pF; JESD22-A114-B | - | 2000 | V |
| | | MM; 0.75 μH, 200 pF; JESD22-A114-A | - | 200 | V |
| | | Charged device model; JESD22-C101-A | | | |
| | | on all pins | - | 200 | V |
| | | on all pins except SVDD in TFBGA64 package | - | 500 | V |

12. Recommended operating conditions

Table 151. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|------------------------|--|------------|-----|-----|------|
| V _{DDA} | analog supply voltage | V _{DD(PVDD)} ≤ V _{DDA} = V _{DDD} = V _{DD(TVDD)} ; V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | [1][2] 2.5 | 3.3 | 3.6 | V |
| V _{DDD} | digital supply voltage | V _{DD(PVDD)} ≤ V _{DDA} = V _{DDD} = V _{DD(TVDD)} ; V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | [1][2] 2.5 | 3.3 | 3.6 | V |
| V _{DD(TVDD)} | TVDD supply voltage | V _{DD(PVDD)} ≤ V _{DDA} = V _{DDD} = V _{DD(TVDD)} ; V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | [1][2] 2.5 | 3.3 | 3.6 | V |
| V _{DD(PVDD)} | PVDD supply voltage | V _{DD(PVDD)} ≤ V _{DDA} = V _{DDD} = V _{DD(TVDD)} ; V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | [3] 1.6 | 1.8 | 3.6 | V |
| V _{DD(SVDD)} | SVDD supply voltage | V _{SSA} = V _{SSD} = V _{SS(PVSS)} = V _{SS(TVSS)} = 0 V | 1.6 | - | 3.6 | V |
| T _{amb} | ambient temperature | HVQFN32 | -25 | - | +85 | °C |

[1] Supply voltages below 3 V reduce the performance (the achievable operating distance).

[2] V_{DDA}, V_{DDD} and V_{DD(TVDD)} must always be the same voltage.

[3] V_{DD(PVDD)} must always be the same or lower voltage than V_{DDD}.

13. Thermal characteristics

Table 152. Thermal characteristics

| Symbol | Parameter | Conditions | Package | Typ | Unit |
|---------------|---|---|---------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in still air with exposed pin soldered on a 4 layer JEDEC PCB | HVQFN32 | 40 | K/W |

14. Characteristics

Table 153. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------------------------------|---|-------------------|-----|-------------------|----------|
| Input characteristics | | | | | | |
| Pins EA, I2C and NRSTPD | | | | | | |
| I_{LI} | input leakage current | | -1 | - | +1 | μA |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(PVDD)}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DD(PVDD)}$ | V |
| Pin MFIN | | | | | | |
| I_{LI} | input leakage current | | -1 | - | +1 | μA |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(SVDD)}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DD(SVDD)}$ | V |
| Pin SDA | | | | | | |
| I_{LI} | input leakage current | | -1 | - | +1 | μA |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(PVDD)}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DD(PVDD)}$ | V |
| Pin RX ^[1] | | | | | | |
| V_i | input voltage | | -1 | - | $V_{DDA} + 1$ | V |
| C_i | input capacitance | $V_{DDA} = 3 V$; receiver active; $V_{RX(p-p)} = 1 V$; 1.5 V (DC) offset | - | 10 | - | pF |
| R_i | input resistance | $V_{DDA} = 3 V$; receiver active; $V_{RX(p-p)} = 1 V$; 1.5 V (DC) offset | - | 350 | - | Ω |
| <i>Input voltage range; see Figure 24</i> | | | | | | |
| $V_{i(p-p)(min)}$ | minimum peak-to-peak input voltage | Manchester encoded; $V_{DDA} = 3 V$ | - | 100 | - | mV |
| $V_{i(p-p)(max)}$ | maximum peak-to-peak input voltage | Manchester encoded; $V_{DDA} = 3 V$ | - | 4 | - | V |
| <i>Input sensitivity; see Figure 24</i> | | | | | | |
| V_{mod} | modulation voltage | minimum Manchester encoded; $V_{DDA} = 3 V$; $RxGain[2:0] = 111b$ (48 dB) | - | 5 | - | mV |
| Pin OSCIN | | | | | | |
| I_{LI} | input leakage current | | -1 | - | +1 | μA |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDA}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DDA}$ | V |

Table 153. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---------------------------|--|-----------------------------|-----|-----------------------------|------|
| C _i | input capacitance | V _{DDA} = 2.8 V; DC = 0.65 V; AC = 1 V (p-p) | - | 2 | - | pF |
| Input/output characteristics | | | | | | |
| pins D1, D2, D3, D4, D5, D6 and D7 | | | | | | |
| I _{LI} | input leakage current | | -1 | - | +1 | μA |
| V _{IH} | HIGH-level input voltage | | 0.7V _{DD(PVDD)} | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{DD(PVDD)} | V |
| V _{OH} | HIGH-level output voltage | V _{DD(PVDD)} = 3 V; I _O = 4 mA | V _{DD(PVDD)} - 0.4 | - | V _{DD(PVDD)} | V |
| V _{OL} | LOW-level output voltage | V _{DD(PVDD)} = 3 V; I _O = 4 mA | V _{SS(PVSS)} | - | V _{SS(PVSS)} + 0.4 | V |
| I _{OH} | HIGH-level output current | V _{DD(PVDD)} = 3 V | - | - | 4 | mA |
| I _{OL} | LOW-level output current | V _{DD(PVDD)} = 3 V | - | - | 4 | mA |
| Output characteristics | | | | | | |
| Pin MFOUT | | | | | | |
| V _{OH} | HIGH-level output voltage | V _{DD(SVDD)} = 3 V; I _O = 4 mA | V _{DD(SVDD)} - 0.4 | - | V _{DD(SVDD)} | V |
| V _{OL} | LOW-level output voltage | V _{DD(SVDD)} = 3 V; I _O = 4 mA | V _{SS(PVSS)} | - | V _{SS(PVSS)} + 0.4 | V |
| I _{OL} | LOW-level output current | V _{DD(SVDD)} = 3 V | - | - | 4 | mA |
| I _{OH} | HIGH-level output current | V _{DD(SVDD)} = 3 V | - | - | 4 | mA |
| Pin IRQ | | | | | | |
| V _{OH} | HIGH-level output voltage | V _{DD(PVDD)} = 3 V; I _O = 4 mA | V _{DD(PVDD)} - 0.4 | - | V _{DD(PVDD)} | V |
| V _{OL} | LOW-level output voltage | V _{DD(PVDD)} = 3 V; I _O = 4 mA | V _{SS(PVSS)} | - | V _{SS(PVSS)} + 0.4 | V |
| I _{OL} | LOW-level output current | V _{DD(PVDD)} = 3 V | - | - | 4 | mA |
| I _{OH} | HIGH-level output current | V _{DD(PVDD)} = 3 V | - | - | 4 | mA |
| Pins AUX1 and AUX2 | | | | | | |
| V _{OH} | HIGH-level output voltage | V _{DDD} = 3 V; I _O = 4 mA | V _{DDD} - 0.4 | - | V _{DDD} | V |
| V _{OL} | LOW-level output voltage | V _{DDD} = 3 V; I _O = 4 mA | V _{SS(PVSS)} | - | V _{SS(PVSS)} + 0.4 | V |
| I _{OL} | LOW-level output current | V _{DDD} = 3 V | - | - | 4 | mA |
| I _{OH} | HIGH-level output current | V _{DDD} = 3 V | - | - | 4 | mA |
| Pins TX1 and TX2 | | | | | | |

Table 153. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|----------------------------|---------------------------|---|------------------------------|-------|------|------|----|
| V _{OH} | HIGH-level output voltage | V _{DD(TVDD)} = 3 V; I _{DD(TVDD)} = 32 mA; CWGsP[5:0] = 3Fh | V _{DD(TVDD)} - 0.15 | - | - | V | |
| | | V _{DD(TVDD)} = 3 V; I _{DD(TVDD)} = 80 mA; CWGsP[5:0] = 3Fh | V _{DD(TVDD)} - 0.4 | - | - | V | |
| | | V _{DD(TVDD)} = 2.5 V; I _{DD(TVDD)} = 32 mA; CWGsP[5:0] = 3Fh | V _{DD(TVDD)} - 0.24 | - | - | V | |
| | | V _{DD(TVDD)} = 2.5 V; I _{DD(TVDD)} = 80 mA; CWGsP[5:0] = 3Fh | V _{DD(TVDD)} - 0.64 | - | - | V | |
| V _{OL} | LOW-level output voltage | V _{DD(TVDD)} = 3 V; I _{DD(TVDD)} = 32 mA; CWGsP[5:0] = 0Fh | - | - | 0.15 | V | |
| | | V _{DD(TVDD)} = 3 V; I _{DD(TVDD)} = 80 mA; CWGsP[5:0] = 0Fh | - | - | 0.4 | V | |
| | | V _{DD(TVDD)} = 2.5 V; I _{DD(TVDD)} = 32 mA; CWGsP[5:0] = 0Fh | - | - | 0.24 | V | |
| | | V _{DD(TVDD)} = 2.5 V; I _{DD(TVDD)} = 80 mA; CWGsP[5:0] = 0Fh | - | - | 0.64 | V | |
| Current consumption | | | | | | | |
| I _{pd} | power-down current | V _{DDA} = V _{DDD} = V _{DD(TVDD)} = V _{DD(PVDD)} = 3 V | | | | | |
| | | hard power-down; pin NRSTPD set LOW | [2] | - | 5 | μA | |
| | | soft power-down; RF level detector on | [2] | - | 10 | μA | |
| I _{DDD} | digital supply current | pin DVDD; V _{DDD} = 3 V | - | 6.5 | 9 | mA | |
| I _{DDA} | analog supply current | pin AVDD; V _{DDA} = 3 V; CommandReg register's bit RcvOff = 0 | - | 7 | 10 | mA | |
| | | pin AVDD; receiver switched off; V _{DDA} = 3 V; CommandReg register's bit RcvOff = 1 | - | 3 | 5 | mA | |
| I _{DD(PVDD)} | PVDD supply current | pin PVDD | [3] | - | 40 | mA | |
| I _{DD(TVDD)} | TVDD supply current | pin TVDD; continuous wave | [4][5][6] | - | 60 | 100 | mA |
| I _{DD(SVDD)} | SVDD supply current | pin SVDD | [7] | - | 4 | mA | |
| Clock frequency | | | | | | | |
| f _{clk} | clock frequency | | - | 27.12 | - | MHz | |
| δ _{clk} | clock duty cycle | | 40 | 50 | 60 | % | |
| t _{jit} | jitter time | RMS | - | - | 10 | ps | |
| Crystal oscillator | | | | | | | |

Table 153. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|------------------------------|------------|-----|-------|-----|------|
| V _{OH} | HIGH-level output voltage | pin OSCOUT | - | 1.1 | - | V |
| V _{OL} | LOW-level output voltage | pin OSCOUT | - | 0.2 | - | V |
| C _i | input capacitance | pin OSCOUT | - | 2 | - | pF |
| | | pin OSCIN | - | 2 | - | pF |
| Typical input requirements | | | | | | |
| f _{xtal} | crystal frequency | | - | 27.12 | - | MHz |
| ESR | equivalent series resistance | | - | - | 100 | Ω |
| C _L | load capacitance | | - | 10 | - | pF |
| P _{xtal} | crystal power dissipation | | - | 50 | 100 | mW |

- [1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.
- [2] I_{pd} is the total current for all supplies.
- [3] I_{DD(PVDD)} depends on the overall load at the digital pins.
- [4] I_{DD(TVDD)} depends on V_{DD(TVDD)} and the external circuit connected to pins TX1 and TX2.
- [5] During typical circuit operation, the overall current is below 100 mA.
- [6] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.
- [7] I_{DD(SVDD)} depends on the load at pin MFOUT.



Fig 24. Pin RX input voltage range

14.1 Timing characteristics

Table 154. SPI timing characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------------|----------------------|-----|-----|-----|------|
| t _{WL} | pulse width LOW | line SCK | 50 | - | - | ns |
| t _{WH} | pulse width HIGH | line SCK | 50 | - | - | ns |
| t _{h(SCKH-D)} | SCK HIGH to data input hold time | SCK to changing MOSI | 25 | - | - | ns |

Table 154. SPI timing characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------------------|----------------------|-----|-----|-----|------|
| $t_{su(D-SCKH)}$ | data input to SCK HIGH set-up time | changing MOSI to SCK | 25 | - | - | ns |
| $t_{h(SCKL-Q)}$ | SCK LOW to data output hold time | SCK to changing MISO | - | - | 25 | ns |
| $t_{(SCKL-NSSH)}$ | SCK LOW to NSS HIGH time | | 0 | - | - | ns |
| t_{NHNL} | NSS high before communication | | 50 | - | - | ns |

Table 155. I²C-bus timing in Fast mode

| Symbol | Parameter | Conditions | Fast mode | | High-speed mode | | Unit |
|--------------|--|---|-----------|-----|-----------------|------|------|
| | | | Min | Max | Min | Max | |
| f_{SCL} | SCL clock frequency | | 0 | 400 | 0 | 3400 | kHz |
| $t_{HD;STA}$ | hold time (repeated) START condition | after this period, the first clock pulse is generated | 600 | - | 160 | - | ns |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 600 | - | 160 | - | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | 600 | - | 160 | - | ns |
| t_{LOW} | LOW period of the SCL clock | | 1300 | - | 160 | - | ns |
| t_{HIGH} | HIGH period of the SCL clock | | 600 | - | 60 | - | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | 900 | 0 | 70 | ns |
| $t_{SU;DAT}$ | data set-up time | | 100 | - | 10 | - | ns |
| t_r | rise time | SCL signal | 20 | 300 | 10 | 40 | ns |
| t_f | fall time | SCL signal | 20 | 300 | 10 | 40 | ns |
| t_r | rise time | SDA and SCL signals | 20 | 300 | 10 | 80 | ns |
| t_f | fall time | SDA and SCL signals | 20 | 300 | 10 | 80 | ns |
| t_{BUF} | bus free time between a STOP and START condition | | 1.3 | - | 1.3 | - | μs |



15. Application information

A typical application diagram using a complementary antenna connection to the MFRC522 is shown in [Figure 27](#).

The antenna tuning and RF part matching is described in the application note [Ref. 1](#) and [Ref. 2](#).

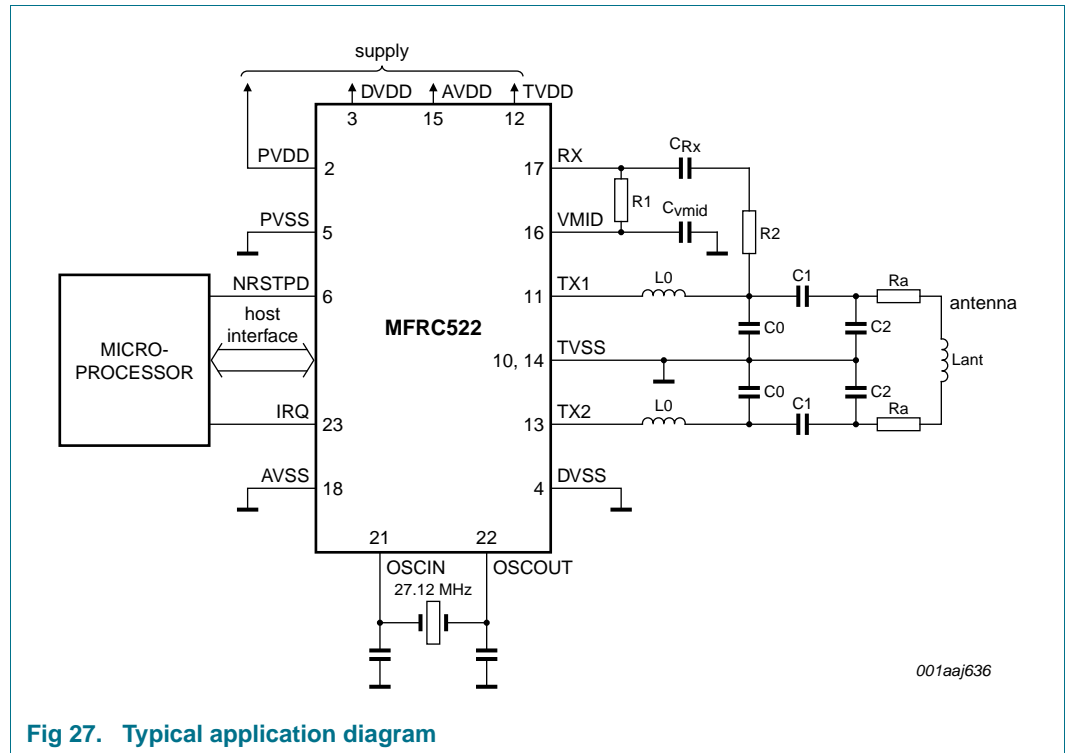


Fig 27. Typical application diagram

16. Test information

16.1 Test signals

16.1.1 Self test

The MFRC522 has the capability to perform a digital self test. The self test is started by using the following procedure:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and implement the Config command.
3. Enable the self test by writing 09h to the AutoTestReg register.
4. Write 00h to the FIFO buffer.
5. Start the self test with the CalcCRC command.
6. The self test is initiated.
7. When the self test has completed, the FIFO buffer contains the following 64 bytes:

FIFO buffer byte values for MFRC522 version 1.0:

00h, C6h, 37h, D5h, 32h, B7h, 57h, 5Ch,
C2h, D8h, 7Ch, 4Dh, D9h, 70h, C7h, 73h,
10h, E6h, D2h, AAh, 5Eh, A1h, 3Eh, 5Ah,
14h, AFh, 30h, 61h, C9h, 70h, DBh, 2Eh,
64h, 22h, 72h, B5h, BDh, 65h, F4h, ECh,
22h, BCh, D3h, 72h, 35h, CDh, AAh, 41h,
1Fh, A7h, F3h, 53h, 14h, DEh, 7Eh, 02h,
D9h, 0Fh, B5h, 5Eh, 25h, 1Dh, 29h, 79h

FIFO buffer byte values for MFRC522 version 2.0:

00h, EBh, 66h, BAh, 57h, BFh, 23h, 95h,
D0h, E3h, 0Dh, 3Dh, 27h, 89h, 5Ch, DEh,
9Dh, 3Bh, A7h, 00h, 21h, 5Bh, 89h, 82h,
51h, 3Ah, EBh, 02h, 0Ch, A5h, 00h, 49h,
7Ch, 84h, 4Dh, B3h, CCh, D2h, 1Bh, 81h,
5Dh, 48h, 76h, D5h, 71h, 061h, 21h, A9h,
86h, 96h, 83h, 38h, CFh, 9Dh, 5Bh, 6Dh,
DCh, 15h, BAh, 3Eh, 7Dh, 95h, 03Bh, 2Fh

16.1.2 Test bus

The test bus is used for production tests. The following configuration can be used to improve the design of a system using the MFRC522. The test bus allows internal signals to be routed to the digital interface. The test bus comprises two sets of test signals which are selected using their subaddress specified in the TestSel2Reg register's TestBusSel[4:0] bits. The test signals and their related digital output pins are described in [Table 156](#) and [Table 157](#).

Table 156. Test bus signals: TestBusSel[4:0] = 07h

| Pins | Internal signal name | Description |
|------|----------------------|--|
| D6 | s_data | received data stream |
| D5 | s_coll | bit-collision detected (106 kBd only) |
| D4 | s_valid | s_data and s_coll signals are valid |
| D3 | s_over | receiver has detected a stop condition |
| D2 | RCV_reset | receiver is reset |
| D1 | - | reserved |

Table 157. Test bus signals: TestBusSel[4:0] = 0Dh

| Pins | Internal test signal name | Description |
|----------|---------------------------|---------------------------------------|
| D6 | clkstable | oscillator output signal |
| D5 | clk27/8 | oscillator output signal divided by 8 |
| D4 to D3 | - | reserved |
| D2 | clk27 | oscillator output signal |
| D1 | - | reserved |

16.1.3 Test signals on pins AUX1 or AUX2

The MFRC522 allows the user to select internal signals for measurement on pins AUX1 or AUX2. These measurements can be helpful during the design-in phase to optimize the design or used for test purposes.

[Table 158](#) shows the signals that can be switched to pin AUX1 or AUX2 by setting AnalogSelAux1[3:0] or AnalogSelAux2[3:0] in the AnalogTestReg register.

Remark: The DAC has a current output, therefore it is recommended that a 1 k Ω pull-down resistor is connected to pin AUX1 or AUX2.

Table 158. Test signal descriptions

| AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value | Signal on pin AUX1 or pin AUX2 |
|---|------------------------------------|
| 0000 | 3-state |
| 0001 | DAC: register TestDAC1 or TestDAC2 |
| 0010 | DAC: test signal Corr1 |
| 0011 | reserved |
| 0100 | DAC: test signal MinLevel |
| 0101 | DAC: test signal ADC_I |
| 0110 | DAC: test signal ADC_Q |
| 0111 to 1001 | reserved |
| 1010 | HIGH |
| 1011 | LOW |
| 1100 | TxActive |

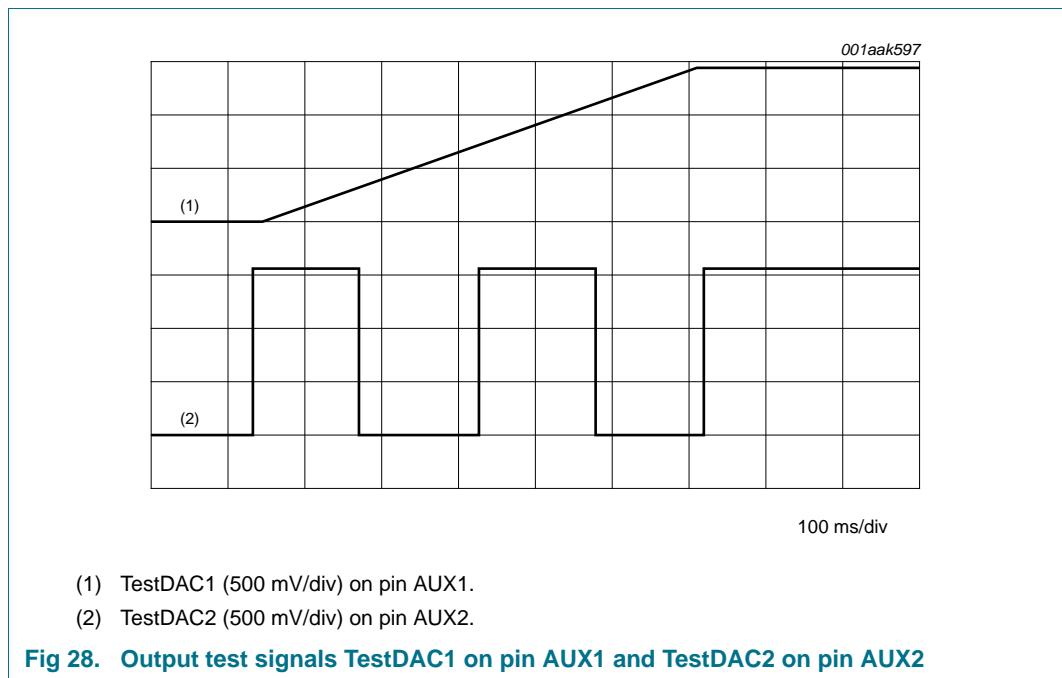
Table 158. Test signal descriptions ...continued

| AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value | Signal on pin AUX1 or pin AUX2 |
|---|--------------------------------|
| 1101 | RxActive |
| 1110 | subcarrier detected |
| 1111 | TstBusBit |

16.1.3.1 Example: Output test signals TestDAC1 and TestDAC2

The AnalogTestReg register is set to 11h. The output on pin AUX1 has the test signal TestDAC1 and the output on pin AUX2 has the test signal TestDAC2. The signal values of TestDAC1 and TestDAC2 are controlled by the TestDAC1Reg and TestDAC2Reg registers.

Figure 28 shows test signal TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2 when the TestDAC1Reg register is programmed with a slope defined by values 00h to 3Fh and the TestDAC2Reg register is programmed with a rectangular signal defined by values 00h and 3Fh.



16.1.3.2 Example: Output test signals Corr1 and MinLevel

Figure 29 shows test signals Corr1 and MinLevel on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 24h.



16.1.3.3 Example: Output test signals ADC channel I and ADC channel Q

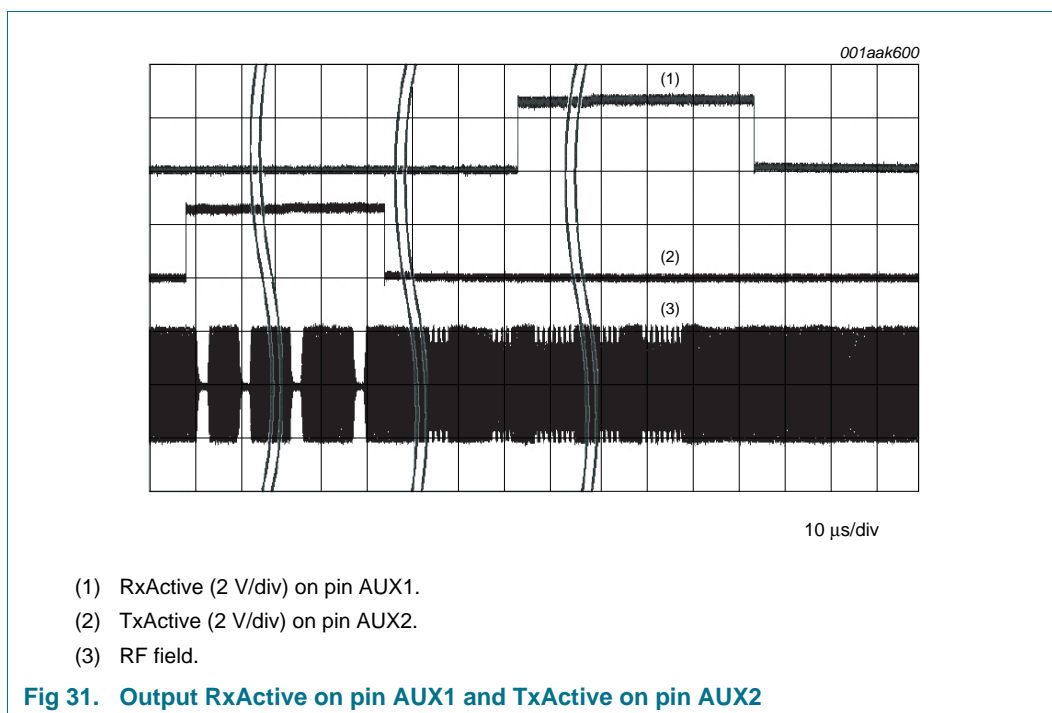
Figure 30 shows the channel behavior test signals ADC_I and ADC_Q on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 56h.



16.1.3.4 Example: Output test signals RxActive and TxActive

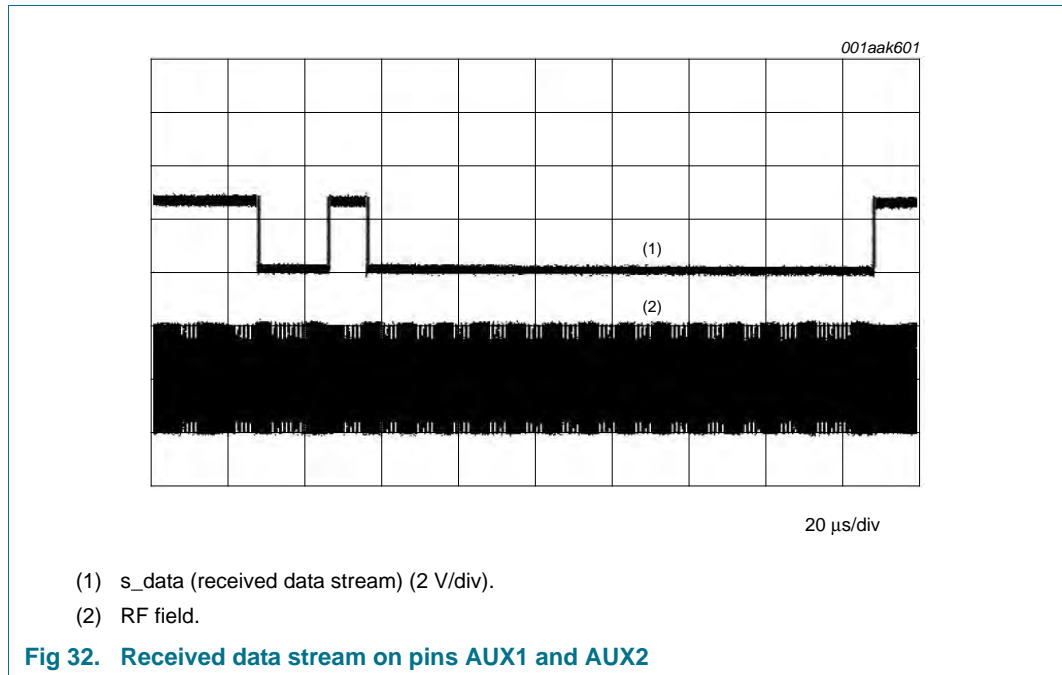
Figure 31 shows the RxActive and TxActive test signals relating to RF communication. The AnalogTestReg register is set to CDh.

- At 106 kBd, RxActive is HIGH during data bits, parity and CRC reception. Start bits are not included
- At 106 kBd, TxActive is HIGH during start bits, data bits, parity and CRC transmission
- At 212 kBd, 424 kBd and 848 kBd, RxActive is HIGH during data bits and CRC reception. Start bits are not included
- At 212 kBd, 424 kBd and 848 kBd, TxActive is HIGH during data bits and CRC transmission



16.1.3.5 Example: Output test signal RX data stream

Figure 32 shows the data stream that is currently being received. The TestSel2Reg register's TestBusSel[4:0] bits are set to 07h to enable test bus signals on pins D1 to D6; see Section 16.1.2 on page 82. The TestSel1Reg register's TstBusBitSel[2:0] bits are set to 06h (pin D6 = s_data) and AnalogTestReg register is set to FFh (TstBusBit) which outputs the received data stream on pins AUX1 and AUX2.



16.1.3.6 PRBS

The pseudo-random binary sequences PRBS9 and PRBS15 are based on ITU-T0150 and are defined with the TestSel2Reg register. Transmission of either data stream is started by the Transmit command. The preamble/sync byte/start bit/parity bit are automatically generated depending on the mode selected.

Remark: All relevant registers for transmitting data must be configured in accordance with ITU-T0150 before selecting PRBS transmission.

17. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

SOT617-1



Fig 33. Package outline SOT617-1 (HVQFN32)

Detailed package information can be found at:
<http://www.nxp.com/package/SOT617-1.html>.

18. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out-of-pack floor life at maximum ambient 30 °C/85 % RH.

19. Packing information



20. Abbreviations

Table 159. Abbreviations

| Acronym | Description |
|------------------|---|
| ADC | Analog-to-Digital Converter |
| BPSK | Binary Phase Shift Keying |
| CRC | Cyclic Redundancy Check |
| CW | Continuous Wave |
| DAC | Digital-to-Analog Converter |
| HBM | Human Body Model |
| I ² C | Inter-integrated Circuit |
| LSB | Least Significant Bit |
| MISO | Master In Slave Out |
| MM | Machine Model |
| MOSI | Master Out Slave In |
| MSB | Most Significant Bit |
| NRZ | Not Return to Zero |
| NSS | Not Slave Select |
| PLL | Phase-Locked Loop |
| PRBS | Pseudo-Random Bit Sequence |
| RX | Receiver |
| SOF | Start Of Frame |
| SPI | Serial Peripheral Interface |
| TX | Transmitter |
| UART | Universal Asynchronous Receiver Transmitter |

21. References

- [1] **Application note** — *MFRC52x Reader IC Family Directly Matched Antenna Design*
- [2] **Application note** — *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

22. Revision history

Table 160. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|--------------------|---------------|---------------|
| MFRC522 v.3.9 | 20160427 | Product data sheet | - | MFRC522 v.3.8 |
| Modifications: | <ul style="list-style-type: none"> • Section 1 "Introduction" and Section 2 "General description": updated and NTAG functionality added • Descriptive title updated | | | |
| MFRC522 v.3.8 | 20140917 | Product data sheet | - | MFRC522 v.3.7 |
| Modifications: | <ul style="list-style-type: none"> • Table 150 "Limiting values": updated | | | |
| MFRC522 v.3.7 | 20140326 | Product data sheet | - | MFRC522 v.3.6 |
| Modifications: | <ul style="list-style-type: none"> • Change of descriptive title • Section 23.4 "Licenses" removed | | | |
| MFRC522 v.3.6 | 20111214 | Product data sheet | - | MFRC522_35 |
| Modifications: | <ul style="list-style-type: none"> • Section 1.1 "Differences between version 1.0 and 2.0" on page 1: added • Table 2 "Ordering information" on page 3: updated • Section 9.3.2.10 "DemodReg register" on page 53: register updated and add reference to Timer unit • Section 8.5 "Timer unit" on page 31: Pre Scaler Information for version 2.0 added • Section 9.3.4.8 "VersionReg register" on page 66: version information structured in chip information and version information updated, including version 1.0 and 2.0 • Section 16.1 "Test signals" on page 82: selftest result including values for version 1.0 and 2.0 | | | |
| MFRC522_35 | 20100621 | Product data sheet | | MFRC522_34 |
| Modifications: | <ul style="list-style-type: none"> • Section 9.3.2.10 "DemodReg register" on page 53: register updated • Section 9.3.3.10 "TModeReg and TPrescalerReg registers" on page 60: register updated • Section 8.5 "Timer unit" on page 31: timer calculation updated • Section 9.3.4.8 "VersionReg register" on page 66: version B2h updated • Section 16.1 "Test signals" on page 82: selftest result updated | | | |
| MFRC522_34 | 20100305 | Product data sheet | | MFRC522_33 |
| Modifications: | <ul style="list-style-type: none"> • Section 8.5 "Timer unit": information added • Table 106 "TModeReg register bit descriptions": bit 7 updated • Table 154 "SPI timing characteristics": row added | | | |
| MFRC522_33 | 20091026 | Product data sheet | - | 112132 |

23. Legal information

23.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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25. Contents

| | | | | | |
|----------|--|----------|----------|--|-----------|
| 1 | Introduction | 1 | 8.6 | Power reduction modes | 32 |
| 2 | General description | 1 | 8.6.1 | Hard power-down | 32 |
| 2.1 | Differences between version 1.0 and 2.0 | 1 | 8.6.2 | Soft power-down mode | 32 |
| 3 | Features and benefits | 2 | 8.6.3 | Transmitter power-down mode | 32 |
| 4 | Quick reference data | 2 | 8.7 | Oscillator circuit | 32 |
| 5 | Ordering information | 3 | 8.8 | Reset and oscillator start-up time | 33 |
| 6 | Block diagram | 4 | 8.8.1 | Reset timing requirements | 33 |
| 7 | Pinning information | 6 | 8.8.2 | Oscillator start-up time | 33 |
| 7.1 | Pin description | 6 | 9 | MFRC522 registers | 34 |
| 8 | Functional description | 8 | 9.1 | Register bit behavior | 34 |
| 8.1 | Digital interfaces | 9 | 9.2 | Register overview | 35 |
| 8.1.1 | Automatic microcontroller interface detection .. | 9 | 9.3 | Register descriptions | 37 |
| 8.1.2 | Serial Peripheral Interface | 10 | 9.3.1 | Page 0: Command and status | 37 |
| 8.1.2.1 | SPI read data | 10 | 9.3.1.1 | Reserved register 00h | 37 |
| 8.1.2.2 | SPI write data | 11 | 9.3.1.2 | CommandReg register | 37 |
| 8.1.2.3 | SPI address byte | 11 | 9.3.1.3 | ComEnReg register | 37 |
| 8.1.3 | UART interface | 11 | 9.3.1.4 | DivlEnReg register | 38 |
| 8.1.3.1 | Connection to a host | 11 | 9.3.1.5 | ComlRqReg register | 38 |
| 8.1.3.2 | Selectable UART transfer speeds | 12 | 9.3.1.6 | DivlRqReg register | 39 |
| 8.1.3.3 | UART framing | 13 | 9.3.1.7 | ErrorReg register | 40 |
| 8.1.4 | I ² C-bus interface | 16 | 9.3.1.8 | Status1Reg register | 41 |
| 8.1.4.1 | Data validity | 17 | 9.3.1.9 | Status2Reg register | 42 |
| 8.1.4.2 | START and STOP conditions | 17 | 9.3.1.10 | FIFODataReg register | 43 |
| 8.1.4.3 | Byte format | 17 | 9.3.1.11 | FIFOLevelReg register | 43 |
| 8.1.4.4 | Acknowledge | 18 | 9.3.1.12 | WaterLevelReg register | 43 |
| 8.1.4.5 | 7-Bit addressing | 19 | 9.3.1.13 | ControlReg register | 44 |
| 8.1.4.6 | Register write access | 19 | 9.3.1.14 | BitFramingReg register | 45 |
| 8.1.4.7 | Register read access | 20 | 9.3.1.15 | CollReg register | 45 |
| 8.1.4.8 | High-speed mode | 21 | 9.3.1.16 | Reserved register 0Fh | 46 |
| 8.1.4.9 | High-speed transfer | 21 | 9.3.2 | Page 1: Communication | 46 |
| 8.1.4.10 | Serial data transfer format in HS mode | 21 | 9.3.2.1 | Reserved register 10h | 46 |
| 8.1.4.11 | Switching between F/S mode and HS mode .. | 23 | 9.3.2.2 | ModeReg register | 47 |
| 8.1.4.12 | MFRC522 at lower speed modes | 23 | 9.3.2.3 | TxModeReg register | 47 |
| 8.2 | Analog interface and contactless UART | 24 | 9.3.2.4 | RxModeReg register | 48 |
| 8.2.1 | General | 24 | 9.3.2.5 | TxControlReg register | 49 |
| 8.2.2 | TX p-driver | 24 | 9.3.2.6 | TxASKReg register | 50 |
| 8.2.3 | Serial data switch | 26 | 9.3.2.7 | TxSelReg register | 50 |
| 8.2.4 | MFIN and MFOUT interface support | 26 | 9.3.2.8 | RxSelReg register | 51 |
| 8.2.5 | CRC coprocessor | 28 | 9.3.2.9 | RxThresholdReg register | 52 |
| 8.3 | FIFO buffer | 28 | 9.3.2.10 | DemodReg register | 52 |
| 8.3.1 | Accessing the FIFO buffer | 28 | 9.3.2.11 | Reserved register 1Ah | 53 |
| 8.3.2 | Controlling the FIFO buffer | 28 | 9.3.2.12 | Reserved register 1Bh | 53 |
| 8.3.3 | FIFO buffer status information | 28 | 9.3.2.13 | MfTxReg register | 53 |
| 8.4 | Interrupt request system | 29 | 9.3.2.14 | MfRxReg register | 54 |
| 8.4.1 | Interrupt sources overview | 29 | 9.3.2.15 | Reserved register 1Eh | 54 |
| 8.5 | Timer unit | 30 | 9.3.2.16 | SerialSpeedReg register | 54 |
| | | | 9.3.3 | Page 2: Configuration | 56 |
| | | | 9.3.3.1 | Reserved register 20h | 56 |

continued >>

| | | | | | |
|-----------|---|-----------|-----------|--|-----------|
| 9.3.3.2 | CRCResultReg registers | 56 | 16.1.2 | Test bus | 81 |
| 9.3.3.3 | Reserved register 23h | 57 | 16.1.3 | Test signals on pins AUX1 or AUX2 | 82 |
| 9.3.3.4 | ModWidthReg register | 57 | 16.1.3.1 | Example: Output test signals TestDAC1 and TestDAC2 | 83 |
| 9.3.3.5 | Reserved register 25h | 57 | 16.1.3.2 | Example: Output test signals Corr1 and MinLevel | 83 |
| 9.3.3.6 | RFCfgReg register | 58 | 16.1.3.3 | Example: Output test signals ADC channel I and ADC channel Q | 84 |
| 9.3.3.7 | GsNReg register | 58 | 16.1.3.4 | Example: Output test signals RxActive and TxActive | 85 |
| 9.3.3.8 | CWGsPReg register | 59 | 16.1.3.5 | Example: Output test signal RX data stream | 86 |
| 9.3.3.9 | ModGsPReg register | 59 | 16.1.3.6 | PRBS | 86 |
| 9.3.3.10 | TModeReg and TPrescalerReg registers | 59 | 17 | Package outline | 87 |
| 9.3.3.11 | TReloadReg register | 61 | 18 | Handling information | 88 |
| 9.3.3.12 | TCounterValReg register | 61 | 19 | Packing information | 88 |
| 9.3.4 | Page 3: Test | 62 | 20 | Abbreviations | 89 |
| 9.3.4.1 | Reserved register 30h | 62 | 21 | References | 89 |
| 9.3.4.2 | TestSel1Reg register | 62 | 22 | Revision history | 90 |
| 9.3.4.3 | TestSel2Reg register | 63 | 23 | Legal information | 91 |
| 9.3.4.4 | TestPinEnReg register | 63 | 23.1 | Data sheet status | 91 |
| 9.3.4.5 | TestPinValueReg register | 64 | 23.2 | Definitions | 91 |
| 9.3.4.6 | TestBusReg register | 64 | 23.3 | Disclaimers | 91 |
| 9.3.4.7 | AutoTestReg register | 65 | 23.4 | Trademarks | 92 |
| 9.3.4.8 | VersionReg register | 65 | 24 | Contact information | 92 |
| 9.3.4.9 | AnalogTestReg register | 66 | 25 | Contents | 93 |
| 9.3.4.10 | TestDAC1Reg register | 67 | | | |
| 9.3.4.11 | TestDAC2Reg register | 67 | | | |
| 9.3.4.12 | TestADCReg register | 67 | | | |
| 9.3.4.13 | Reserved register 3Ch | 67 | | | |
| 10 | MFRC522 command set | 69 | | | |
| 10.1 | General description | 69 | | | |
| 10.2 | General behavior | 69 | | | |
| 10.3 | MFRC522 command overview | 69 | | | |
| 10.3.1 | MFRC522 command descriptions | 70 | | | |
| 10.3.1.1 | Idle | 70 | | | |
| 10.3.1.2 | Mem | 70 | | | |
| 10.3.1.3 | Generate RandomID | 70 | | | |
| 10.3.1.4 | CalcCRC | 70 | | | |
| 10.3.1.5 | Transmit | 70 | | | |
| 10.3.1.6 | NoCmdChange | 70 | | | |
| 10.3.1.7 | Receive | 71 | | | |
| 10.3.1.8 | Transceive | 71 | | | |
| 10.3.1.9 | MFAuthent | 71 | | | |
| 10.3.1.10 | SoftReset | 72 | | | |
| 11 | Limiting values | 73 | | | |
| 12 | Recommended operating conditions | 73 | | | |
| 13 | Thermal characteristics | 73 | | | |
| 14 | Characteristics | 74 | | | |
| 14.1 | Timing characteristics | 77 | | | |
| 15 | Application information | 80 | | | |
| 16 | Test information | 81 | | | |
| 16.1 | Test signals | 81 | | | |
| 16.1.1 | Self test | 81 | | | |

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