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Team Nexperia



# PDTA144VMB

PNP resistor-equipped transistor; R1 = 47 k $\Omega$ , R2 = 10 k $\Omega$

Rev. 1 — 26 June 2012

Product data sheet

## 1. Product profile

### 1.1 General description

PNP Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC144VMB.

### 1.2 Features and benefits

- 100 mA output current capability
- Reduces component count
- Built-in bias resistors
- Reduces pick and place costs
- Simplifies circuit design
- AEC-Q101 qualified
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm

### 1.3 Applications

- Low-current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

### 1.4 Quick reference data

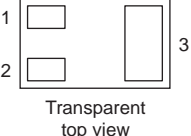
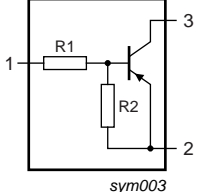
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-50	V
I <sub>O</sub>	output current		-	-	-100	mA
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	33	47	61	k $\Omega$
R2/R1	bias resistor ratio		0.17	0.21	0.26	



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p>Transparent top view</p> <p><b>DFN1006B-3 (SOT883B)</b></p>	 <p><i>sym003</i></p>
2	G	GND (emitter)		
3	O	output (collector)		

## 3. Ordering information

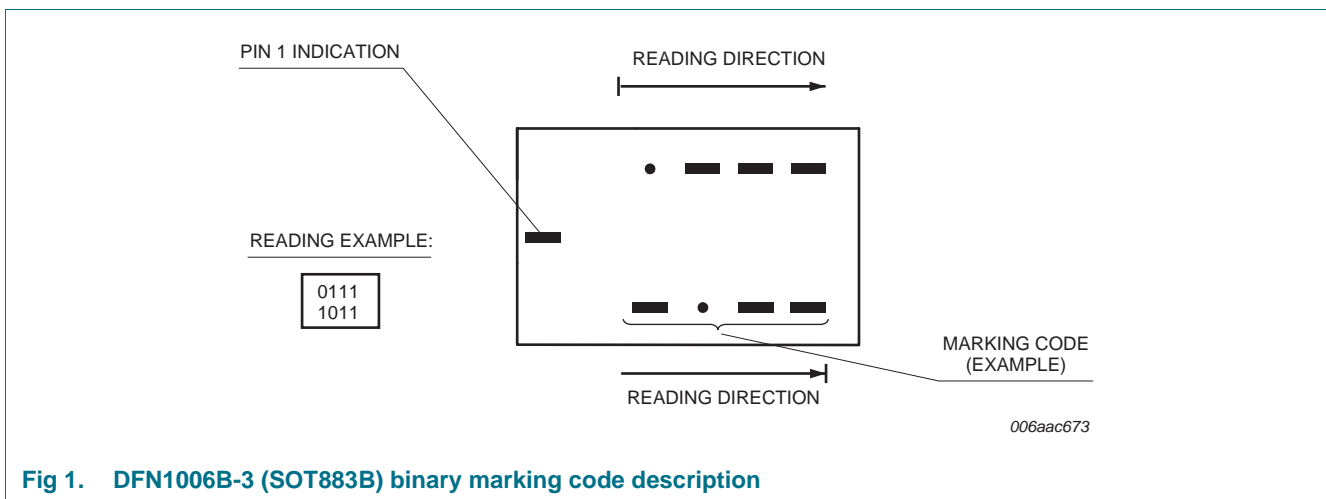
Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PDTA144VMB	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PDTA144VMB	0010 1101



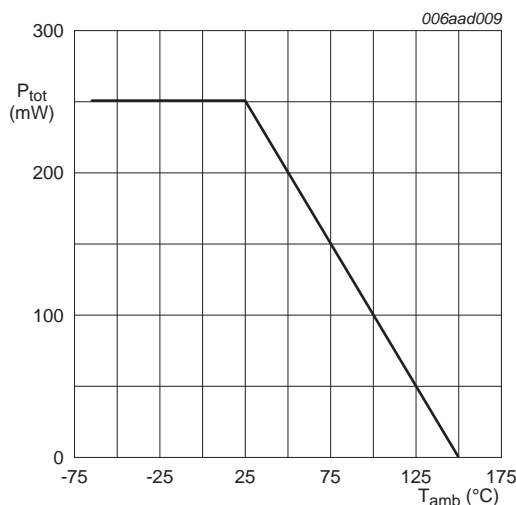
## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CBO</sub>	collector-base voltage	open emitter	-	-50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	-15	V
V <sub>I</sub>	input voltage	positive	-	15	V
		negative	-	-40	V
I <sub>O</sub>	output current		-	-100	mA
I <sub>CM</sub>	peak collector current	pulsed; t <sub>p</sub> ≤ 1 ms	-	-100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	250	mW
T <sub>j</sub>	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-65	150	°C
T <sub>stg</sub>	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

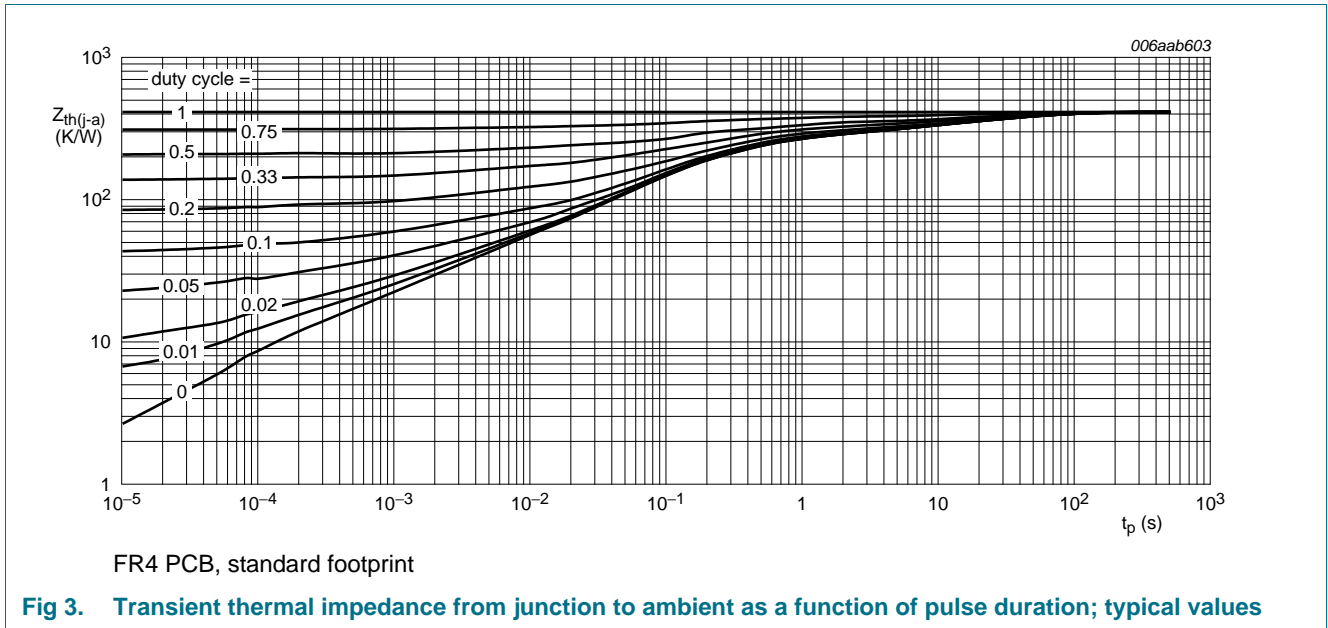
**Fig. 2. Power derating curve for DFN1006B-3 (SOT883B)**

## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

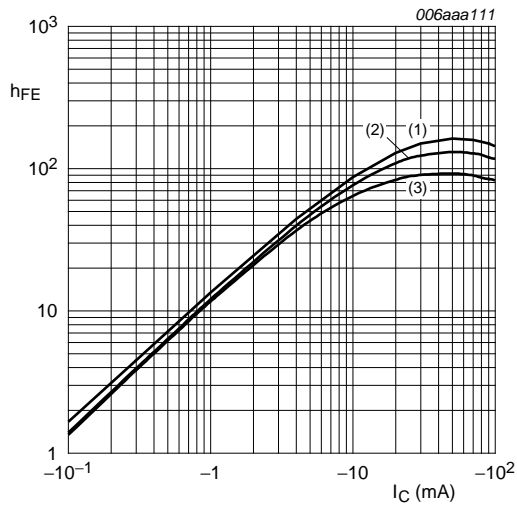


## 7. Characteristics

**Table 7. Characteristics**

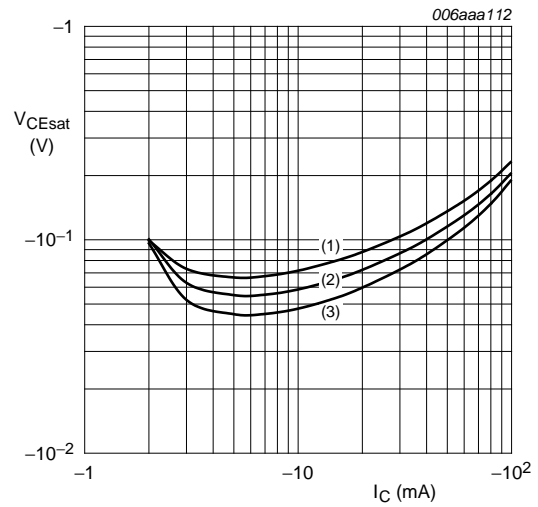
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-1	μA
		V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-5	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-150	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -5 mA; T <sub>amb</sub> = 25 °C	40	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -10 mA; I <sub>B</sub> = -0.5 mA; T <sub>amb</sub> = 25 °C	-	-	-150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -100 μA; T <sub>amb</sub> = 25 °C	-	-3.1	-1	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = -0.3 V; I <sub>C</sub> = -2 mA; T <sub>amb</sub> = 25 °C	-6	-3.8	-	V
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	33	47	61	kΩ
R2/R1	bias resistor ratio		0.17	0.21	0.26	
C <sub>C</sub>	collector capacitance	V <sub>CB</sub> = -10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz; T <sub>amb</sub> = 25 °C	-	-	2	pF
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -10 mA; f = 100 MHz; T <sub>amb</sub> = 25 °C	-	180	-	MHz

[1] Characteristics of built-in transistor.



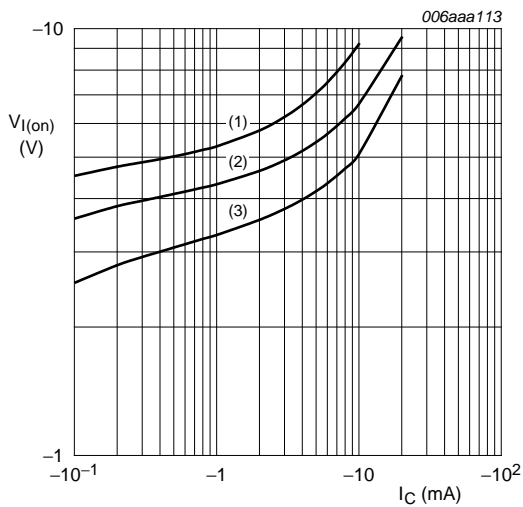
$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig 4. DC current gain as a function of collector current; typical values**



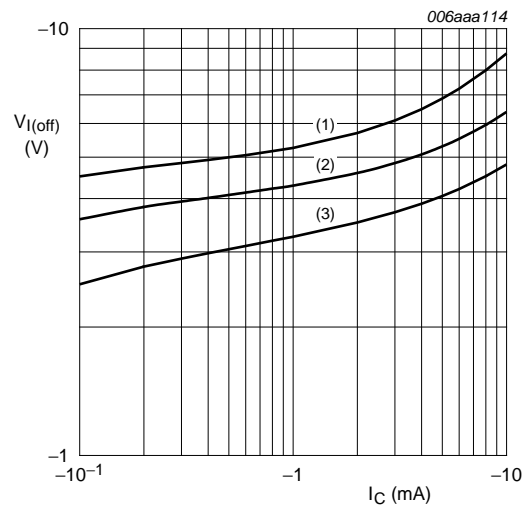
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values**



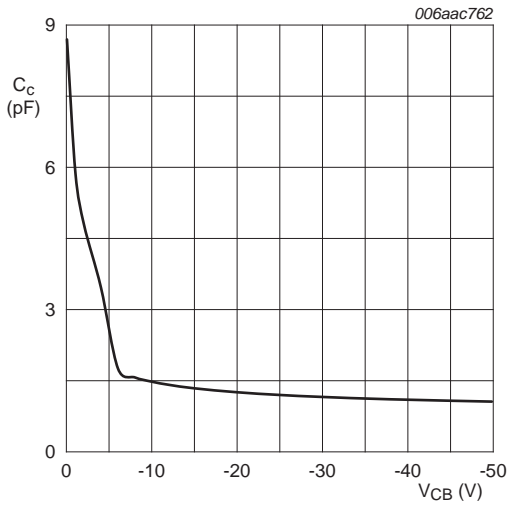
$V_{CE} = -0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

**Fig 6. On-state input voltage as a function of collector current; typical values**



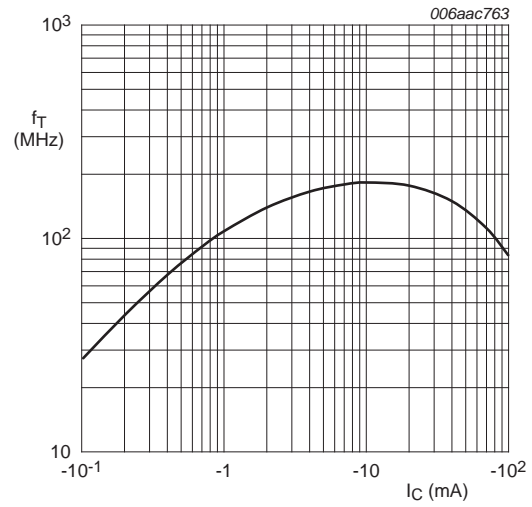
$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

**Fig 7. Off-state input voltage as a function of collector current; typical values**



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 8. Collector capacitance as a function of collector-base voltage; typical values of built-in transistor**



$V_{CE} = -5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 9. Transition frequency as a function of collector current; typical values of built-in transistor**

## 8. Test information

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 9. Package outline

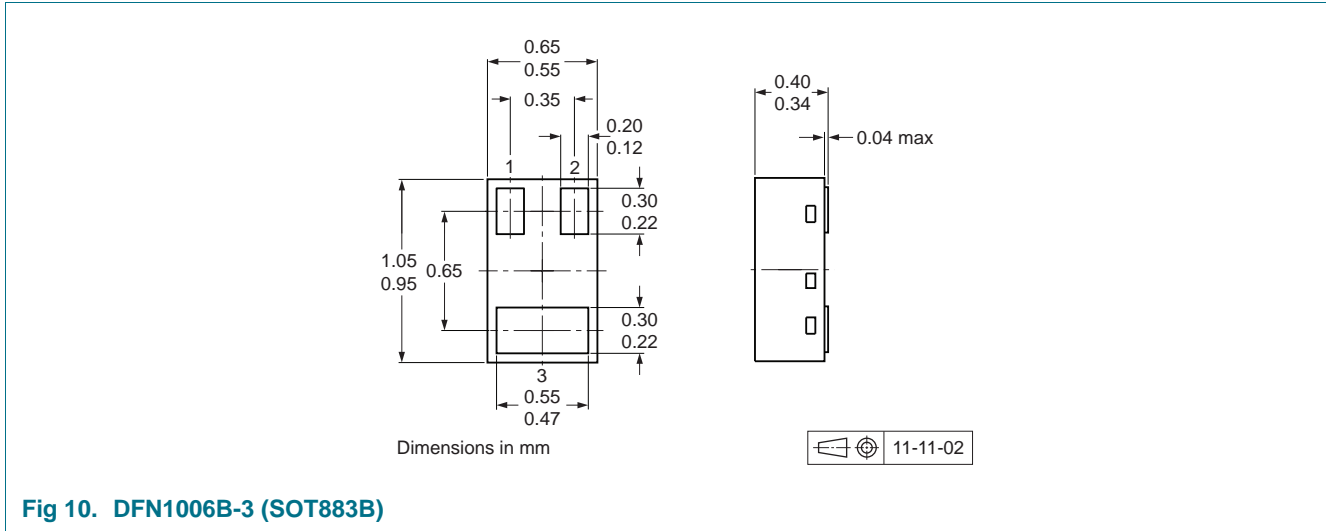


Fig 10. DFN1006B-3 (SOT883B)

## 10. Soldering

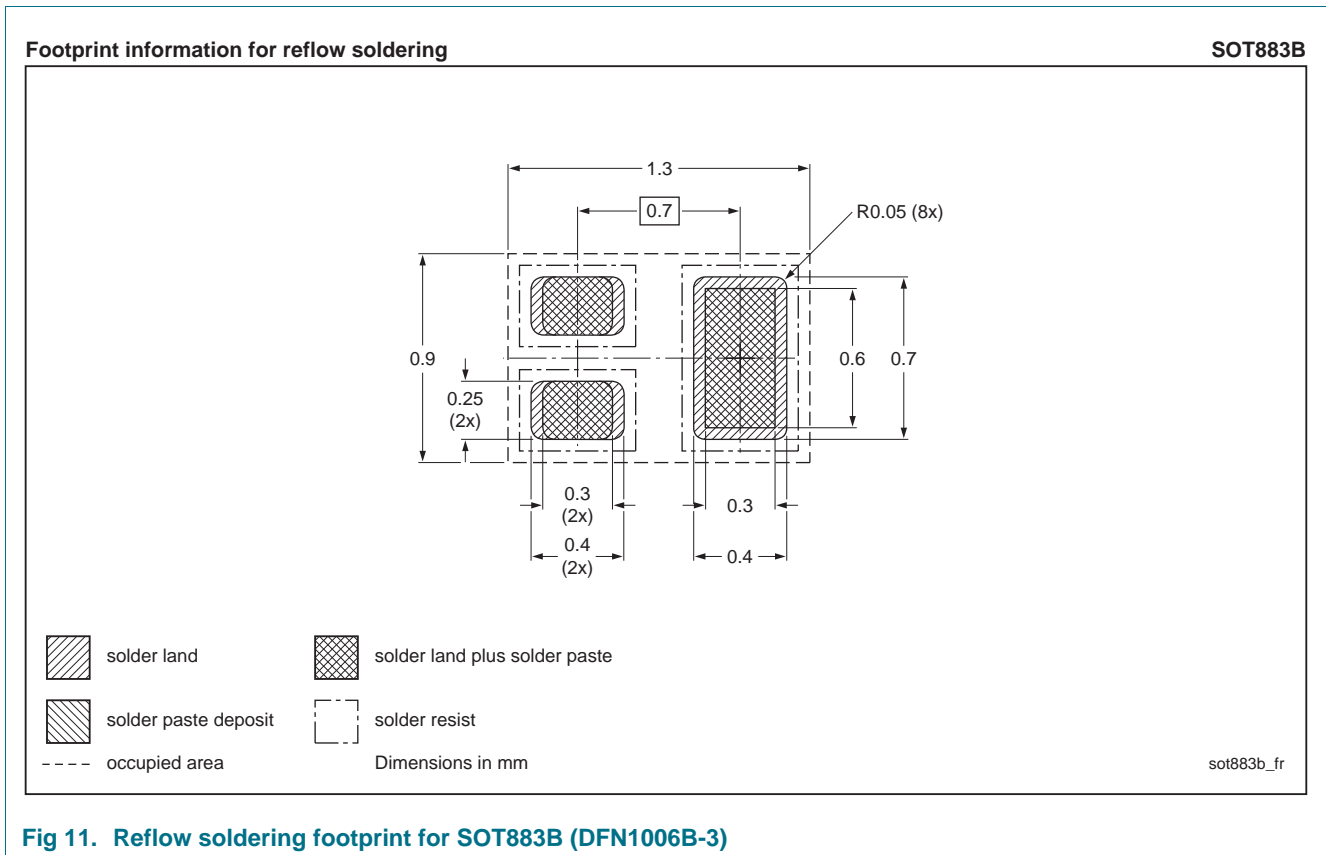


Fig 11. Reflow soldering footprint for SOT883B (DFN1006B-3)



## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA144VMB v.1	20120626	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1]</sup> [2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Document identifier: PDTA144VMB

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