CYW4339

Single-Chip 5G WiFi IEEE 802.11ac MAC/ Baseband/Radio with Integrated Bluetooth 4.1

General Description

The Cypress® CYW4339 single-chip device provides the highest level of integration for Internet of Things and handheld wireless system with integrated single-stream IEEE 802.11ac MAC/baseband/radio and Bluetooth 4.1. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 433.3 Mbps. In addition, all the rates specified in IEEE 802.11a/b/g/n are supported. Included on-chip are 2.4 GHz and 5 GHz transmit amplifiers, and receive low-noise amplifiers. Optional external PAs, LNAs, and antenna diversity are also supported.

For the WLAN section, several alternative host interface options are included: an SDIO v3.0 interface that can operate in 4b or 1b and a PCIe Gen1 interface (3.0 compliant). For the Bluetooth section, host interface options of a high-speed 4-wire UART and USB 2.0 full-speed (12 Mbps) are provided.

Using advanced design techniques and process technology to reduce active and idle power, the CYW4339 is designed to address the needs of mobile devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology and allows for direct operation from a mobile platform battery while maximizing battery life.

The CYW4339 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. In addition, coexistence support for external radios (such as LTE cellular, GPS, and WiMAX) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission is achieved.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Cypress to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4339	CYW4339
BCM4339XKUBG	CYW4339XKUBG
BCM4339NKFFBG	CYW4339NKFFBG
BCM4339XKWBG	CYW4339XKWBG

Features

IEEE 802.11x Key Features

- IEEE 802.11ac compliant.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports Rx space-time block coding (STBC)
- Supports IEEE 802.11ac/n beamforming.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Support for optional front-end modules (FEM) with external PAs and LNAs
- Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE, GPS, or WiMAX
- Supports standard SDIO v3.0 (including DDR50 mode at 50 MHz and SDR104 mode at 208 MHz, 4-bit and 1-bit) host interfaces.
- Backward compatible with SDIO v2.0 host interfaces.
- PCIe mode (FCBGA package only) complies with PCI Express base specification revision 3.0 compliant Gen1 interface for ×1 lane and power management base specification.
- Integrated ARMCR4™ processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 768 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

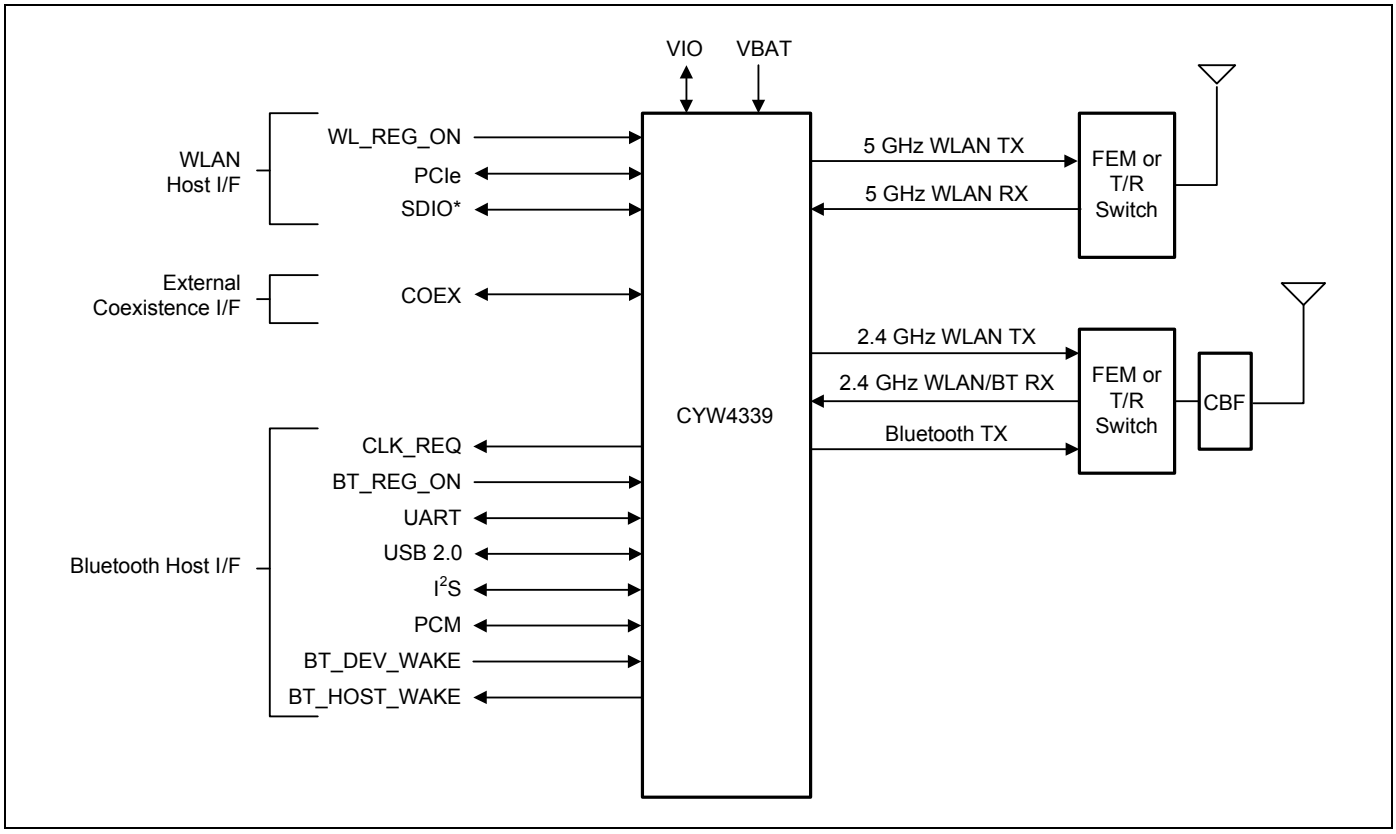
Bluetooth Key Features

- Complies with Bluetooth Core Specification Version 4.1 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a USB or high-speed UART interface and PCM for audio data.
- USB 2.0 full-speed (12 Mbps) supported (FCFBGA and WLCSP packages).
- Low power consumption improves battery life of handheld devices.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.
- Supports serial flash interfaces.

General Features

- Supports battery voltage range from 3.0V to 5.25V supplies with internal switching regulator.
- Programmable dynamic power management
- OTP: 502 bytes of user-accessible memory
- GPIOs: 12 on FCFBGA, nine on WLBGA, and 16 on WLCSP
- Package options:
  - 160 ball FCFBGA (8 mm x 8 mm, 0.4 mm pitch)
  - 145 ball WLBGA (4.87 mm × 5.413 mm, 0.4 mm pitch)
  - 286 bump WLCSP (4.87 mm × 5.413 mm, 0.2 mm pitch)Security:
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Figure 1: Functional Block Diagram



Contents

1. Overview

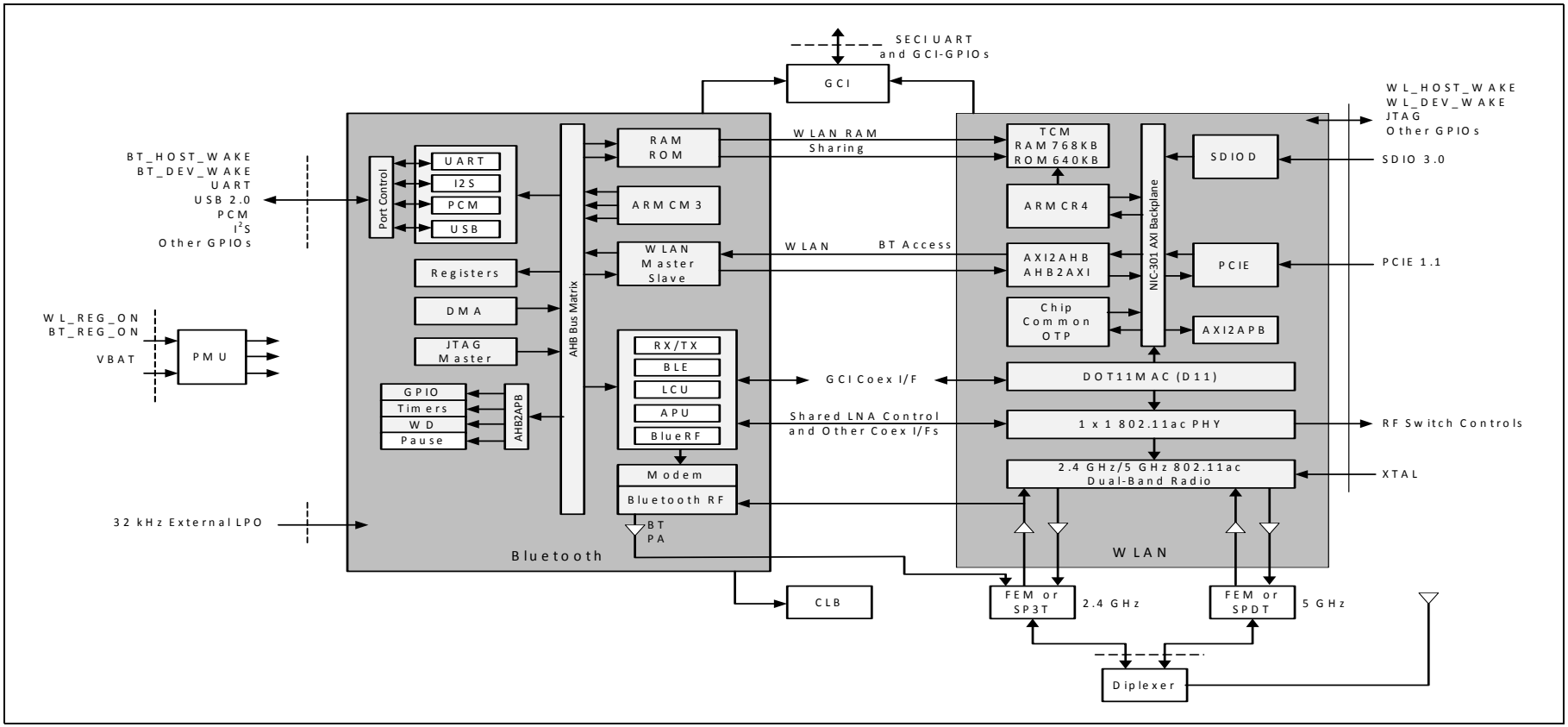
1.1 Overview

The Cypress CYW4339 single-chip device provides the highest level of integration for IoT applications or handheld wireless system, with integrated IEEE 802.11 a/b/g/n/ac MAC/baseband/radio, Bluetooth 4.1 + enhanced data rate (EDR).

It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

The following figure shows the interconnect of all the major physical blocks in the CYW4339 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 1. CYW4339 Block Diagram



1.2 Features

The CYW4339 supports the following features:

- IEEE 802.11a/b/g/n/ac dual-band radio with virtual-simultaneous dual-band operation
- Bluetooth v4.1 + EDR with integrated Class 1 PA
- Concurrent Bluetooth, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- WLAN host interface options:
  - SDIO v3.0 (1-bit/4-bit)—up to 208 MHz clock rate in SDR104 mode
- BT host digital interface (which can be used concurrently with the above interfaces):
  - UART (up to 4 Mbps)
- BT supports full-speed USB version 1.1 for FCBGA package.
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receptions
- I^2S/PCM for BT audio
- HCI high-speed UART (H4, H4+, H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Bluetooth low-power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth Wide Band Speech (WBS)
- Audio rate-matching algorithms
- Multiple simultaneous A2DP audio streams

1.3 Standards Compliance

The CYW4339 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.1 (Bluetooth Low Energy)
- IEEE802.11ac single-stream mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance—on silicon solution compliant with IEEE 3 wire requirements

The CYW4339 will support the following future drafts/standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11k Radio Resource Measurement

2. Power Supplies and Power Management

2.1 Power Supply Topology

One buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW4339. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT (3.0V to 5.25V DC maximum) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW4339.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off and on based on the dynamic demands of the digital baseband.

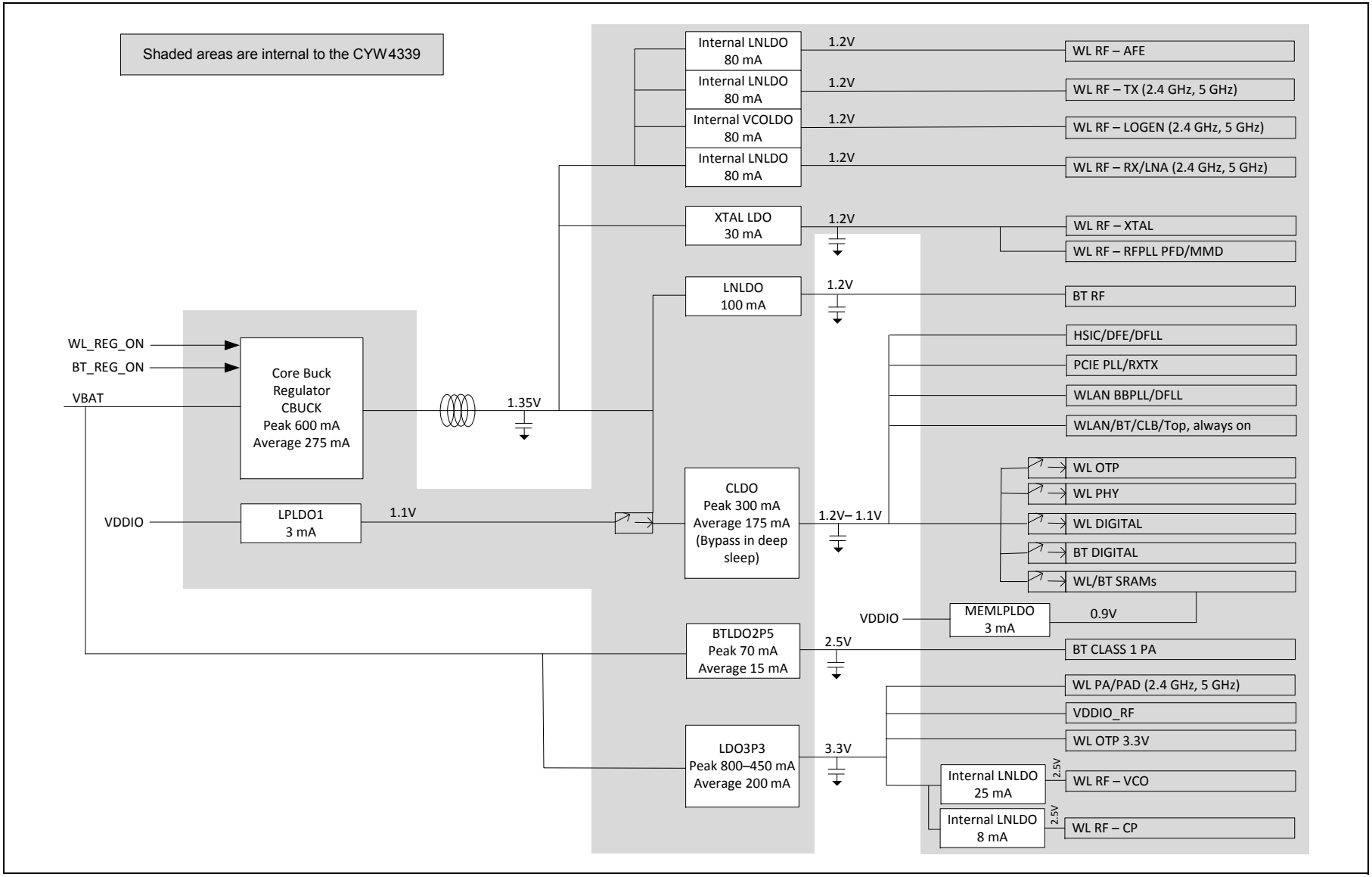
The CYW4339 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the CYW4339 with all the voltages it requires, further reducing leakage currents.

2.2 PMU Features

- VBAT to 1.35V (275 mA nominal, 600 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3V (200 mA nominal, 450 mA maximum) LDO3P3
- VBAT to 2.5V (15 mA nominal, 70 mA maximum) BTLDO2P5
- 1.35V to 1.2V (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2V (175 mA nominal, 300 mA maximum) CLDO with bypass mode for deep-sleep
- Additional internal LDOs (not externally accessible)

The following figure shows the regulators and a typical power topology.

Figure 2. Typical Power Topology for CYW4339



2.3 WLAN Power Management

The CYW4339 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW4339 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW4339 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW4339 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at the 32.768 kHz LPO clock frequency) in the PMU sequencer are used to turn on and turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW4339 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the CYW4339 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW4339 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power consumption to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip, including both analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
- Power-down mode—The CYW4339 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic reenabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states (enabled, disabled, transition_on, and transition_off) and has a timer that contains 0 when the resource is enabled or disabled and a nonzero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the Resource Pending bit for the resource and inverts the Resource State bit.

- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW4339 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW4339 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW4339 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, the provided VDDIO remains applied to the CYW4339, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW4339 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW4339 is powered on from this state, it is the same as a normal power-up, and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW4339 has two signals (see Table 1) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power-Up Sequence and Timing on page 119.

Table 1. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4339 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW4339 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

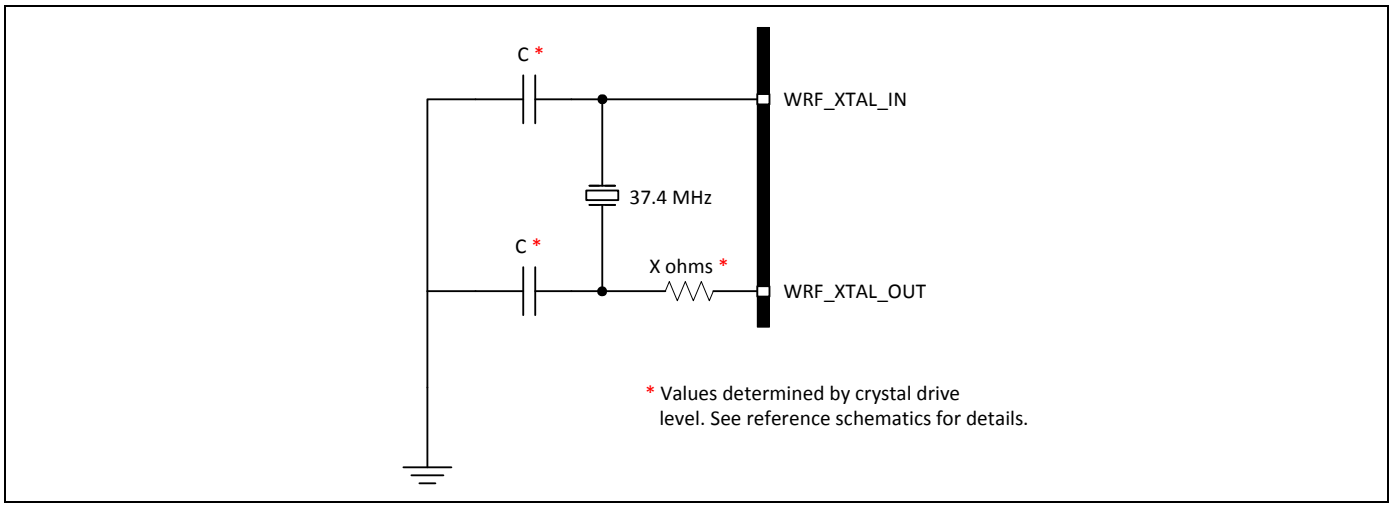
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW4339 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 3. Consult the reference schematics for the latest configuration and recommended components.

Figure 3. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW4339 generates the radio frequencies, clocks, and data/packet timing, enabling the CYW4339 to operate using a wide selection of frequency references.

For SDIO applications, the recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in Table 2.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for details.

3.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be used. The recommended default frequency is 37.4 MHz. This must meet the phase noise requirements listed in Table 2.

If used, the external clock should be connected to the WRF_XTAL_IN pin through an external 1000 pF coupling capacitor, as shown in Figure 4. The internal clock buffer connected to this pin will be turned off when the CYW4339 goes into sleep mode. When the clock buffer turns on and off, there will be a small impedance variation. Power must be supplied to the WRF_XTAL_BUCK_VDD1P5 pin.

Figure 4. Recommended Circuit to Use with an External Reference Clock

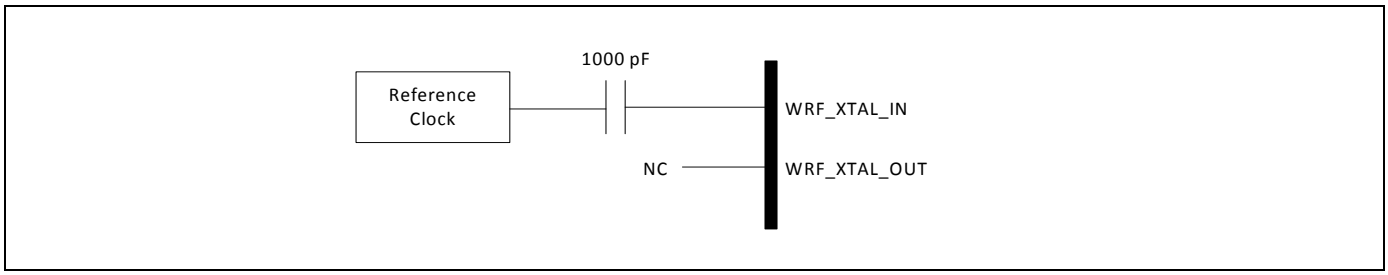


Table 2. Crystal Oscillator and External Clock—Requirements and Performance

Parameter	Conditions/Notes	Crystal[1]			External Frequency Reference[2 3]			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	2.4 GHz and 5 GHz bands, IEEE 802.11ac operation	35	37.4	38.4	–	37.4	–	MHz
Frequency	5 GHz band, IEEE 802.11n operation only	19	37.4	38.4	35	37.4	38.4	MHz
Frequency	2.4 GHz band IEEE 802.11n operation, and both bands legacy 802.11a/b/g operation only	Ranges between 19 MHz and 38.4 MHz[4]						
Frequency tolerance over the lifetime of the equipment, including temperature[5]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_IN)	Resistive	–	–	–	30k	100k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_IN input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_IN input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_IN input voltage (see Figure 4)	AC-coupled analog signal	–	–	–	1000	–	1200	mV_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase noise[6] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase noise[6] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/Hz

Table 2. Crystal Oscillator and External Clock—Requirements and Performance (Cont.)

Parameter	Conditions/Notes	Crystal[1]			External Frequency Reference[2 3]			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Phase noise[6] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase noise[6] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz
Phase noise[6] (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–148	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–155	dBc/Hz

1. (Crystal) Use WRF_XTAL_IN and WRF_XTAL_OUT.

2. See External Frequency Reference for alternative connection methods.

3. For a clock reference other than 37.4 MHz, 20 × log10(f/37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.

4. The frequency step size is approximately 80 Hz.

5. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

6. Assumes that external clock has a flat phase-noise response above 100 kHz.

3.3 Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard mobile platform reference frequencies of 19.2, 19.8, 24, 26, 33.6, 37.4, and 38.4 MHz, but also other frequencies in this range with an approximate resolution of 80 Hz. The CYW4339 must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Cypress for details.

The reference frequency for the CYW4339 may be set in the following ways:

- Set the xtalfreq=xxxxx parameter in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.
- Autodetect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the CYW4339 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for automatic frequency detection to work correctly, the CYW4339 must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 3 and is present during power-on reset.

3.4 External 32.768 kHz Low-Power Oscillator

The CYW4339 uses a secondary low-frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 3.

Table 3. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[1]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

1. When power is applied or switched off.

4. Bluetooth Subsystem Overview

The Cypress CYW4339 is a Bluetooth 4.1 + EDR-compliant, baseband processor/2.4 GHz transceiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth plus Wi-Fi system.

The CYW4339 is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. The CYW4339 incorporates all Bluetooth 4.1 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

The CYW4339 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

4.1 Features

Major Bluetooth features of the CYW4339 include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.1 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO)—Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports Bluetooth 4.1 packet types
- Supports maximum Bluetooth data rates over HCI UART
- BT supports full-speed USB version 1.1 in the FCBGA package
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Cypress fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes

- Bluetooth clock request
- Bluetooth standard sniff
- Deep-sleep modes and software regulator shutdown

- TCXO input and autodetection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

4.2 Bluetooth Radio

The CYW4339 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality.

4.2.1 Transmit

The CYW4339 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path performs signal filtering, I/Q upconversion, output power amplification, and RF filtering. The transmitter path also incorporates π/4-DQPSK and 8-DPSK modulations for 2 Mbps and 3 Mbps EDR support, respectively. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth Class 1 or Class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near-thermal-noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYW4339 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator

The radio portion of the CYW4339 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can determine whether the transmitter should increase or decrease its output power.

4.2.8 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW4339 uses an internal RF and IF loop filter.

4.2.9 Calibration

The CYW4339 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features, with the following benefits:

- Dual-mode bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Bluetooth Low Energy

The CYW4339 supports the Bluetooth Low Energy operating mode.

5.3 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

5.4 Test Mode Support

The CYW4339 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW4339 also supports enhanced testing features to simplify RF debugging, qualification, and type-approval testing. These features include:

- Fixed-frequency carrier-wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed-frequency constant-receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.5 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the CYW4339 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

5.5.1 RF Power Management

The BBC generates power-down control signals to the 2.4 GHz transceiver for the transmit path, receive path, PLL, and power amplifier. The transceiver then processes the power-down functions accordingly.

5.5.2 Host Controller Power Management

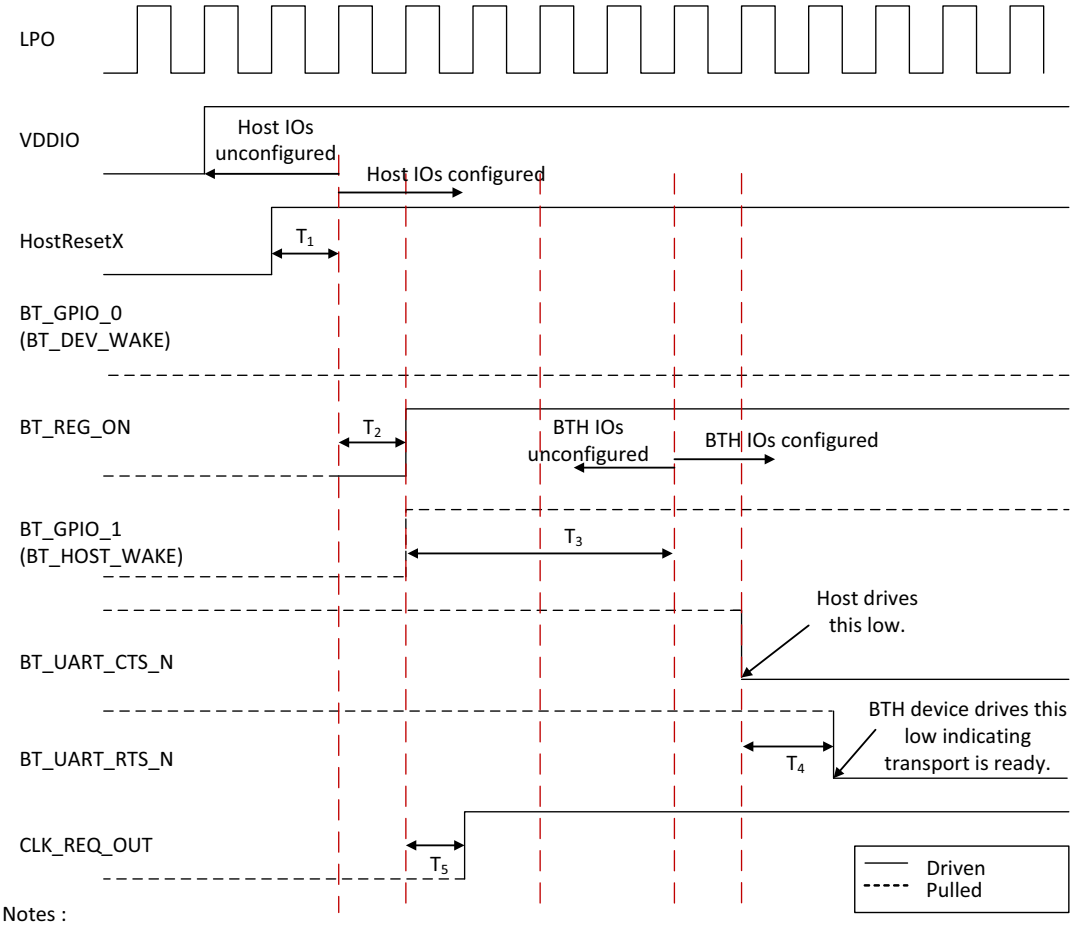
When running in UART mode, the CYW4339 may be configured so that dedicated signals are used for power management handshaking between the CYW4339 and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Table 4 describes the power-control handshake signals used with the UART interface.

Table 4. Power Control Pin Description

Signal	Mapped to Pin	Type	Description
BT_DEV_WAKE	BT_GPIO_0	I	Bluetooth device wake-up: Signal from the host to the CYW4339 indicating that the host requires attention. • Asserted: The Bluetooth device must wake-up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	BT_GPIO_1	O	Host wake up. Signal from the CYW4339 to the host indicating that the CYW4339 requires attention. • Asserted: host device must wake-up or remain awake. • Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	BT_CLK_REQ_OUT WL_CLK_REQ_OUT	O	The CYW4339 asserts CLK_REQ when either the Bluetooth or WLAN block wants the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW4339 powers up or resets when VDDIO is present.
Note: Pad function Control Register is set to 0 for these pins. See DC Characteristics for more details.			

Figure 5. Startup Signaling Sequence



Notes :

- T_1 is the time for the host to settle its IOs after a reset.
- T_2 is the time for the host to drive BT_REG_ON high after the host IOs are configured.
- T_3 is the time for the BTH device to settle its IOs after a reset and the reference clock settling time has elapsed.
- T_4 is the time for the BTH device to drive BT_UART_RTS_N low after the host drives BT_UART_CTS_N low. This assumes the BTH device has completed initialization.
- T_5 is the time for the BTH device to drive CLK_REQ_OUT high after BT_REG_ON goes high. The CLK_REQ_OUT pin is used in designs that have an external reference clock source from the host. It is irrelevant on clock-based designs where the BTH device generates its own reference clock from an external crystal connected to its oscillator circuit.
- The timing diagram assumes that VBAT is present.

5.5.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW4339 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW4339 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW4339 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

During the low-power shut-down state, provided VDDIO remains applied to the CYW4339, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the CYW4339 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW4339 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW4339 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.5.4 Wideband Speech

The CYW4339 provides support for wideband speech (WBS) using on-chip SmartAudio technology. The CYW4339 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

5.5.5 Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bitstream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bitstream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW4339 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 6 and Figure 7 show audio waveforms with and without Packet Loss Concealment. Cypress PLC and bit-error correction (BEC) algorithms also support wideband speech.

Figure 6. CVSD Decoder Output Waveform Without PLC

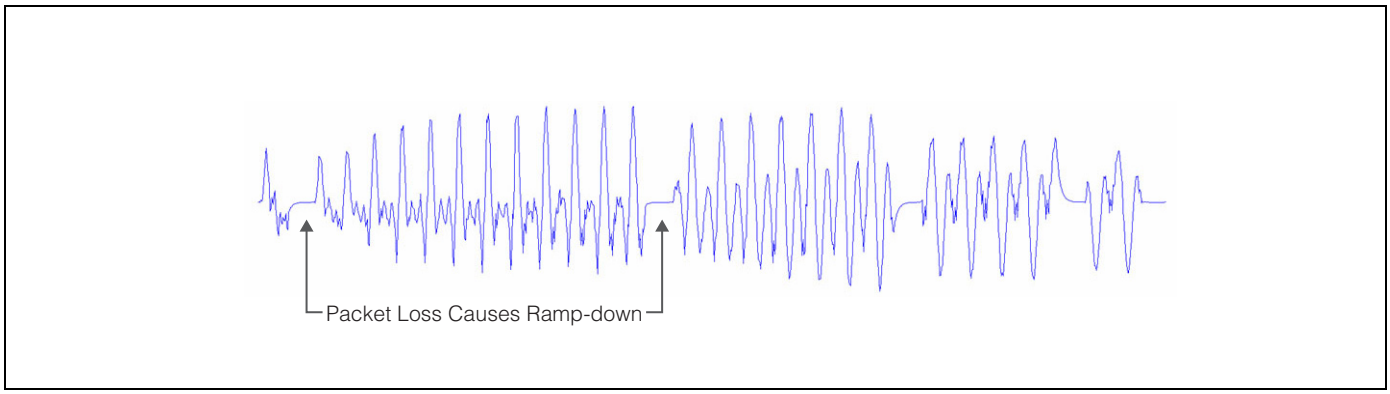
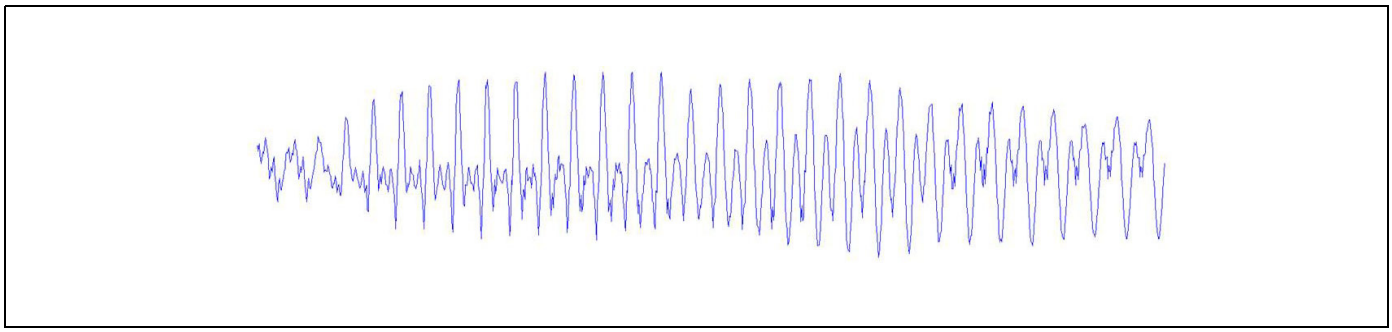


Figure 7. CVSD Decoder Output Waveform After Applying PLC



5.5.6 Audio Rate-Matching Algorithms

The CYW4339 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth audio data rates.

5.5.7 Codec Encoding

The CYW4339 can support SBC and mSBC encoding and decoding for wideband speech.

5.5.8 Multiple Simultaneous A2DP Audio Streams

The CYW4339 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.5.9 Burst Buffer Operation

The CYW4339 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.6 Adaptive Frequency Hopping

The CYW4339 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.7 Advanced Bluetooth/WLAN Coexistence

The CYW4339 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. The CYW4339 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The CYW4339 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW4339 also supports Transmit Power Control (TPC) on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

5.8 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW4339 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 608 KB of ROM memory for program storage and boot ROM, 192 KB of RAM for data scratch-pad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or feature additions. These patches may be downloaded from the host to the CYW4339 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the CYW4329 and CYW4330 devices.

6.1 RAM, ROM, and Patch Memory

The CYW4339 Bluetooth core has 192 KB of internal RAM which is mapped between general purpose scratch-pad memory and patch memory and 608 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables feature additions and bug fixes to the ROM memory.

6.2 Reset

The CYW4339 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes high. If BT_REG_ON is low, then the POR circuit is held in reset.

7. Bluetooth Peripheral Transport Unit

7.1 SPI Interface

The CYW4339 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates are possible. The physical interface between the SPI master and the CYW4339 contains the four SPI signals (SPI_CSB, SPI_CLK, SPI_SI, and SPI_SO) and one interrupt signal (SPI_INT). The SPI signals are muxed onto the UART signals, see Table 5. The CYW4339 can be configured to accept active-low or active-high polarity on the SPI_CSB chip-select signal. It can also be configured to drive an active-low or active-high SPI_INT interrupt signal. Bit ordering on the SPI_SI and SPI_SO data lines can be configured as either little-endian or big-endian.

Additionally, proprietary sleep mode and half-duplex handshaking is implemented between the SPI master and the CYW4339. The SPI_INT is required to negotiate the start of a transaction. The SPI interface does not require flow control in the middle of a payload. The FIFO is large enough to handle the largest packet size. Only the SPI master can stop the flow of bytes on the data lines, since it controls SPI_CSB and SPI_CLK. Flow control should be implemented in the higher layer protocols.

Table 5. SPI to UART Signal Mapping

SPI Signals	UART Signals
SPI_CLK	UART_CTS_N
SPI_CSB	UART_RTS_N
SPI_MISO	UART_RXD
SPI_MOSI	UART_TXD
SPI_INT	BT_HOST_WAKE

7.2 SPI/UART Transport Detection

The BT_HOST_WAKE (BT_GPIO1) pin is also used for BT transport detection. Transport detection occurs during the power-up sequence. Either UART or SPI transport operation is selected based on the following pin state:

- If the BT_HOST_WAKE (BT_GPIO1) pin is pulled low by an external pull-down during power-up, the SPI transport interface is selected.
- If the BT_HOST_WAKE (BT_GPIO1) pin is not pulled low externally during power-up, then the default internal pull-up is detected as a high and the UART transport interface is selected.

7.3 PCM Interface

The CYW4339 supports two independent PCM interfaces that share pins with the I^2S interfaces. The PCM Interface on the CYW4339 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW4339 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW4339.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.3.1 Slot Mapping

The CYW4339 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tri-states its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.3.2 Frame Synchronization

The CYW4339 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.3.3 Data Formatting

The CYW4339 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW4339 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

7.3.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The CYW4339 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.3.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

7.3.6 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 8. PCM Timing Diagram (Short Frame Sync, Master Mode)

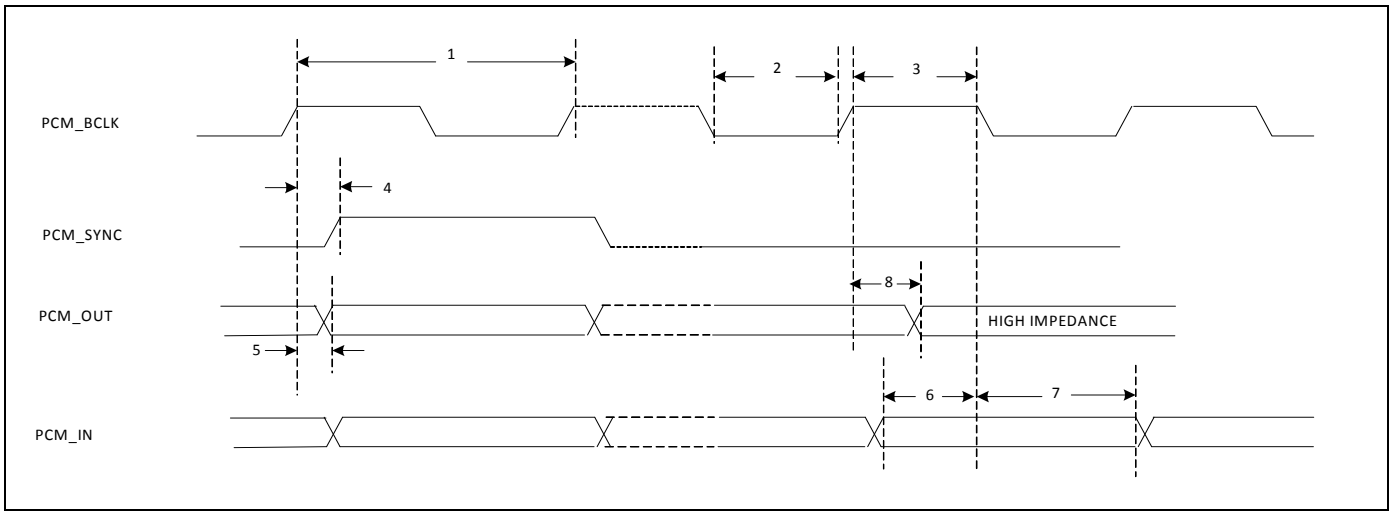


Table 6. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 9. PCM Timing Diagram (Short Frame Sync, Slave Mode)

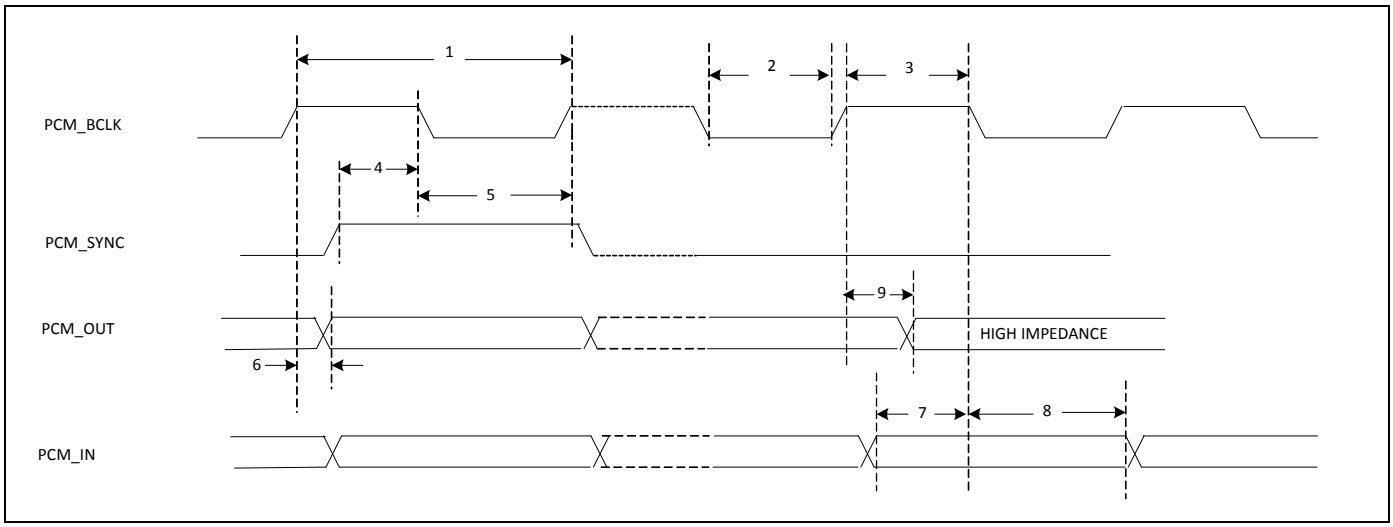


Table 7. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

Figure 10. PCM Timing Diagram (Long Frame Sync, Master Mode)

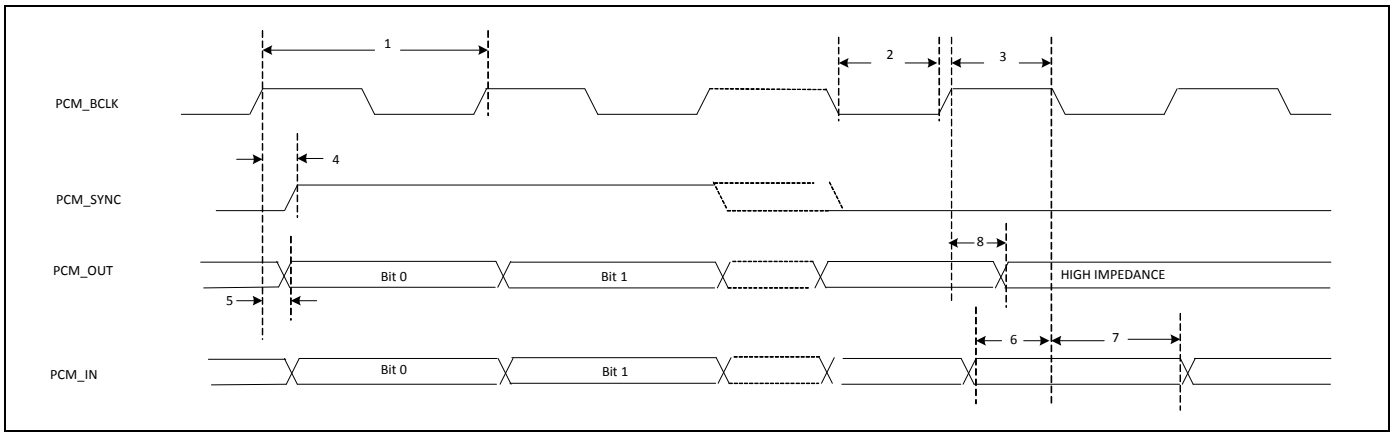


Table 8. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 11. PCM Timing Diagram (Long Frame Sync, Slave Mode)

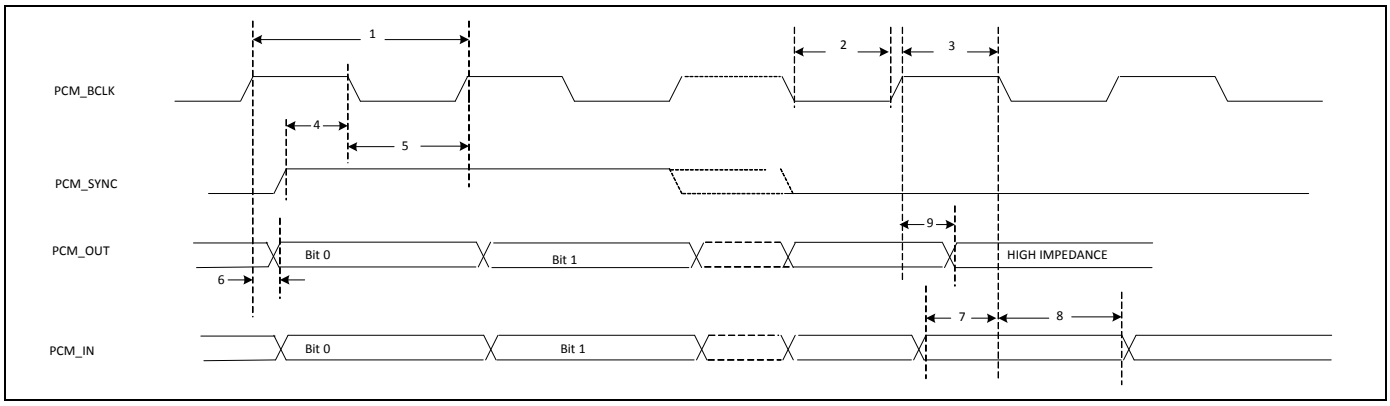


Table 9. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 12. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

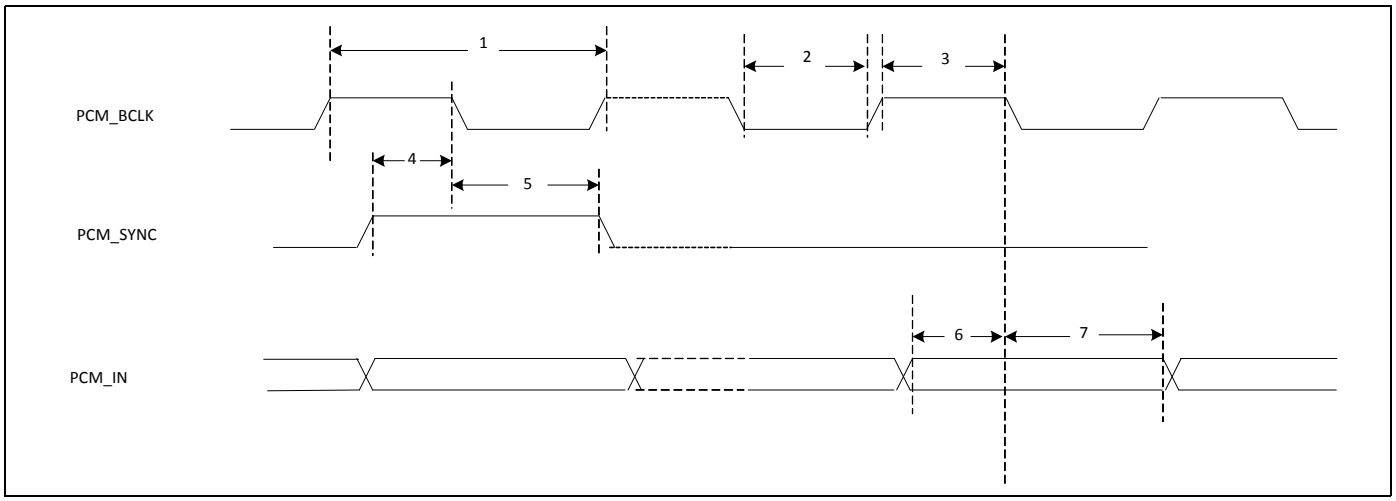


Table 10. PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 13. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

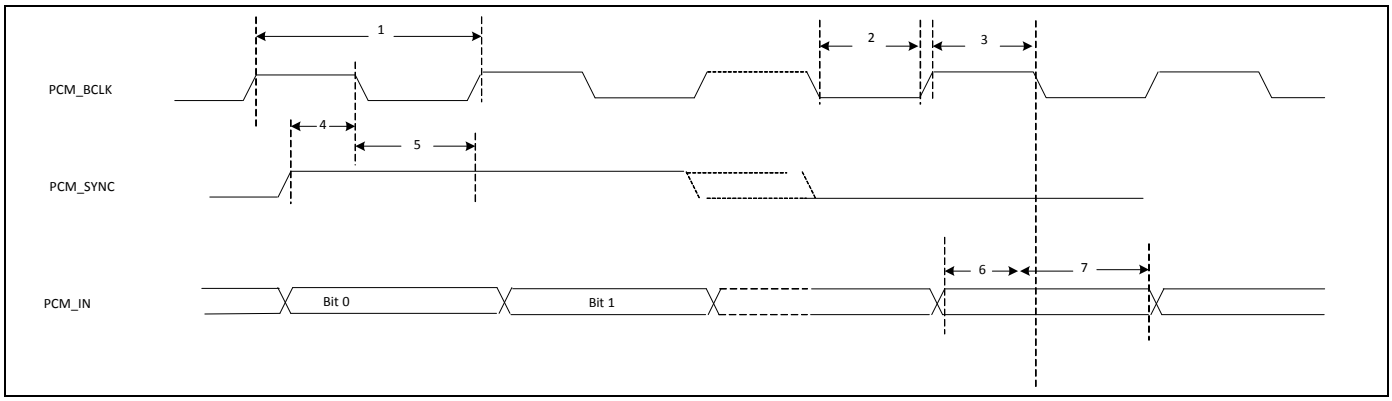


Table 11. PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

7.4 USB Interface

7.4.1 Features

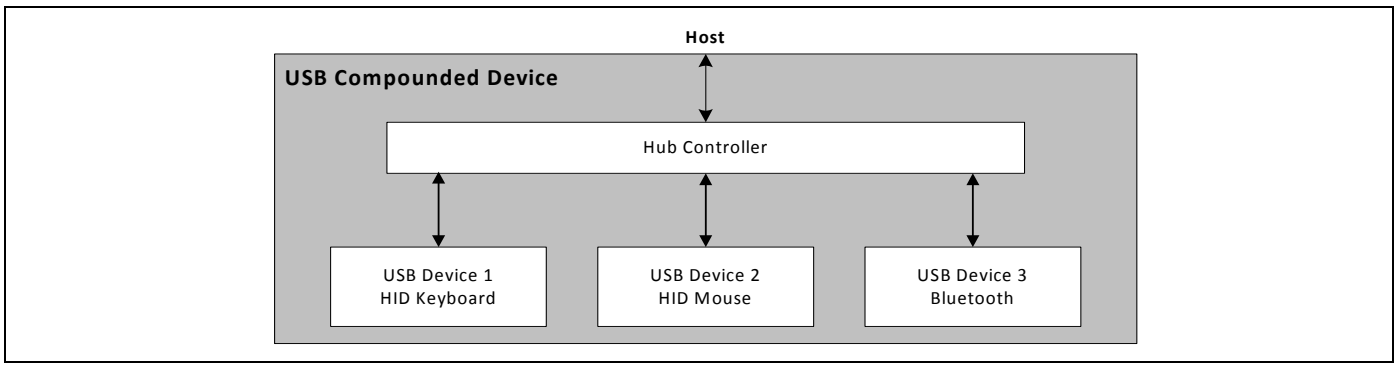
The following USB interface features are supported:

- USB Protocol, Revision 2.0, full-speed (12 Mbps) compliant including the hub
- Optional hub compound device with up to three device cores internal to device
- Bus or self-power, dynamic configuration for the hub
- Global and selective suspend and resume with remote wakeup
- Bluetooth HCI
- HID, DFU, UHE (proprietary method to emulate an HID device at system bootup)
- Integrated detach resistor

7.4.2 Operation

The CYW4339 can be configured to boot up as either a single USB peripheral or a USB hub with several USB peripherals attached. As a single peripheral, the host detects a single USB Bluetooth device. In hub mode, the host detects a hub with one to three of the ports already connected to USB devices (see Figure 14).

Figure 14. USB Compounded Device Configuration



Depending on the desired hub mode configuration, the CYW4339 can boot up showing the three ports connected to logical USB devices internal to the CYW4339: a generic Bluetooth device, a mouse, and a keyboard. In this mode, the mouse and keyboard are emulated devices, since they connect to real HID devices via a Bluetooth link. The Bluetooth link to these HID devices is hidden from the USB host. To the host, the mouse and/or keyboard appear to be directly connected to the USB port. This Broadcom proprietary architecture is called USB HID Emulation (UHE).

The USB device, configuration, and string descriptors are fully programmable, allowing manufacturers to customize the descriptors, including vendor and product IDs, the CYW4339 uses to identify itself on the USB port. To make custom USB descriptor information available at boot time, stored it in external NVRAM.

Despite the mode of operation (single peripheral or hub), the Bluetooth device is configured to include the following interfaces:

Interface 0	Contains a Control endpoint (Endpoint 0x00) for HCI commands, a Bulk In Endpoint (Endpoint 0x82) for receiving ACL data, a Bulk Out Endpoint (Endpoint 0x02) for transmitting ACL data, and an Interrupt Endpoint (Endpoint 0x81) for HCI events.
Interface 1	Contains Isochronous In and Out endpoints (Endpoints 0x83 and 0x03) for SCO traffic. Several alternate Interface 1 settings are available for reserving the proper bandwidth of isochronous data (depending on the application).
Interface 2	Contains Bulk In and Bulk Out endpoints (Endpoints 0x84 and 0x04) used for proprietary testing and debugging purposes. These endpoints can be ignored during normal operation.

7.4.3 USB Hub and UHE Support

The CYW4339 supports the USB hub and device model (USB, Revision 2.0, full-speed compliant). Optional mouse and keyboard devices utilize Broadcom's proprietary USB HID Emulation (UHE) architecture, which allows these devices appear as standalone HID devices even though connected through a Bluetooth link.

The presence of UHE devices requires the hub to be enabled. The CYW4339 cannot appear as a single keyboard or a single mouse device without the hub. Once either mouse or keyboard UHE device is enabled, the hub must also be enabled.

When the hub is enabled, the CYW4339 handles all standard USB functions for the following devices:

- HID keyboard
- HID mouse
- Bluetooth

All hub and device descriptors are firmware-programmable. This USB compound device configuration (see Figure 14) supports up to three downstream ports. This configuration can also be programmed to a single USB device core. The device automatically detects activity on the USB interface when connected. Therefore, no special configuration is needed to select HCI as the transport.

The hub's downstream port definition is as follows:

- Port 1 USB lite device core (for HID applications)
- Port 2 USB lite device core (for HID applications)
- Port 3 USB full device core (for Bluetooth applications)

When operating in hub mode, all three internal devices do not have to be enabled. Each internal USB device can be optionally enabled. The configuration record in NVRAM determines which devices are present.

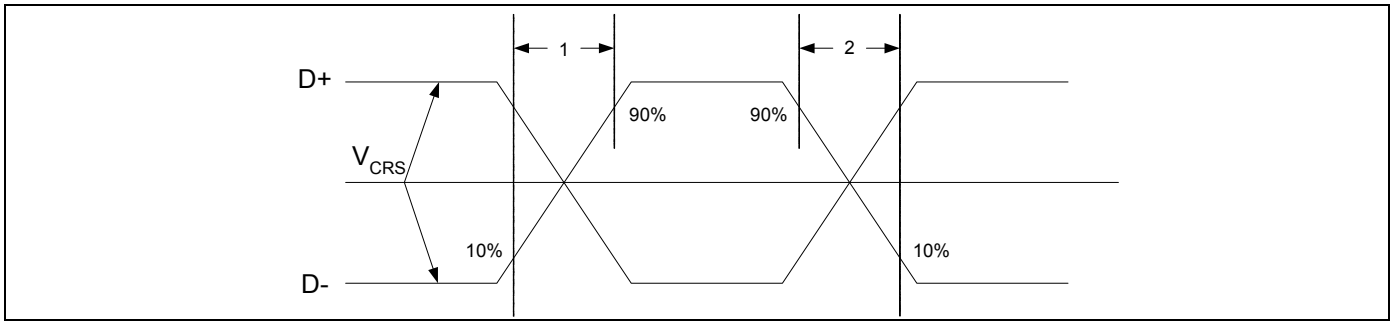
7.4.4 USB Full-Speed Timing

Table 12 shows timing specifications for the VDD_USB = 3.3V, V_{SS} = 0V, and T_A = 0°C to 85°C operating temperature range.

Table 12. USB Full-Speed Timing Specifications

Reference	Characteristics	Minimum	Maximum	Unit
1	Transition rise time	4	20	ns
2	Transition fall time	4	20	ns
3	Rise/fall timing matching	90	111	%
4	Full-speed data rate	12 – 0.25%	12 + 0.25%	Mb/s

Figure 15. USB Full-Speed Timing



7.5 UART Interface

The CYW4339 has a UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW4339 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW4339 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 13. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 16. UART Timing

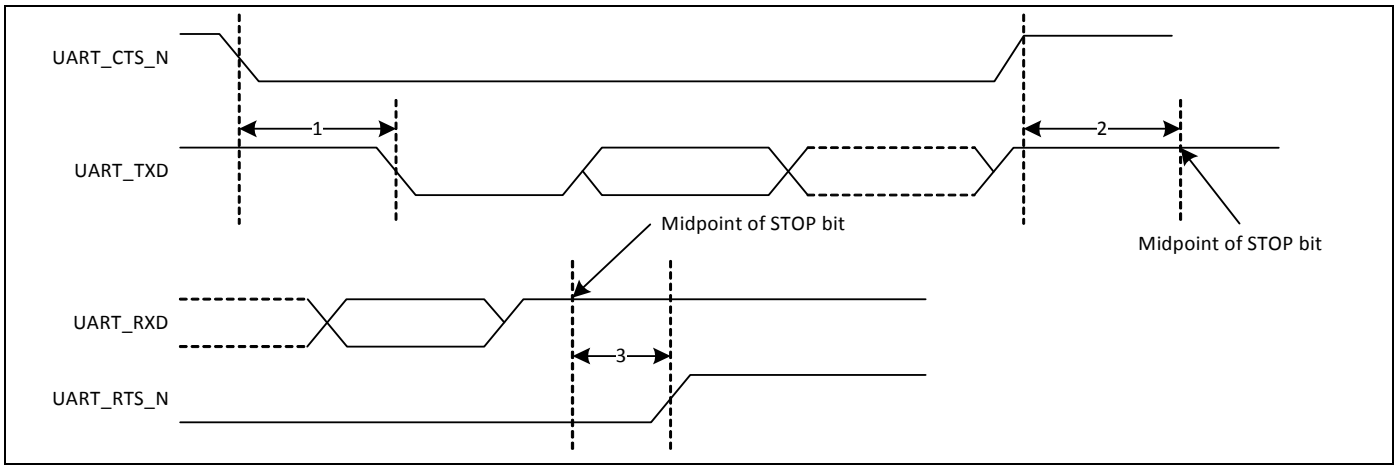


Table 14. UART Timing Specifications

Ref No.	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit period
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit period
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit period

7.6 I²S Interface

The CYW4339 supports I²S digital audio port for Bluetooth audio. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW4339 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

7.6.1 I²S Timing

Note: Timing values specified in Table 15 are relative to high and low threshold levels.

Table 15. Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–	–	–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

1. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.

2. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.

3. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.

4. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.

5. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

6. The data setup and hold time must not be less than the specified receiver setup and hold time.

Note: The time periods specified in Figure 17 and Figure 18 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 17. I²S Transmitter Timing

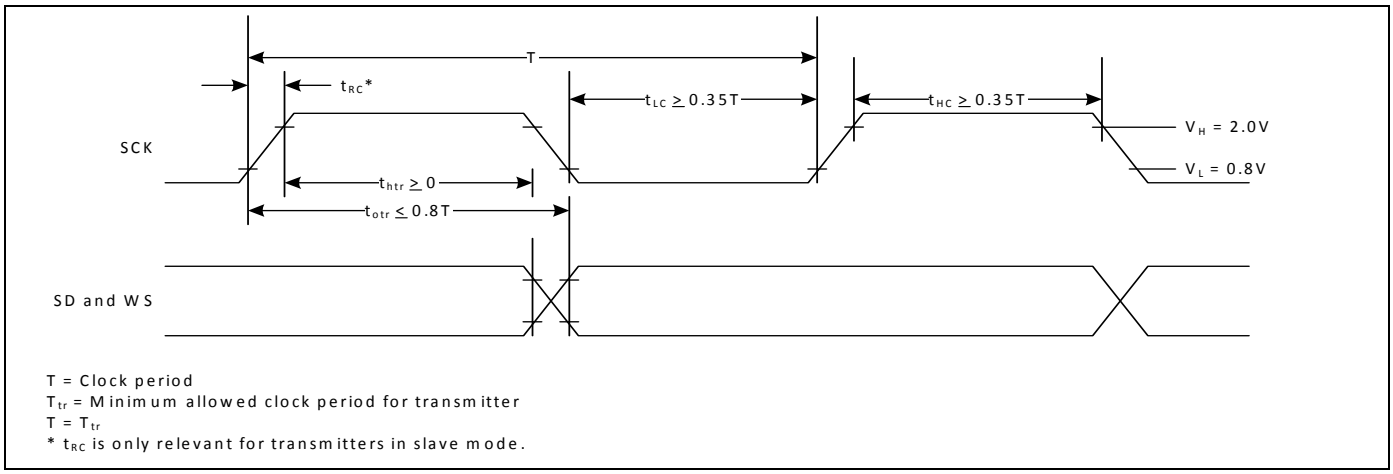
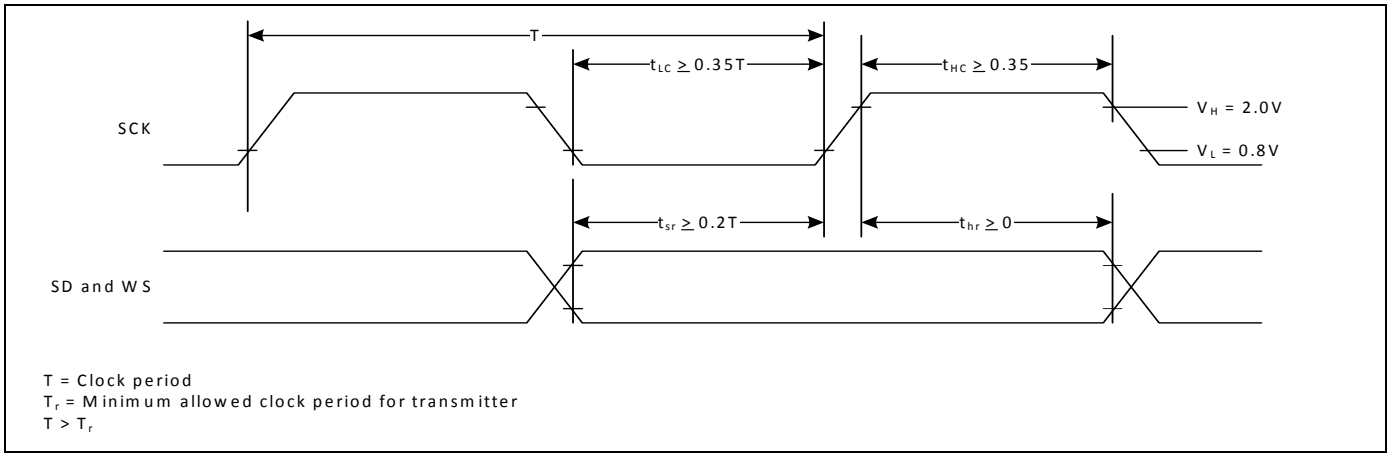


Figure 18. I²S Receiver Timing



8. WLAN Global Functions

8.1 WLAN CPU and Memory Subsystem

The CYW4339 WLAN section includes an integrated ARM Cortex-R4™ 32-bit processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering more than 30% performance gain over ARM7TDMI, the ARM Cortex-R4 implements the ARM v7-R architecture with support for the Thumb®-2 instruction set.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

Using multiple technologies to reduce cost, the ARM Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and System buses), and extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 768 KB SRAM and 640 KB ROM.

8.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Customer accessible OTP memory is 502 bytes.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP memory programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

8.3 GPIO Interface

The following number of general-purpose I/O (GPIO) pins are available on the WLAN section of the CYW4339 that can be used to connect to various external devices:

- FCBGA package – 12 GPIOs
- WLBGA package – 9 GPIOs
- WLCSP package – 16 GPIOs

Upon power up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions (see Table 26, “CYW4339 GPIO/SDIO Alternative Signal Functions,”).

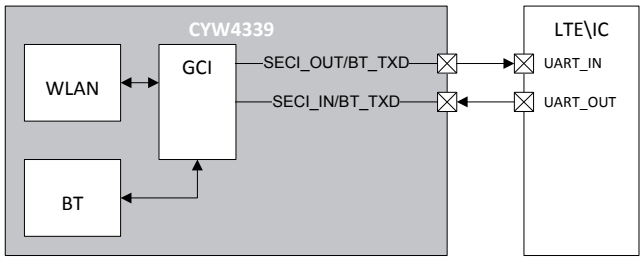
8.4 External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as GPS, WiMAX, LTE, or UWB, to manage wireless medium sharing for optimum performance.

Figure 19 shows the LTE coexistence interface. See Table 26, “CYW4339 GPIO/SDIO Alternative Signal Functions,” for details on multiplexed signals such as the GPIO pins.

See Table 13, “Example of Common Baud Rates,” for UART baud rates.

Figure 19. Broadcom GCI or BT-SIG Mode LTE Coexistence Interface for CYW4339



NOTES:

- SECI_OUT/BT_TXD and SECI_IN/BT_RXD, on the BCM4339, are multiplexed on the GPIOs.
- The 2-wire LTE coexistence interface is intended for future compatibility with the BT SIG 2-wire interface that is being standardized for Core 4.1.
- ORing to generate ISM_RX_PRIORITY for ERCX_TXCONF or BT_RX_PRIORITY is achieved by setting the GPIO mask registers appropriately.

8.5 UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins (see Table 26, “CYW4339 GPIO/SDIO Alternative Signal Functions,”). Provided primarily for debugging during development, this UART enables the CYW4339 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.6 JTAG Interface

The CYW4339 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bringup. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

See Table 26, “CYW4339 GPIO/SDIO Alternative Signal Functions,” for JTAG pin assignments.

8.7 SPROM Interface (FCBGA Package only)

For use only with the PCIe Interface in the FCBGA package, various hardware configuration parameters may be stored in an external SPROM instead of the OTP. The SPROM is read by system software after device reset. In addition, depending on the board design, customer-specific parameters may be stored in SPROM.

The four SPROM control signals —SPROM_CS, SPROM_CLK, SPROM_DIN, and SPROM_DOUT are multiplexed on the SDIO interface (see Table 26, “CYW4339 GPIO/SDIO Alternative Signal Functions,” for additional details). By default, the SPROM interface supports 2 kbit serial SPROMs, and it can also support 4 kbit and 16 kbit serial SPROMs by using the appropriate strapping option.

9. WLAN Host Interfaces

9.1 SDIO v3.0

The CYW4339 WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 100 MHz (1.8V signaling).
- SDR104: SDR up to 208 MHz (1.8V signaling).
- DDR50: DDR up to 50 MHz (1.8V signaling).

Note: The CYW4339 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options. Refer to Table 19 WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max. BlockSize/ByteCount = 512B)

9.1.1 SDIO Pins

Table 16. SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 20. Signal Connections to SDIO Host (SD 4-Bit Mode)

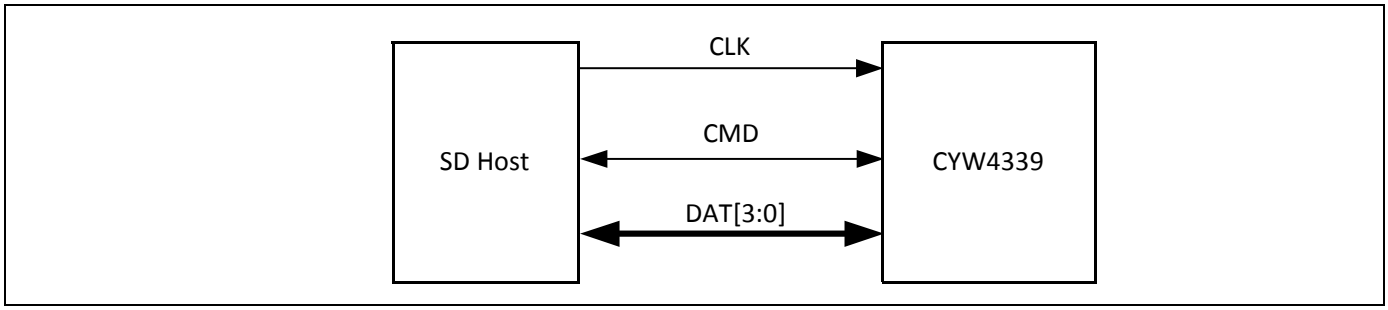
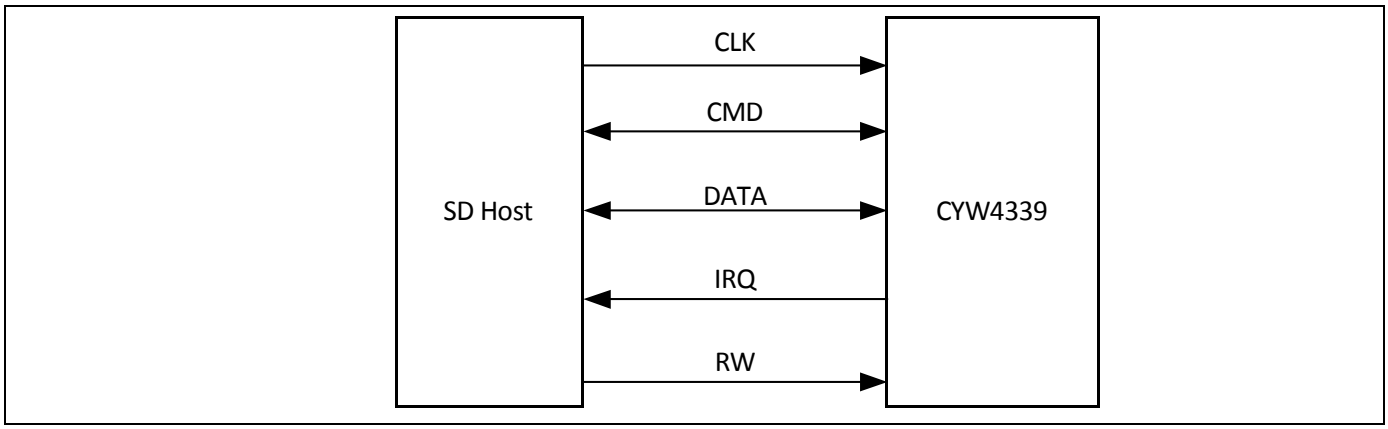


Figure 21. Signal Connections to SDIO Host (SD 1-Bit Mode)



Note: Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

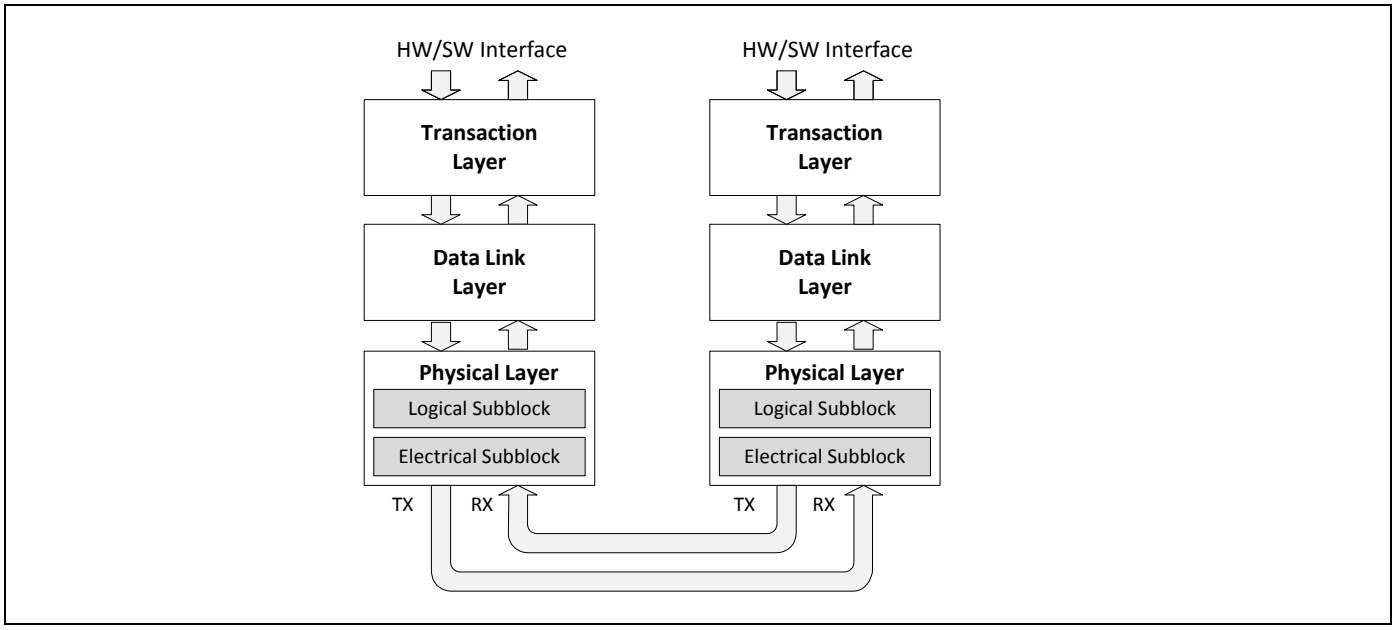
9.2 PCI Express Interface (FCBGA Package Only)

The PCI Express (PCIe™) core on the CYW4339 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification (*revision 3.0 compliant Gen1 interface). This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 22. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW4339 device. The transmit side processes outbound packets while the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 22. PCI Express Layer Model



9.2.1 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW4339 device, delivering new levels of performance and features. The upper layer of the PCIe is the Transaction Layer. The Transaction layer is primarily responsible for assembly and disassembly of Transaction Layer Packets (TLPs). TLP structure contains header, data payload, and End-to-End CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

9.2.2 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

Data Link Layer Packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

9.2.3 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW4339 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

9.2.4 Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

9.2.5 Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

9.2.6 8B/10B Encoder/Decoder

The PCIe core on the CYW4339 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the twelve Special Symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. Special Symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

9.2.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

9.2.8 Electrical Subblock

The high-speed signals utilize the Common Mode Logic (CML) signaling interface with on-chip termination and de-emphasis for best-in-class signal integrity. A de-emphasis technique is employed to reduce the effects of Intersymbol Interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable Bit-Error Rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

9.2.9 Configuration Space

The PCIe function in the CYW4339 implements the configuration space as defined in the *PCI Express Base Specification* (revision 3.0 compliant Gen1 interface).

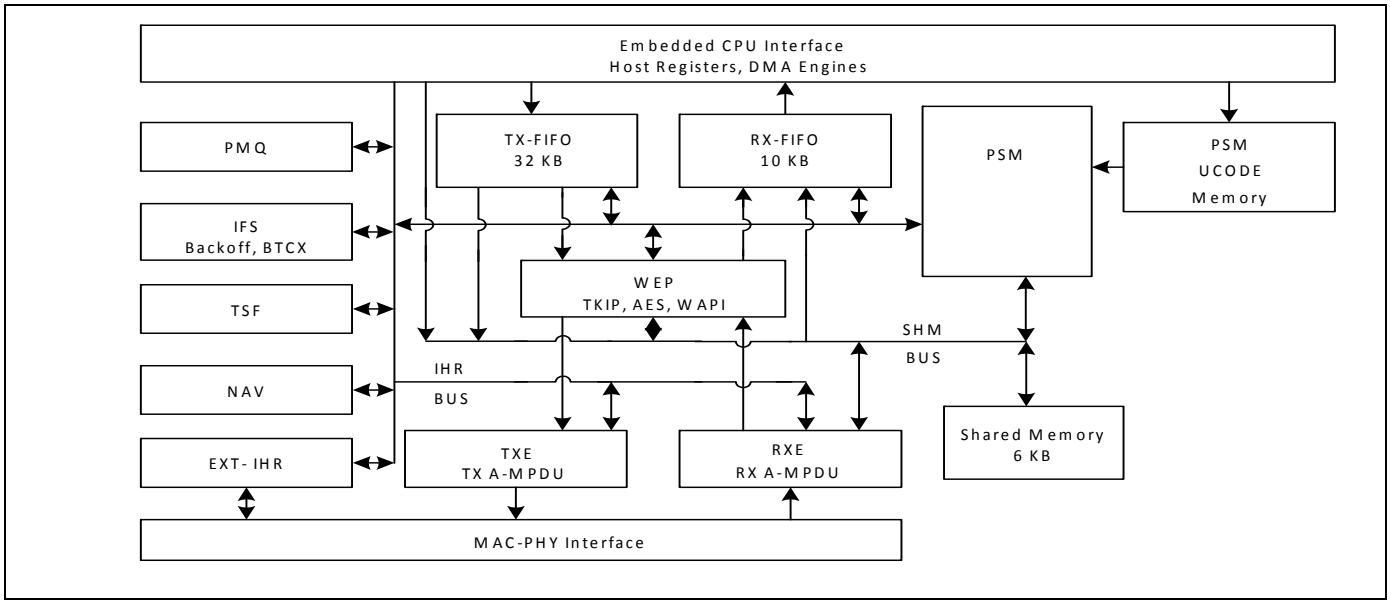
10. Wireless LAN MAC and PHY

10.1 IEEE 802.11ac MAC

The CYW4339 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 23.

The following sections provide an overview of the important modules in the MAC.

Figure 23. WLAN MAC Architecture



The CYW4339 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ac features
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

10.1.1 PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch-pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

10.1.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

10.1.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

10.1.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

10.1.5 IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

10.1.6 TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

10.1.7 NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

10.2 IEEE 802.11ac PHY

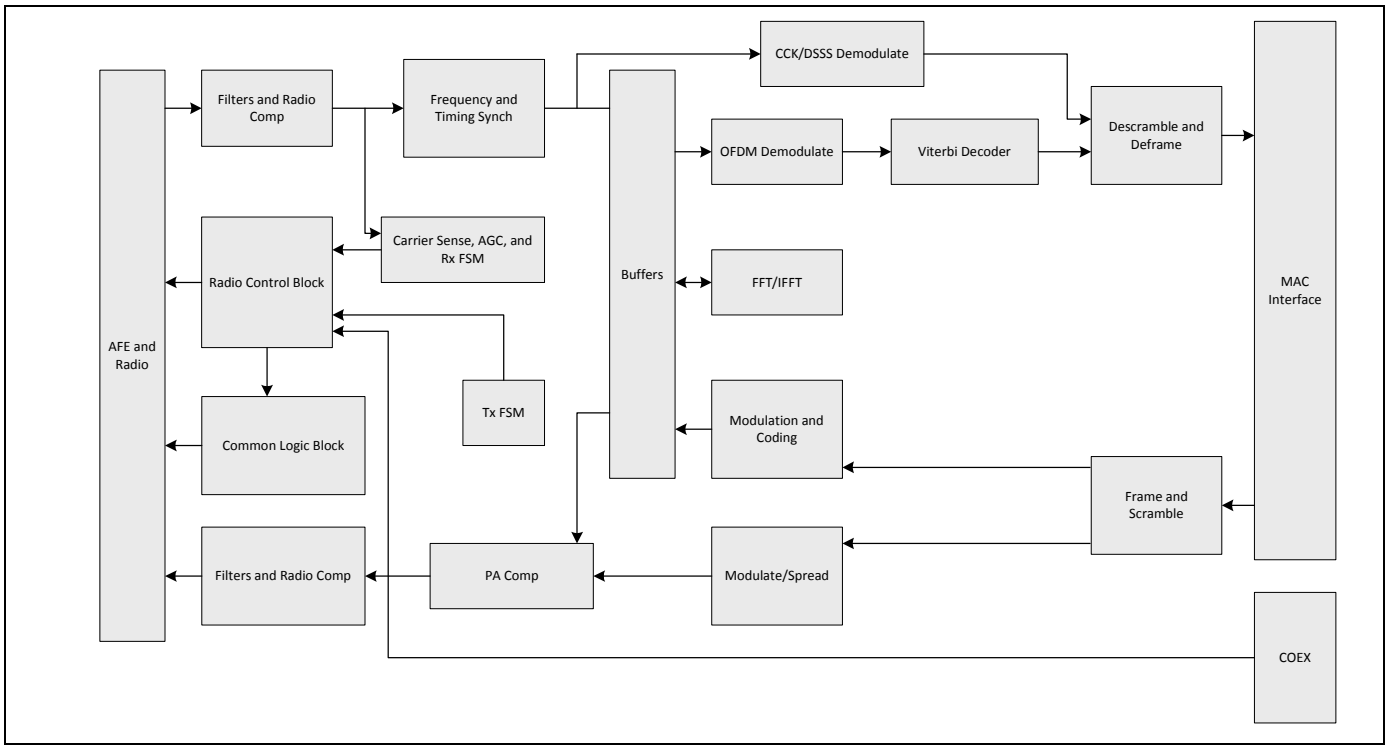
The CYW4339 WLAN Digital PHY is designed to comply with IEEE 802.11ac and IEEE 802.11a/b/g/n single-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 433.3 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous RX-RX.

The key PHY features include:

- Programmable data rates from MCS0–9 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac
- Supports Optional Short GI mode in TX and RX
- TX and RX LDPC for improved range and power efficiency
- Supports optional space-time block code (STBC) receive of two space-time streams for improved throughput and range in fading channel environments.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet RX antenna diversity
- Available per-packet channel quality and signal strength measurements
- Designed to meet FCC and other worldwide regulatory requirements

Figure 24. WLAN PHY Block Diagram



11. WLAN Radio Subsystem

The CYW4339 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Ten RF control signals are available to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

A block diagram of the radio subsystem is shown in Figure 25. Note that integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

11.1 Receiver Path

The CYW4339 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN receivers, while the 5 GHz receive path has a dedicated on-chip LNA. Control signals are available that can support the use of optional LNAs for each band, which can increase the receive sensitivity by several dB.

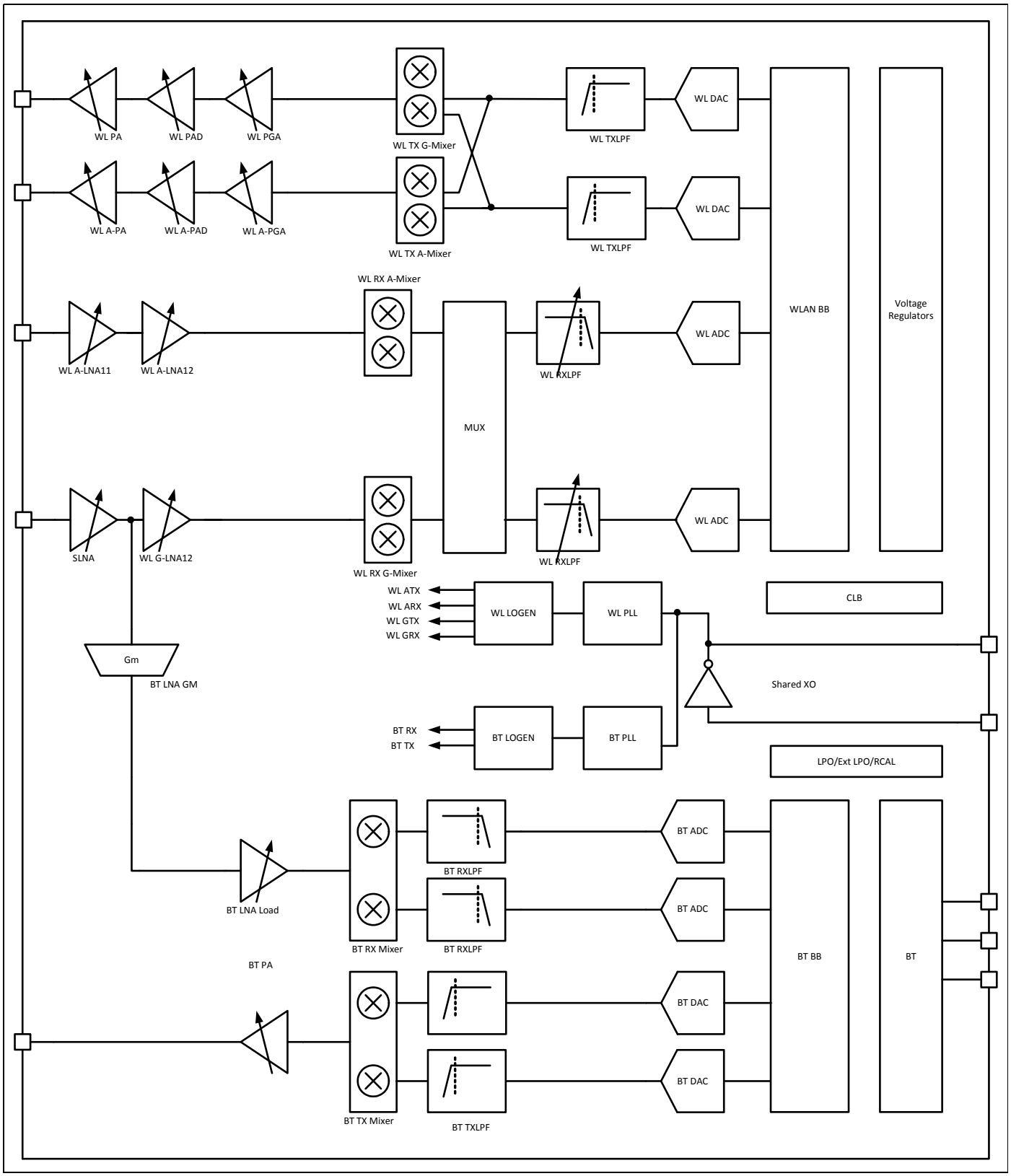
11.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated. As an option, external PAs can be used for even higher output power, in which case the closed-loop output power control is provided by means of a-band and g-band TSSI inputs from external power detectors.

11.3 Calibration

The CYW4339 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

Figure 25. Radio Functional Block Diagram



12. Pinout and Signal Descriptions

12.1 Ball Maps

Figure 26 shows the FCFBGA ball map. Figure 27 shows the WLBGA ball map. Figure 28 shows the WLCSP bump map.

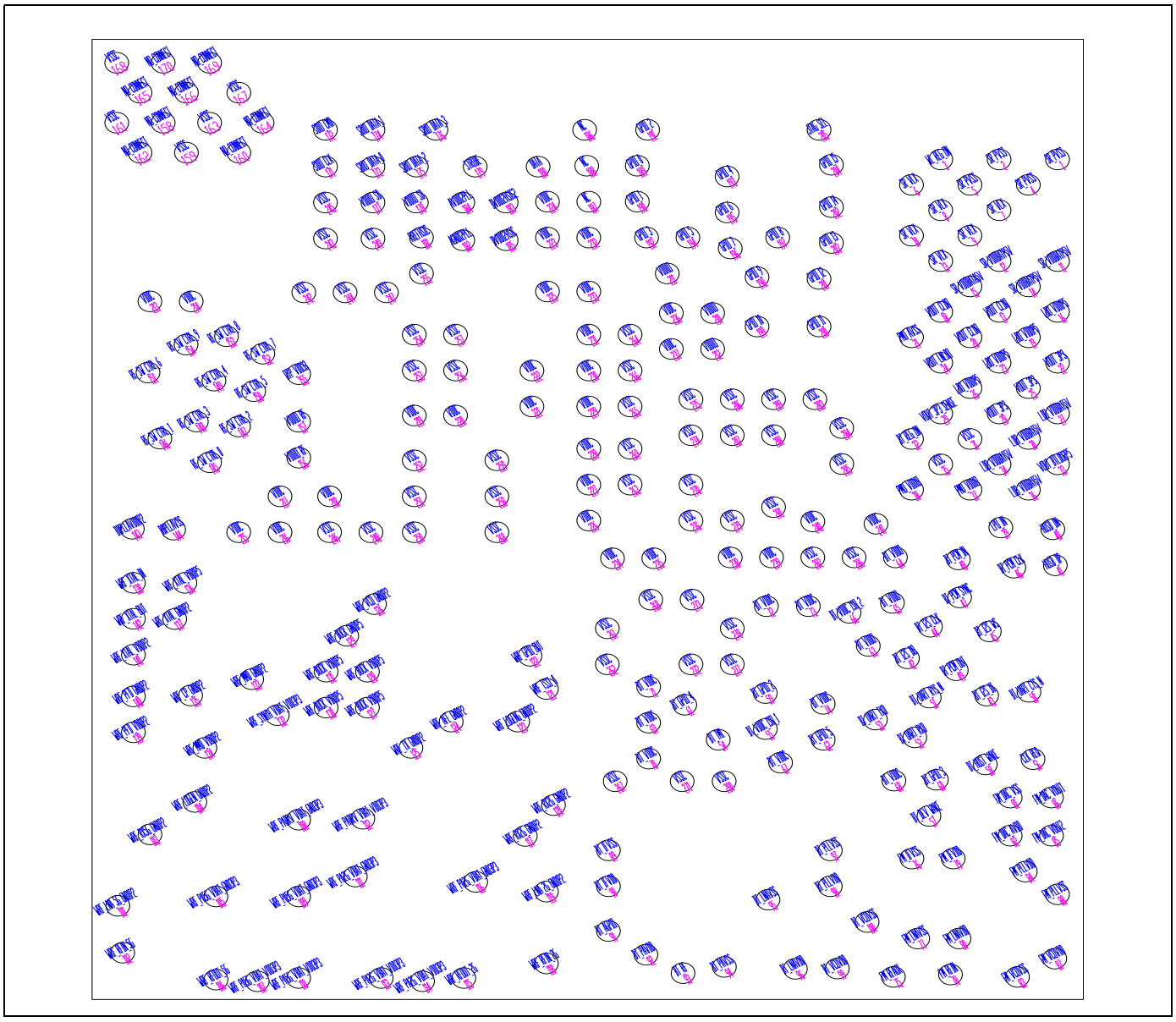
Figure 26. 160-Ball FCFBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A		SR_VLX	GPIO_13		GPIO_5		GPIO_3		VDDIO_SD		SDIO_DATA_1							PAD_REFCLKN	PCIE_CLKREQ_L	A
B	SR_VDDBATP5V	SR_VLX	VDDIO		GPIO_4		GPIO_7		SDIO_DATA_3		SDIO_CLK		PAD_RDN0	PAD_TDP0	PAD_TDN0	PERST_L		PAD_REFCLKP	PCI_PME_L	B
C	SR_VDDBATP5V	SR_VDDBATP5V	SR_VDDBATA5V		BT_REG_ON	JTAG_SEL	GPIO_6	GPIO_2	SDIO_DATA_2	SDIO_DATA_0	SDIO_CMD		PAD_RDP0			GPIO_1			BT_GPIO_4	C
D	SR_PVSS				WL_REG_ON	GPIO_15		GPIO_14	GPIO_0				PCIE_VSS			PCIE_VSS		PAD_PLL_AVDD1P2	PAD_AVDD1P2	D
E	SR_PVSS	SR_PVSS						GPIO_8		VDDC	VDDC									E
F	LDO_VDD1P5	LDO_VDD1P5			NO CONNECT															F
G		VOUT_CLDO			NO CONNECT									VDDC		RF_SW_CTRL_8	RF_SW_CTRL_5	RF_SW_CTRL_6	RF_SW_CTRL_3	G
H	VOUT_3P3	VOUT_3P3_SENSE						PMU_AVSS	VSSC	VSSC	VSSC	VSSC		VDDC		RF_SW_CTRL_9	RF_SW_CTRL_4			H
J		VOUT_BTLDO2P5					LPO_IN	VSSC				VSSC				RF_SW_CTRL_7	RF_SW_CTRL_1	RF_SW_CTRL_2	RF_SW_CTRL_0	J
K		VOUT_LNLDO					VDDC	VSSC				VSSC					VDDIO_RF			K
L	LDO_VDDBATSV	PMU_VDDIO	BT_VDDIO				BT_VDDC	VSSC			VSSC	WRF_VCO_GND1P2	BBPLLAVSS		WRF_BUCK_VDD1P5			OTP_VDD33	BBPLLAVDD	L
M			BT_DEV_WAKE				BT_VDDC	VSSC	VSSC	VSSC	WRF_LOGENG_GND1P2	WRF_BUCK_GND1P5			WRF_XTAL_GND1P2					M
N	HUSB_DN	HUSB_DP	BT_SF_MOSI												WRF_CP_GND1P2				WRF_XTAL_VDD1P5	N
P			BT_SF_CLK				BT_VCOVSS				WRF_RX2G_GND1P2			WRF_MMD_GND1P2	WRF_PFD_GND1P2			WRF_XTAL_GND1P2	WRF_XTAL_IN	P
R	BT_SF_CSN	BT_SF_MISO	BT_I2S_CLK				BT_PLLVSS	BT_LNAVSS	BT_IFVSS		WRF_PA2G_VBAT_GND3P3	WRF_AFE_GND1P2	WRF_TX_GND1P2	WRF_PADRV_VBATGND3P3	WRF_LOGEN_GND1P2				WRF_XTAL_OUT	R
T			BT_UART_CTS_N					BT_PAVSS		WRF_LNA_2G_GND1P2					WRF_LNA_5G_GND1P2	WRF_RX5G_GND1P2		WRF_PFD_VDD1P2	WRF_XTAL_VDD1P2	T
U	BT_I2S_WS	BT_I2S_DO	BT_I2S_DI												WRF_PA5G_VBAT_GND3P3			WRF_MMD_VDD1P2		U
V	BT_UART_RTS_N		BT_HOST_WAKE		BT_VCOVDD	BT_PLLVDD		BT_PAVDD		WRF_GPIO_OUT	WRF_TSSI_A	WRF_PA2G_VBAT_GND3P3	WRF_PA2G_VBAT_VDD3P3	WRF_PADRV_VBAT_VDD3P3	WRF_PA5G_VBAT_VDD3P3	WRF_PA5G_VBAT_GND3P3			WRF_SYNTH_VBAT_VDD3P3	V
W	BT_UART_RXD	BT_UART_TXD	CLK_REQ		BT_LNAVDD	BT_IFVDD		BT_RF		WRF_RFIN_2G		WRF_RFOUT_2G				WRF_RFOUT_5G		WRF_RFIN_5G	NO CONNECT	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Figure 27. 145-Ball WLBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	
A		NO CONNECT	NO CONNECT	NO CONNECT		NO CONNECT	NO CONNECT		NO CONNECT	NO CONNECT	NO CONNECT		A
B	SR_PVSS	SR_VLX	WL_REG_ON	LPO_IN	GPIO_3	GPIO_0	HSIC_DATA	HSIC_STROBE	RREFHSIC	SDIO_DATA_0	SDIO_CLK	SDIO_CMD	B
C	SR_VDDBATP5V	SR_VDDBATA5V	PMU_AVSS	GPIO_6	GPIO_4	GPIO_1	WL_VDDC	HSIC_AVDD12PLL	HSIC_DVDD12	SDIO_DATA_1	SDIO_DATA_3	WL_VDDC	C
D	LDO_VDD1P5	VOUT_CLDO	BT_REG_ON	GPIO_7	GPIO_5	GPIO_2	VSSC	HSIC_AGNDPLL	VDDIO_SD	SDIO_DATA_2	VSSC	RF_SW_CTRL_4	D
E	VOUT_3P3	VOUT_LNLDO	VSSC		JTAG_SEL	BT_UART_CTS	VDDIO_RF	VSSC		RF_SW_CTRL_8	RF_SW_CTRL_3	RF_SW_CTRL_2	E
F	VOUT_BTLDO2P5	LDO_VDDBAT5V	VDDIO		RF_SW_CTRL_9	BT_UART_RTS	BT_UART_TXD	RF_SW_CTRL_5			RF_SW_CTRL_1	RF_SW_CTRL_0	F
G	BT_PCM_IN	BT_PCM_CLK		WL_VDDC	WL_VDDC	BT_UART_RXD	RF_SW_CTRL_7	WL_VDDC		BBPLL_AVS	WRF_XTAL_GND1P2	BBPLL_AVDD1P2	G
H	GPIO_8	BT_PCM_SYNC	CLK_REQ	BT_VDDIO	BT_VDDC	BT_I2S_WS	WRF_GPIO_OUT	WRF_WL_LNLDOIN_VDD1P5	RF_SW_CTRL_6	WRF_VCO_GND	WRF_XTAL_VDD1P5	WRF_XTAL_IN	H
J	FM_AUDIOVDD1P2	BT_HOST_WAKE	BT_PCM_OUT	BT_VDDC	VSSC	BT_I2S_CLK	WRF_TSSI_A	WRF_BUCK_GND1P5	WRF_MMD_GND1P2	WRF_PFD_GND1P2	WRF_CP_GND	WRF_XTAL_OUT	J
K	FM_AOUT1	FM_AUDIOVSS	BT_DEV_WAKE	VSSC	BT_I2S_DI	BT_I2S_DO	WRF_AFE_GND1P2	WRF_LO_GND1P2_2	WRF_SYNTH_VBAT_VDD3P3	WRF_MMD_VDD1P2	WRF_PFD_VDD1P2	WRF_XTAL_VDD1P2	K
L	FM_AOUT2	FM_PLLVDD1P2	FM_PLLVSS	BT_IFVDD1P2	BT_PLLVSS	BT_IFVSS	WRF_RX2G_GND1P2	WRF_TX_GND1P2	WRF_PADRV_VBAT_VDD3P3	WRF_PADRV_VBAT_GND3P3	WRF_LO_GND1P2_2	WRF_RX5G_GND1P2	L
M	FM_VCOVSS	FM_LNAVSS	BT_VCOVSS	BT_PLLVDD1P2	BT_PAVSS	BT_AGPIO	WRF_LNA_2G_GND1P2	WRF_PA_VBAT_GND3P3_4	WRF_PA_VBAT_GND3P3_3	WRF_PA_VBAT_GND3P3_2	WRF_PA_VBAT_GND3P3_1	WRF_LNA_5G_GND1P2	M
N	FM_LNAVCOVDD1P2	FM_RFIN	BT_VCOVDD1P2	BT_LNAVDD1P2	BT_RF	BT_PAVDD2P5	WRF_RFIN_2G	WRF_RFOUT_2G	WRF_PA2G_VBAT_VDD3P3	WRF_PA5G_VBAT_VDD3P3	WRF_RFOUT_5G	WRF_RFIN_5G	N
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 28. 286-Bump WLCSP (Bottom View)



12.2 Pin Lists

Table 17 contains the 286-bump WLCSP coordinates.

Table 17. 286-Bump WLCSP Coordinates

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
1	SR_PVSS	2275.005	2003.355	–2275.005	2003.355
2	SR_PVSS	1992.162	2003.355	–1992.162	2003.355
3	WL_REG_ON	1709.319	2003.355	–1709.319	2003.355
4	SR_PVSS	2133.584	1861.934	–2133.584	1861.934
5	SR_PVSS	1850.741	1861.934	–1850.741	1861.934
6	SR_VLX	1567.898	1861.934	–1567.898	1861.934
7	SR_VLX	1992.162	1720.512	–1992.162	1720.512
8	SR_VLX	1709.319	1720.512	–1709.319	1720.512
9	SR_VLX	1850.741	1579.091	–1850.741	1579.091
10	SR_VLX	1567.898	1579.091	–1567.898	1579.091
11	SR_VDDBATP5V	2275.005	1437.669	–2275.005	1437.669
12	SR_VDDBATP5V	1992.162	1437.669	–1992.162	1437.669
13	SR_VLX	1709.319	1437.669	–1709.319	1437.669
14	SR_VDDBATP5V	2133.584	1296.248	–2133.584	1296.248
15	SR_VDDBATA5V	1850.741	1296.248	–1850.741	1296.248
16	LDO_VDD1P5	2275.005	1154.826	–2275.005	1154.826
17	VOUT_CLDO	1992.162	1154.826	–1992.162	1154.826
18	VOUT_CLDO	1709.319	1154.826	–1709.319	1154.826
19	LDO_VDD1P5	2133.584	1013.405	–2133.584	1013.405
20	VOUT_CLDO	1850.741	1013.405	–1850.741	1013.405
21	PMU_AVSS	1567.898	1013.405	–1567.898	1013.405
22	VOUT_3P3	2275.005	871.983	–2275.005	871.983
23	LDO_VDD1P5	1992.162	871.983	–1992.162	871.983
24	VOUT_LNLDO	1709.319	871.983	–1709.319	871.983
25	VOUT_3P3	2133.584	730.562	–2133.584	730.562
26	LDO_VDD1P5	1850.741	730.562	–1850.741	730.562
27	LDO_VDDBAT5V	2275.005	589.140	–2275.005	589.140
28	VOUT_3P3	1992.162	589.140	–1992.162	589.140
29	VOUT_3P3_SENSE	1709.319	589.140	–1709.319	589.140
30	LDO_VDDBAT5V	2133.584	447.719	–2133.584	447.719
31	VSSC	1850.741	447.719	–1850.741	447.719
32	BT_REG_ON	1567.898	447.719	–1567.898	447.719
33	VOUT_BTLDO2P5	2275.005	306.297	–2275.005	306.297
34	LDO_VDDBAT5V	1992.162	306.297	–1992.162	306.297
35	VSSC	1709.319	306.297	–1709.319	306.297

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
36	LDO_VDDBAT5V	2133.584	164.876	–2133.584	164.876
37	PMU_VDDIO	1850.741	164.876	–1850.741	164.876
38	PMU_VDDIO	1567.898	164.876	–1567.898	164.876
39	LPO_IN	2000.397	–45.054	–2000.397	–45.054
40	HUSB_DN	2252.010	–55.251	–2252.010	–55.251
41	HUSB_DP	2264.169	–255.429	–2264.169	–255.429
42	BT_I2S_DO	1548.201	–773.253	–1548.201	–773.253
43	BT_I2S_DI	1931.412	–980.847	–1931.412	–980.847
44	BT_I2S_CLK	1659.396	–597.546	–1659.396	–597.546
45	BT_I2S_WS	1944.471	–623.367	–1944.471	–623.367
46	BT_PCM_CLK	2063.397	–268.848	–2063.397	–268.848
47	BT_PCM_SYNC	1800.498	–434.448	–1800.498	–434.448
48	BT_PCM_IN	1794.801	–223.146	–1794.801	–223.146
49	BT_PCM_OUT	1784.397	–839.853	–1784.397	–839.853
50	BT_UART_CTS_N	2136.414	–959.733	–2136.414	–959.733
51	BT_UART_RTS_N	1653.744	–991.854	–1653.744	–991.854
52	BT_UART_RXD	1583.904	–1213.488	–1583.904	–1213.488
53	BT_UART_TXD	1393.104	–1114.101	–1393.104	–1114.101
54	BT_TM1	632.001	–1226.646	–632.001	–1226.646
55	BT_VDDC_ISO_1	859.998	–1166.652	–859.998	–1166.652
56	CLK_REQ	2156.196	–1334.853	–2156.196	–1334.853
57	BT_DEV_WAKE	1652.097	–1650.546	–1652.097	–1650.546
58	BT_HOST_WAKE	1925.202	–1363.752	–1925.202	–1363.752
59	BT_GPIO_2	859.998	–966.654	–859.998	–966.654
60	BT_GPIO_3	1688.097	–1449.099	–1688.097	–1449.099
61	BT_GPIO_4	470.001	–1031.652	–470.001	–1031.652
62	BT_GPIO_5	1139.997	–1226.646	–1139.997	–1226.646
63	BT_VDDIO	1358.481	–704.151	–1358.481	–704.151
64	BT_VDDIO	1489.998	–211.653	–1489.998	–211.653
65	BT_VDDIO	1475.499	–464.652	–1475.499	–464.652
66	BT_VDDC_ISO_2	1265.574	–519.930	–1265.574	–519.930
67	BT_VDDC	933.699	–1354.050	–933.699	–1354.050
68	BT_VDDC	1482.501	–1453.950	–1482.501	–1453.950
69	BT_VDDC	294.996	–1131.651	–294.996	–1131.651
70	BT_VDDC	294.996	–1331.649	–294.996	–1331.649
71	BT_VDDC	294.996	–931.653	–294.996	–931.653
72	BT_VDDC	864.903	–482.949	–864.903	–482.949
73	BT_VDDC	1067.997	–482.949	–1067.997	–482.949

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
74	BT_VDDC	1139.997	–1026.648	–1139.997	–1026.648
75	FM_RFAUX	1479.864	–2546.550	–1479.864	–2546.550
76	FM_IFVSS	1569.797	–1888.101	–1569.797	–1888.101
77	FM_LNAVSS	1597.593	–2333.169	–1597.593	–2333.169
78	FM_RFIN	1756.686	–2533.167	–1756.686	–2533.167
79	FM_IFVDD	1769.795	–1888.101	–1769.795	–1888.101
80	FM_LNAVDD	1797.591	–2333.169	–1797.591	–2333.169
81	FM_DAC_VSS	2045.451	–1548.549	–2045.451	–1548.549
82	FM_DAC_AVDD	2045.451	–1760.319	–2045.451	–1760.319
83	FM_VCOVSS	2080.781	–2546.550	–2080.781	–2546.550
84	FM_PLLVDD	2118.860	–1960.317	–2118.860	–1960.317
85	FM_DAC_VOUT2	2245.449	–1760.319	–2245.449	–1760.319
86	FM_DAC_VOUT1	2245.449	–1548.549	–2245.449	–1548.549
87	FM_VCOVDD	2261.469	–2444.675	–2261.469	–2444.675
88	FM_PLLVSS	2274.852	–2086.889	–2274.852	–2086.889
89	BT_IFVSS	99.975	–1842.066	–99.975	–1842.066
90	BT_IFVDD	99.975	–2042.064	–99.975	–2042.064
91	BT_AGPIO	99.975	–2291.099	–99.975	–2291.099
92	BT_PAVDD	281.860	–2422.625	–281.860	–2422.625
93	BT_RF	461.505	–2525.544	–461.505	–2525.544
94	BT_PAVSS	661.503	–2491.097	–661.503	–2491.097
95	BT_LNAVSS	873.183	–2116.746	–873.183	–2116.746
96	BT_LNAVDD	1005.281	–2501.330	–1005.281	–2501.330
97	BT_PLLVSS	1174.454	–1842.066	–1174.454	–1842.066
98	BT_PLLVDD	1174.454	–2042.064	–1174.454	–2042.064
99	BT_VCOVDD	1208.352	–2500.155	–1208.352	–2500.155
100	BT_VCOVSS	1352.595	–2240.766	–1352.595	–2240.766
101	WRF_LNA_5G_GND1P2	–2275.490	–2150.537	2275.490	–2150.537
102	WRF_RFIN_5G	–2251.986	–2411.789	2251.986	–2411.789
103	WRF_RX5G_GND1P2	–2119.686	–1753.146	2119.686	–1753.146
104	WRF_LOGEN_GND1P2	–1902.494	–1572.417	1902.494	–1572.417
105	WRF_PA5G_VBAT_GND3P3	–1800.006	–2098.656	1800.006	–2098.656
106	WRF_RFOUT_5G	–1800.006	–2561.652	1800.006	–2561.652
107	WRF_PA5G_VBAT_VDD3P3	–1600.008	–2570.652	1600.008	–2570.652
108	WRF_PADRV_VBAT_GND3P3	–1400.010	–1671.660	1400.010	–1671.660
109	WRF_PA5G_VBAT_GND3P3	–1400.010	–2098.656	1400.010	–2098.656
110	WRF_PA5G_VBAT_VDD3P3	–1400.010	–2552.652	1400.010	–2552.652
111	WRF_PA2G_VBAT_GND3P3	–1125.249	–1987.776	1125.249	–1987.776

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
112	WRF_PADRV_VBAT_VDD3P3	–1089.249	–1666.260	1089.249	–1666.260
113	WRF_PA2G_VBAT_VDD3P3	–1000.014	–2552.652	1000.014	–2552.652
114	WRF_PA2G_VBAT_VDD3P3	–800.016	–2570.652	800.016	–2570.652
115	WRF_RFOUT_2G	–600.018	–2552.652	600.018	–2552.652
116	WRF_PA2G_VBAT_GND3P3	–542.224	–2017.656	542.224	–2017.656
117	WRF_RX2G_GND1P2	–302.509	–1761.939	302.509	–1761.939
118	WRF_RFIN_2G	–200.022	–2471.652	200.022	–2471.652
119	WRF_LNA_2G_GND1P2	–200.022	–2071.656	200.022	–2071.656
120	WRF_RX2G_GND1P2	–165.822	–1590.174	165.822	–1590.174
121	WRF_TSSI_A	–200.022	–943.668	200.022	–943.668
122	WRF_GPIO_OUT	–279.173	–759.168	279.173	–759.168
123	WRF_LOGENG_GND1P2	–338.919	–1125.594	338.919	–1125.594
124	WRF_AFE_GND1P2	–661.308	–1125.594	661.308	–1125.594
125	WRF_TX_GND1P2	–856.014	–1271.664	856.014	–1271.664
126	WRF_VCO_GND1P2	–1032.414	–471.672	1032.414	–471.672
127	WRF_BUCK_VDD1P5	–1066.853	–1047.744	1066.853	–1047.744
128	WRF_BUCK_VDD1P5	–1066.853	–847.746	1066.853	–847.746
129	WRF_BUCK_GND1P5	–1166.852	–647.748	1166.852	–647.748
130	WRF_BUCK_VDD1P5	–1266.851	–1047.744	1266.851	–1047.744
131	WRF_BUCK_VDD1P5	–1266.851	–847.746	1266.851	–847.746
132	WRF_SYNTH_VBAT_VDD3P3	–1503.344	–1089.662	1503.344	–1089.662
133	WRF_MMD_GND1P2	–1627.031	–889.668	1627.031	–889.668
134	WRF_MMD_VDD1P2	–1854.006	–1271.664	1854.006	–1271.664
135	WRF_CP_GND1P2	–1922.892	–980.154	1922.892	–980.154
136	WRF_XTAL_VDD1P5	–1950.522	–353.066	1950.522	–353.066
137	WRF_XTAL_GND1P2	–2000.004	–554.598	2000.004	–554.598
138	WRF_XTAL_IN	–2199.998	–353.066	2199.998	–353.066
139	WRF_PFD_VDD1P2	–2200.002	–1185.062	2200.002	–1185.062
140	WRF_PFD_GND1P2	–2200.002	–985.064	2200.002	–985.064
141	WRF_XTAL_VDD1P2	–2200.002	–753.062	2200.002	–753.062
142	WRF_XTAL_OUT	–2200.002	–553.063	2200.002	–553.063
143	BBPLLAVDD1P2	–2205.429	–52.326	2205.429	–52.326
144	BBPLLAVSS	–2005.431	–57.348	2005.431	–57.348
145	RF_SW_CTRL_0	–1831.200	318.141	1831.200	318.141
146	RF_SW_CTRL_1	–2072.022	449.946	2072.022	449.946
147	RF_SW_CTRL_2	–1691.052	517.221	1691.052	517.221
148	RF_SW_CTRL_3	–1895.118	544.410	1895.118	544.410
149	RF_SW_CTRL_4	–1809.960	772.110	1809.960	772.110

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
150	RF_SW_CTRL_5	–1617.639	713.790	1617.639	713.790
151	RF_SW_CTRL_6	–2129.154	817.452	2129.154	817.452
152	RF_SW_CTRL_7	–1573.278	922.392	1573.278	922.392
153	RF_SW_CTRL_8	–1749.264	1019.259	1749.264	1019.259
154	RF_SW_CTRL_9	–1944.888	972.936	1944.888	972.936
155	OTP_VDD33	–1400.001	808.353	1400.001	808.353
156	VDDIO_RF	–1399.398	343.350	1399.398	343.350
157	VDDIO_RF	–1400.001	543.348	1400.001	543.348
158	NC	–2055.795	2207.556	2055.795	2207.556
159	PAD_PLL_AVDD1P2	–1943.295	2041.056	1943.295	2041.056
160	NC	–1689.455	2041.056	1689.455	2041.056
161	PAD_PLL_AVSS	–2280.795	2207.556	2280.795	2207.556
162	NC	–2168.295	2041.056	2168.295	2041.056
163	PAD_PLL_AVSS	–1830.795	2207.556	1830.795	2207.556
164	NC	–1576.959	2207.556	1576.959	2207.556
165	NC	–2168.295	2374.758	2168.295	2374.758
166	NC	–1943.295	2374.758	1943.295	2374.758
167	PAD_RXTX_AVDD1P2	–1689.455	2374.758	1689.455	2374.758
168	PAD_RXTX_AVSS	–2280.795	2541.258	2280.795	2541.258
169	NC	–1830.795	2541.258	1830.795	2541.258
170	NC	–2055.795	2541.258	2055.795	2541.258
171	SDIO_CLK	–1269.996	1963.350	1269.996	1963.350
172	SDIO_CMD	–1269.996	2168.352	1269.996	2168.352
173	SDIO_DATA_0	–1040.001	1963.350	1040.001	1963.350
174	SDIO_DATA_1	–1040.001	2168.352	1040.001	2168.352
175	SDIO_DATA_2	–830.004	1963.350	830.004	1963.350
176	SDIO_DATA_3	–735.000	2168.352	735.000	2168.352
177	VDDIO_SD	–1040.001	1763.352	1040.001	1763.352
178	VDDIO_SD	–830.004	1763.352	830.004	1763.352
179	STROBE	–545.001	1963.350	545.001	1963.350
180	DATA	–240.000	1963.350	240.000	1963.350
181	RREFHSIC	–805.002	1568.349	805.002	1568.349
182	AGND12PLL	–605.004	1553.346	605.004	1553.346
183	DVDD12HSIC2	–394.998	1763.352	394.998	1763.352
184	AVDD12PLL	–605.004	1763.352	605.004	1763.352
185	DVDD12HSIC	–394.998	1553.346	394.998	1553.346
186	NC	–15.000	2168.352	15.000	2168.352
187	NC	4.998	1768.347	–4.998	1768.347

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
188	NC	–5.001	1968.354	5.001	1968.354
189	GPIO_0	239.997	1968.354	–239.997	1968.354
190	GPIO_1	239.997	1768.347	–239.997	1768.347
191	GPIO_2	290.001	2168.352	–290.001	2168.352
192	GPIO_3	284.997	1568.349	–284.997	1568.349
193	GPIO_4	675.003	1908.351	–675.003	1908.351
194	GPIO_5	485.004	1568.349	–485.004	1568.349
195	GPIO_6	675.003	1708.353	–675.003	1708.353
196	GPIO_7	689.997	1508.346	–689.997	1508.346
197	GPIO_8	920.001	1568.349	–920.001	1568.349
198	GPIO_9	820.002	1348.353	–820.002	1348.353
199	GPIO_10	820.002	1073.349	–820.002	1073.349
200	GPIO_11	1119.999	1073.349	–1119.999	1073.349
201	GPIO_12	1119.999	1338.354	–1119.999	1338.354
202	GPIO_14	1180.002	1738.350	–1180.002	1738.350
203	GPIO_13	1180.002	1538.352	–1180.002	1538.352
204	GPIO_15	1180.002	1973.349	–1180.002	1973.349
205	JTAG_SEL	1119.999	2168.352	–1119.999	2168.352
206	VSSC	699.996	668.349	–699.996	668.349
207	VSSC	699.996	468.351	–699.996	468.351
208	VSSC	900.003	468.351	–900.003	468.351
209	VSSC	900.003	668.349	–900.003	668.349
210	VDDIO	605.001	1148.346	–605.001	1148.346
211	VDDIO	384.996	1368.351	–384.996	1368.351
212	VDDIO	605.001	948.348	–605.001	948.348
213	VDDC_PHY	–2120.001	1213.353	2120.001	1213.353
214	VDDC_PHY	–1920.003	1213.353	1920.003	1213.353
215	VDDC	–1689.999	–71.649	1689.999	–71.649
216	VDDC	–1490.001	–71.649	1490.001	–71.649
217	VDDC_PHY	–1490.001	128.349	1490.001	128.349
218	VDDC_PHY	–1249.998	128.349	1249.998	128.349
219	VDDC_PHY	–840.003	578.349	840.003	578.349
220	VDDC_PHY	–639.996	578.349	639.996	578.349
221	VDDC_PHY	–269.997	628.353	269.997	628.353
222	VDDC_PHY	–269.997	828.351	269.997	828.351
223	VDDC	–195.000	1568.349	195.000	1568.349
224	VDDC	–195.000	1768.347	195.000	1768.347
225	VDDC_PHY	–195.000	1268.352	195.000	1268.352

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
226	VDDC	4.998	–6.651	–4.998	–6.651
227	VDDC_SUBCORE	4.998	193.347	–4.998	193.347
228	VDDC_SUBCORE	4.998	393.354	–4.998	393.354
229	VDDC	4.998	628.353	–4.998	628.353
230	VDDC	4.998	828.351	–4.998	828.351
231	VDDC_SUBCORE	4.998	1028.349	–4.998	1028.349
232	VDDC_SUBCORE	4.998	1568.349	–4.998	1568.349
233	VDDC_SUBCORE	4.998	1268.352	–4.998	1268.352
234	VDDC	120.000	–216.648	–120.000	–216.648
235	VDDC	319.998	–216.648	–319.998	–216.648
236	VDDC	405.003	1148.346	–405.003	1148.346
237	VDDC_SUBCORE	405.003	948.348	–405.003	948.348
238	VDDC	689.997	–211.653	–689.997	–211.653
239	VDDC	890.004	–211.653	–890.004	–211.653
240	VDDC_SUBCORE	1090.002	–11.646	–1090.002	–11.646
241	VDDC_SUBCORE	1396.119	–24.588	–1396.119	–24.588
242	VSSC	–1374.999	1263.348	1374.999	1263.348
243	VSSC	–1269.996	1563.354	1269.996	1563.354
244	VSSC	–1175.001	1263.348	1175.001	1263.348
245	VSSC	–1269.996	1763.352	1269.996	1763.352
246	VSSC	–1249.998	–71.649	1249.998	–71.649
247	VSSC	–975.003	1263.348	975.003	1263.348
248	VSSC	–1050.000	–71.649	1050.000	–71.649
249	VSSC	–1040.001	1563.354	1040.001	1563.354
250	VSSC	–840.003	–71.649	840.003	–71.649
251	VSSC	–840.003	128.349	840.003	128.349
252	VSSC	–840.003	328.347	840.003	328.347
253	VSSC	–840.003	828.351	840.003	828.351
254	VSSC	–840.003	1028.349	840.003	1028.349
255	VSSC	–805.002	1368.351	805.002	1368.351
256	VSSC	–639.996	828.351	639.996	828.351
257	VSSC	–639.996	1028.349	639.996	1028.349
258	VSSC	–439.998	128.349	439.998	128.349
259	VSSC	–439.998	328.734	439.998	328.734
260	VSSC	–439.998	–71.649	439.998	–71.649
261	VSSC	94.998	–606.654	–94.998	–606.654
262	VSSC	94.998	–806.652	–94.998	–806.652
263	VSSC	204.996	193.347	–204.996	193.347

Table 17. 286-Bump WLCSP Coordinates (Cont.)

Bump#	Signal Name	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
264	VSSC	204.996	1028.349	–204.996	1028.349
265	VSSC	204.996	628.353	–204.996	628.353
266	VSSC	204.996	828.351	–204.996	828.351
267	VSSC	133.104	–1457.550	–133.104	–1457.550
268	VSSC	305.004	–446.652	–305.004	–446.652
269	VSSC	204.996	393.354	–204.996	393.354
270	VSSC	499.998	193.347	–499.998	193.347
271	VSSC	457.401	–1457.550	–457.401	–1457.550
272	VSSC	499.998	–806.652	–499.998	–806.652
273	VSSC	505.002	–446.652	–505.002	–446.652
274	VSSC	499.998	468.351	–499.998	468.351
275	VSSC	499.998	668.349	–499.998	668.349
276	VSSC	499.998	–6.651	–499.998	–6.651
277	VSSC	699.996	–806.652	–699.996	–806.652
278	VSSC	699.996	–606.654	–699.996	–606.654
279	VSSC	699.996	–6.651	–699.996	–6.651
280	VSSC	660.603	–1457.550	–660.603	–1457.550
281	VSSC	900.003	68.346	–900.003	68.346
282	VSSC	1090.002	–211.653	–1090.002	–211.653
283	VSSC	1100.001	668.349	–1100.001	668.349
284	VSSC	1229.997	508.347	–1229.997	508.347
285	VSSC	1229.997	308.349	–1229.997	308.349
286	VSSC	1290.000	–211.653	–1290.000	–211.653

12.3 Signal Descriptions

The signal name, type, and description of each pin in the CYW4339 is listed in Table 18. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
WLAN and Bluetooth RF Signal Interface					
N7	W10	118	WRF_RFIN_2G	I	2.4 GHz Bluetooth and WLAN receiver shared input.
N5	W8	93	BT_RF_TX	O	Bluetooth PA output.
N12	W18	102	WRF_RFIN_5G	I	5 GHz WLAN receiver input.
N8	W12	115	WRF_RFOUT_2G	O	2.4 GHz WLAN PA output.
N11	W16	106	WRF_RFOUT_5G	O	5 GHz WLAN PA output.
J7	V11	121	WRF_TSSI_A	I	5 GHz TSSI input from an optional external power amplifier/power detector.
H7	V10	122	WRF_RES_EXT/WRF_GPIO_OUT/WRF_TSSI_G	I/O	GPIO or 2.4 GHz TSSI input from an optional external power amplifier/power detector.
RF Switch Control Lines					
F12	J19	145	RF_SW_CTRL_0	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
F11	J17	146	RF_SW_CTRL_1	O	
E12	J18	147	RF_SW_CTRL_2	O	
E11	G19	148	RF_SW_CTRL_3	O	
D12	H17	149	RF_SW_CTRL_4	O	
F8	G17	150	RF_SW_CTRL_5	O	
H9	G18	151	RF_SW_CTRL_6	O	
G7	J16	152	RF_SW_CTRL_7	O	
E10	G16	153	RF_SW_CTRL_8	O	
F5	H16	154	RF_SW_CTRL_9	O	
WLAN PCI Express Interface					
–	A19	–	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required
–	B16	–	PERST_L	I (PU)	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1.
–	B13	–	PAD_RDN0	I	Receiver differential pair (x1 lane).
–	C13	–	PAD_RDP0	I	
–	A18	–	PAD_REFCLKN	I	PCIE Differential Clock inputs (negative and positive). 100 MHz differential.
–	B18	–	PAD_REFCLKP	I	
–	B15	–	PAD_TDN0	O	Transmitter differential pair (x1 lane).
–	B14	–	PAD_TDP0	O	

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions (Cont.)

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
–	B19	–	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
–	–	–	PAD_TESTP	–	PCIe test pin.
–	–	–	PAD_TESTN	–	
WLAN SDIO Bus Interface **Note:** These signals can also have alternate functionality depending on package and host interface mode. Refer to Table 26, "CYW4339 GPIO/SDIO Alternative Signal Functions," for additional details.					
B11	B11	171	SDIO_CLK	I	SDIO clock input.
B12	C11	172	SDIO_CMD	I/O	SDIO command line.
B10	C10	173	SDIO_DATA_0	I/O	SDIO data line 0.
C10	A11	174	SDIO_DATA_1	I/O	SDIO data line 1.
D10	C9	175	SDIO_DATA_2	I/O	SDIO data line 2.
C11	B9	176	SDIO_DATA_3	I/O	SDIO data line 3.
WLAN GPIO Interface **Note:** The GPIO signals can be multiplexed via software and the JTAG_SEL pin to behave as various specific functions. See Table 26, "CYW4339 GPIO/SDIO Alternative Signal Functions," for additional details.					
B6	D9	189	GPIO_0	I/O	Programmable GPIO pins. **Note:** These GPIO signals can be configured by software: as either inputs or outputs, to have internal pull-ups or pull-downs enabled or disabled, and to use either a high or low polarity upon assertion.
C6	C16	190	GPIO_1	I/O	
D6	C8	191	GPIO_2	I/O	
B5	A7	192	GPIO_3	I/O	
C5	B5	193	GPIO_4	I/O	
D5	A5	194	GPIO_5	I/O	
C4	C7	195	GPIO_6	I/O	
D4	B7	196	GPIO_7	I/O	
H1	E8	197	GPIO_8	I/O	
–	–	198	GPIO_9	I/O	
–	–	199	GPIO_10	I/O	
–	–	200	GPIO_11	I/O	
–	–	201	GPIO_12	I/O	
–	A3	202	GPIO_14	I/O	
–	D8	203	GPIO_13	I/O	
–	D6	204	GPIO_15	I/O	
JTAG Interface					
E5	C6	205	JTAG_SEL	I/O	JTAG select. Pull high to select the JTAG interface. If the JTAG interface is not used, this pin may be left floating or connected to ground. **Note:** See Table 26, "CYW4339 GPIO/SDIO Alternative Signal Functions," for the JTAG signal pins.

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions (Cont.)

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
Clocks					
H12	P19	138	WRF_XTAL_IN	I	XTAL oscillator input.
J12	R19	142	WRF_XTAL_OUT	O	XTAL oscillator output.
B4	J7	39	LPO_IN	I	External sleep clock input (32.768 kHz).
H3	W3	56	CLK_REQ	O	Reference clock request (shared by BT and WLAN).
	SFLASH				
–	N3	49	BT_SF_MOSI	I/O	SFLASH_SI
–	P3	46	BT_SF_CLK	I/O	SFLASH_CLK
–	R1	47	BT_SF_CSN	I/O	SFLASH_CSN
–	R2	48	BT_SF_MISO	I/O	SFLASH_SO
N2	–	78	FM_RFIN	I	FM Radio antenna port.
–	–	75	FM_RFAUX	I	FM radio auxiliary antenna port.
K1	–	86	FM_DAC_VOUT1/FM_AOUT1	O	FM DAC output 1.
L1	–	85	FM_DAC_VOUT2/FM_AOUT2	O	FM DAC output 2.
Bluetooth PCM					
G2	–	46	BT_PCM_CLK/BT_PCMCLK	I/O	PCM clock; can be master (output) or slave (input).
G1	–	48	BT_PCM_IN	I	PCM data input.
J3	–	49	BT_PCM_OUT	O	PCM data output.
H2	–	47	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input).
Bluetooth USB Interface					
–	N1	40	HUSB_DN	I/O	USB (Host) data negative. Negative terminal of the USB transceiver.
–	N2	41	HUSB_DP	I/O	USB (Host) data positive. Positive terminal of the USB transceiver.
Bluetooth UART					
E6	T3	50	BT_UART_CTS_N/ BT_UART_CTS	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
F6	V1	51	BT_UART_RTS_N/ BT_UART_RTS/BT_LED	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
G6	W1	52	BT_UART_RXD/ BT_RFDIS-ABLE2	I	UART serial input. Serial data input for the HCI UART interface. BT RF disable pin 2.
F7	W2	53	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
Bluetooth/I2S					
J6	R3	44	BT_I2S_CLK	I/O	I^2S clock, can be master (output) or slave (input).
K6	U2	42	BT_I2S_DO	I/O	I^2S data output.
K5	U3	43	BT_I2S_DI	I/O	I^2S data input.

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions (Cont.)

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
H6	U1	45	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input).
Bluetooth Test Mode					
–	U1	55	BT_TM1	I/O	ARM JTAG mode.
Bluetooth GPIO					
–	–	59	BT_GPIO_2	I/O	Bluetooth general-purpose I/O.
–	–	60	BT_GPIO_3	I/O	Bluetooth general-purpose I/O.
–	C19	61	BT_GPIO_4	I/O	Bluetooth general-purpose I/O.
–	–	62	BT_GPIO_5	I/O	Bluetooth general-purpose I/O.
M6	–	91	BT_AGPIO	I/O	BT analog GPIO pin.
Miscellaneous					
B3	D5	3	WL_REG_ON	I	Used by PMU to power up or power down the internal CYW4339 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
D3	C5	32	BT_REG_ON	I	Used by PMU to power up or power down the internal CYW4339 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
K3	M3	57	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE.
J2	V3	58	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE.
B8	–	179	HSIC_STROBE/STROBE	I/O	Unsupported. This pin can be connected to ground or left unconnected (no-connect).
B7	–	180	HSIC_DATA/DATA	I/O	Unsupported. This pin can be connected to ground or left unconnected (no-connect).
B9	–	181	RREFHSIC	I	Unsupported. Leave this pin unconnected (no-connect).
Integrated Voltage Regulators					
C2	C3	15	SR_VDDBATA5V	I	Quiet VBAT.
C1	B1, B2, C1	11, 12, 14	SR_VDDBATP5V	I	Power VBAT.
B2	A2, B2	6–10, 13	SR_VLX	O	Cbuck switching regulator output. Refer to Table 42 for details of the inductor and capacitor required on this output.
D1	F1, F2	16, 19, 23, 26	LDO_VDD1P5	I	LNLDO input.
F2	L1	27, 30, 34, 36	LDO_VDDBAT5V	I	LDO VBAT.
H11	N19	136	WRF_XTAL_VDD1P5/WRF_XTAL_BUCK_VDD1P5	I	XTAL LDO input (1.35V).
K12	T19	141	WRF_XTAL_VDD1P2/WRF_XTAL_OUT_VDD1P2	O	XTAL LDO output (1.2V).
E2	K2	24	VOUT_LNLDO	O	Output of LNLDO.
D2	G2	17, 18, 20	VOUT_CLDO	O	Output of core LDO.
F1	J2	33	VOUT_BTLDO2P5	O	Output of BT LDO.

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions (Cont.)

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
E1	H1	22, 25, 28	VOUT_3P3	O	LDO 3.3V output.
–	H2	29	VOUT_3P3_SENSE	O	Voltage sense pin for LDO 3.3V output.
Bluetooth Supplies					
N6	V8	92	BT_PAVDD/BT_PAVDD2P5	PWR	Bluetooth PA power supply.
N4	W5	96	BT_LNAVDD/BT_LNAVDD1P2	PWR	Bluetooth LNA power supply.
L4	W6	90	BT_IFVDD/BT_IFVDD1P2	PWR	Bluetooth IF block power supply.
M4	V6	98	BT_PLLVDD/BT_PLLVDD1P2	PWR	Bluetooth RF PLL power supply.
N3	V5	99	BT_VCOVDD/BT_VCOVDD1P2	PWR	Bluetooth RF power supply.
–	–	55	BT_VDDC_ISO_1	PWR	Core supply for power-on/off island VDDC_G.
–	–	66	BT_VDDC_ISO_2	PWR	Core supply for power-on/off island VDDB.
FM Transceiver Supplies					
–	–	87	FM_VCOVDD	PWR	FM VCO supply.
–	–	80	FM_LNAVDD	PWR	FM LNA power supply.
N1	–	–	FM_LNAVCOVDD1P2	PWR	FM LNA VCO power supply.
L2	–	84	FM_PLLVDD/FM_PLLVDD1P2	PWR	FM PLL power supply.
–	–	79	FM_IFVDD	PWR	FM IF power supply.
–	–	82	FM_DAC_AVDD	PWR	FM DAC power supply.
J1	–	–	FM_AUDIOVDD1P2	PWR	FM Audio power supply.
WLAN Supplies					
–	L15	127, 128, 130, 131	WRF_BUCK_VDD1P5	PWR	Internal capacitor-less LDO supply.
H8	–	–	WRF_WL_LNLDOIN_VDD1P5	PWR	LNLDO 1.35V supply.
K9	V19	132	WRF_SYNTH_VBAT_VDD3P3	PWR	Synth VDD 3.3V supply.
L9	V14	112	WRF_PADRV_VBAT_VDD3P3	PWR	PA Driver VBAT supply.
N10	V15	107, 110	WRF_PA5G_VBAT_VDD3P3	PWR	5 GHz PA 3.3V VBAT supply.
N9	V13	113, 114	WRF_PA2G_VBAT_VDD3P3	PWR	2 GHz PA 3.3V VBAT supply.
K10	U18	134	WRF_MMD_VDD1P2	PWR	1.2V supply.
K11	T18	139	WRF_PFD_VDD1P2	PWR	1.2V supply.
Miscellaneous Supplies					
–	L18	155	OTP_VDD33	PWR	OTP 3.3V supply.
C7, C12, G4, G5, G8	E10, E11, G14, H14, K7	213–241	VDDC/WL_VDDC	PWR	1.2V core supply for WLAN.
F3	B3	210–212	VDDIO /VDDIO2	PWR	1.8V–3.3V supply for WLAN. Must be directly connected to PMU_VDDIO and BT_VDDIO on the PCB.
H5, J4	L7, M7	67–74	BT_VDDC	PWR	1.2V core supply for BT.
–	L2	37, 38	PMU_VDDIO	PWR	1.8V–3.3V supply for PMU controls. Must be directly connected to VDDIO and BT_VDDIO on the PCB.
H4	L3	63–65	BT_VDDIO	PWR	1.8V–3.3V supply for BT. Must be directly connected to PMU_VDDIO and VDDIO on the PCB.

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions (Cont.)

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
D9	A9	177, 178	VDDIO_SD	PWR	1.8V–3.3V supply for SDIO pads.
E7	K17	156, 157	VDDIO_RF	PWR	IO supply for RF switch control pads (3.3V).
C8	–	184	AVDD12PLL/HSIC_AVDD12PLL	PWR	HSIC is not supported. Connect this pin to ground to minimize leakage.
C9	–	185	DVDD12HSIC/HSIC_DVDD12	PWR	HSIC is not supported. Connect this pin to ground to minimize leakage.
G12	L19	143	BBPLL_AVDD1P2	PWR	1.2V supply for baseband PLL.
–	D18	159	PLL_AVDD1P2	PWR	1.2V supply for PCIe PLL.
–	D19	167	AVDD1P2	PWR	1.2V supply for PCIe.
Ground					
H10	L12	126	WRF_VCO_GND1P2/ WRF_VCO_GND	GND	VCO/LOGEN ground.
–	–	183	DVDD12HSIC2	GND	Supply for DVDD12HSIC2.
K7	R12	124	WRF_AFE_GND1P2	GND	AFE ground.
J8	M12	129	WRF_BUCK_GND1P5	GND	Internal capacitor-less LDO ground.
M7	T10	119	WRF_LNA_2G_GND1P2	GND	2 GHz internal LNA ground.
M12	T15	101	WRF_LNA_5G_GND1P2	GND	5 GHz internal LNA ground.
L8	R13	125	WRF_TX_GND1P2	GND	TX ground.
L10	R14	108	WRF_PADRV_VBAT_GND3P3	GND	PAD ground.
G11	M15, P18	137	WRF_XTAL_GND1P2	GND	XTAL ground.
L7	P11	117, 120	WRF_RX2G_GND1P2	GND	RX 2GHz ground.
L12	T16	103	WRF_RX5G_GND1P2	GND	RX 5GHz ground.
–	R15	104	WRF_LOGEN_GND1P2	GND	LOGEN ground.
–	M11	123	WRF_LOGENG_GND1P2	GND	LOGEN ground.
L11	–	–	WRF_LO_GND1P2_1	GND	LO ground.
K8	–	–	WRF_LO_GND1P2_2	GND	LO ground.
–	U15, V16	105, 109	WRF_PA5G_VBAT_GND3P3	GND	5 GHz PA ground.
–	R11, V12	111, 116	WRF_PA2G_VBAT_GND3P3	GND	2 GHz PA ground.
M11	–	–	WRF_PA_VBAT_GND3P3_1	GND	PA ground.
M10	–	–	WRF_PA_VBAT_GND3P3_2	GND	PA ground.
M9	–	–	WRF_PA_VBAT_GND3P3_3	GND	PA ground.
M8	–	–	WRF_PA_VBAT_GND3P3_4	GND	PA ground.
J9	P14	133	WRF_MMD_GND1P2	GND	Ground.
J11	N15	135	WRF_CP_GND1P2/ WRF_CP_GND	GND	Ground.
J10	P15	140	WRF_PFD_GND1P2	GND	Ground.
D7, D11, E3, E8, J5, K4	H9–H12, J8, J12, K8, K12, L8, L11, M8–M10	31, 35, 161, 163, 168, 242–286	VSSC	GND	Core ground for WLAN and BT.
B1	D1, E1, E2	1, 2, 4, 5	SR_PVSS	GND	Power ground.
C3	H8	21	PMU_AVSS	GND	Quiet ground.

Table 18. FCFBGA, WLBGA, and WLCSP Signal Descriptions (Cont.)

WLBGA Ball#	FCFBGA Ball#	WLCSP Bump#	Signal Name	Type	Description
D8	–	182	AGND12PLL/HSIC_AGNDPLL	GND	PLL ground.
M5	T8	94	BT_PAVSS	GND	Bluetooth PA ground.
–	R8	95	BT_LNAVSS	GND	Bluetooth LNA ground.
L6	R9	89	BT_IFVSS	GND	Bluetooth IF block ground.
L5	R7	97	BT_PLLVSS	GND	Bluetooth PLL ground.
M3	P8	100	BT_VCOVSS	GND	Bluetooth VCO ground.
M1	–	83	FM_VCOVSS	GND	FM VCO Ground.
M2	–	77	FM_LNAVSS	GND	FM LNA Ground.
L3	–	88	FM_PLLVSS	GND	FM PLL Ground.
–	–	76	FM_IFVSS	GND	FM IF ground.
–	–	81	FM_DAC_VSS	GND	FM DAC ground.
K2	–	–	FM_AUDIOVSS	GND	FM Audio Ground.
G10	L13	144	AVSS_BBPLL/BBPLLAVSS	GND	Baseband PLL ground.
–	D13, D16	–	PCIE_VSS	GND	PCIe ground.
–	–	209	VSSC	GND	Ground.
–	–	208	VSSC	GND	Ground.
–	–	207	VSSC	GND	Ground.
–	–	206	VSSC	GND	Ground.
No Connect					
A2, A3, A4, A6, A7, A9, A10, A11	F5, G5, W19	158, 160, 162, 164, 165, 166, 169, 170, 186, 187, 188	NC	–	No connect

12.4 WLAN GPIO Signals and Strapping Options

The pins listed in Table 19 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 19. WLAN GPIO Functions and Strapping Options

Pin Name	FCBGA Pin #	WLBGA Pin #	WLCSP Pin #	Default Function	Description
GPIO_7	B7	D4	196	1	SDIO_SEL[1]
GPIO_8	E8	H1	197	0	SDIO_PADVDDIO
GPIO_14	A3	–	202	0	PCIE_DISABLE
SDIO_CLK	B11	B11	171	1	CPU-LESS/SPROM_DISABLE[1]
SDIO_DATA_2	C9	D10	175	1	SPI_SEL[1]

1. See Table 20, Table 21, and Table 22.

Table 20. SDIO/ I/O Voltage Selection (All Packages)

SDIO_SEL	SPI_SEL	SDIO_PADVDDIO	Mode
1	X	0	1.8V I/O
1	X	1	3.3V I/O
0	1	0	1.8V I/O
0	1	1	3.3V I/O
0	0	X	3.3V I/O

Table 21. Host Interface Selection (FCBGA Package only)

SDIO_SEL	SPI_SEL	PCIE_DISABLE	SPROM_DISABLE[1]	Mode
1	X	0	X	SDIO and PCIe mode
1	X	1	X	SDIO mode
0	1	0	X	PCIe mode
0	1	1	X	reserved
0	0	0	0	PCIe mode with SPROM on the SDIO pins[2]
0	0	0	1	PCIe mode (no SPROM)

1. SPROM_DISABLE strapping is valid only in the FCBGA package and only used if SDIO is disabled.

2. SPROM is only available for PCIe mode.

Table 22. Host Interface Selection (WLBGA and WLCSP Packages[1])

SDIO_SEL	SPI_SEL	CPULESS	Mode
1	X	X	SDIO Mode (3.3V or 1.8V I/O)
0	1	X	reserved
0	0	0	Unsupported
0	0	1	Unsupported

1. PCIe and SPROM modes are not available in the WLBGA and WLCSP packages.

Table 23. OTP/SPROM Select

Mode	SDIO CIS	PCIE Configuration
PCIe Disabled	From OTP if OTP is programmed; ELSE default CIS.	–
PCIe Enabled	Default CIS	From SPROM if SPROM is present; ELSE from OTP (if programmed); ELSE default configuration.

12.4.1 Multiplexed Bluetooth GPIO Signals

The Bluetooth GPIO pins (BT_GPIO_0 to BT_GPIO_7) are multiplexed pins and can be programmed to be used as GPIOs or for other Bluetooth interface signals such as I^2S. The specific function for a given BT_GPIO_X pin is chosen by programming the Pad Function Control register for that specific pin. Table 24 shows the possible options for each BT_GPIO_X pin. Note that each BT_GPIO_X pin's Pad Function Control register setting is independent (BT_GPIO_1 can be set to pad function 7 at the same time that BT_GPIO_3 is set to pad function 0). When the Pad Function Control register is set to 0, the BT_GPIOs do not have specific functions assigned to them and behave as generic GPIOs. The A_GPIO_X pins described below are multiplexed behind the CYW4339's PCM and I^2S interface pins.

Table 24. GPIO Multiplexing Matrix

Pin Name	Pad Function Control Register Setting								
	0	1	2	3	4	5	6	7	15
BT_UART_CTS_N	UART_CTS_N	–	–	–	–	–	–	A_GPIO[1]	–
BT_UART_RTS_N	UART_RTS_N	–	–	–	–	–	–	A_GPIO[0]	–
BT_UART_RXD	UART_RXD	–	–	–	–	–	–	GPIO[5]	–
BT_UART_TXD	UART_TXD	–	–	–	–	–	–	GPIO[4]	–
BT_PCM_IN	A_GPIO[3]	PCM_IN	PCM_IN	HCLK	–	–	–	I2S_SSDI/ MSDI	SF_MISO
BT_PCM_OUT	A_GPIO[2]	PCM_OUT	PCM_OUT	LINK_IND	–	I2S_MSDO	–	I2S_SSDO	SF_MOSI
BT_PCM_SYNC	A_GPIO[1]	PCM_SYNC	PCM_SYNC	HCLK	INT_LPO	I2S_MWS	–	I2S_SWS	SF_SPI_CSN
BT_PCM_CLK	A_GPIO[0]	PCM_CLK	PCM_CLK	–	–	I2S_MSCK	–	I2S_SSCK	SF_SPI_CLK
BT_I2S_DO	A_GPIO[5]	PCM_OUT	–	–	I2S_SSDO	I2S_MSDO	–	STATUS	–
BT_I2S_DI	A_GPIO[6]	PCM_IN	–	HCLK	I2S_SSDI/ MSDI	–	–	TX_CON_FX	–
BT_I2S_WS	GPIO[7]	PCM_SYNC	–	LINK_IND	–	I2S_MWS	–	I2S_SWS	–
BT_I2S_CLK	GPIO[6]	PCM_CLK	–	–	INT_LPO	I2S_MSCK	–	I2S_SSCK	–
BT_GPIO_5[1]	GPIO[5]	HCLK	–	I2S_MSCK	I2S_SSCK	–	–	CLK_REQ	–
BT_GPIO_4[1]	GPIO[4]	LINK_IND	–	I2S_MSDO	I2S_SSDO	–	–	–	–
BT_GPIO_3[1]	GPIO[3]	–	–	I2S_MWS	I2S_SWS	–	–	–	–
BT_GPIO_2[1]	GPIO[2]	–	–	–	I2S_SSDI/ MSDI	–	–	–	–
BT_GPIO_1	GPIO[1]	–	–	–	–	–	–	CLASS1[2]	–
BT_GPIO_0	GPIO[0]	–	–	–	clk_12p288	–	–	–	–
CLK_REQ	WL/ BT_CLK_REQ	–	–	–	–	–	–	A_GPIO[7]	–

1. Available only in the WLCSP package.

The multiplexed GPIO signals are described in Table 25.

Table 25. Multiplexed GPIO Signals

Pin Name	Type	Description
UART_CTS_N	I	Host UART clear to send.
UART_RTS_N	O	Device UART request to send.
UART_RXD	I	Device UART receive data.
UART_TXD	O	Host UART transmit data.
PCM_IN	I	PCM data input.
PCM_OUT	O	PCM data output.
PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input).
PCM_CLK	I/O	PCM clock, can be master (output) or slave (input).
GPIO[7:0]	I/O	General-purpose I/O.
A_GPIO[7:0]	I/O	A group general-purpose I/O.
I2S_MSDO	O	I^2S master data output.
I2S_MWS	O	I^2S master word select.
I2S_MSCK	O	I^2S master clock.
I2S_SSCK	I	I^2S slave clock.
I2S_SSDO	O	I^2S slave data output.
I2S_SWS	I	I^2S slave word select.
I2S_SSDI/MSDI	I	I^2S slave/master data input.
STATUS	O	Signals Bluetooth priority status.
TX_CON_FX	I	WLAN-BT coexist. Transmission confirmation; permission for BT to transmit.
RF_ACTIVE	O	WLAN-BT coexist. Asserted (logic high) during local BT RX and TX slots.
LINK_IND	O	BT receiver/transmitter link indicator.
CLK_REQ	O	WLAN/BT clock request output.
SF_SPI_CLK	O	SFlash SCLK: serial clock (output from master).
SF_MISO	I	SFlash MISO; SOMI: master input, slave output (output from slave).
SF_MOSI	O	SFlash MOSI; SIMO: master output, slave input (output from master).
SF_SPI_CSN	O	SFlash SS: slave select (active low, output from master).

12.5 GPIO/SDIO Alternative Signal Functions

Table 26. CYW4339 GPIO/SDIO Alternative Signal Functions [1 2]

Pins	WLBGA SDIO	WLCSP SDIO	FCBGA PCIE	FCBGA SDIO
GPIO_0	WL_HOST_WAKE	WL_HOST_WAKE	WL_HOST_WAKE	WL_HOST_WAKE
GPIO_1	WL_DEV_WAKE	WL_DEV_WAKE	WL_RF_DISABLE_L	WL_RF_DISABLE_L
GPIO_2	TCK, GCI_GPIO_1, or UART RX	TCK or GCI_GPIO_1	TCK, GCI_GPIO_1, or UART RX	TCK, GCI_GPIO_1, or UART RX
GPIO_3	TMS or GCI_GPIO_0	TMS or GCI_GPIO_0	TMS or GCI_GPIO_0	TMS or GCI_GPIO_0
GPIO_4	TDI or SECI_IN	TDI	TDI or SECI_IN	TDI or SECI_IN
GPIO_5	TDO or SECI_OUT	TDO	TDO or SECI_OUT	TDO or SECI_OUT
GPIO_6	TRST_L or UART TX	TRST_L	TRST_L or UART TX	TRST_L or UART TX
GPIO_7	[Strap, tied High]	[Strap, tied High]	[Strap, tied Low]	[Strap, tied High]
GPIO_8	[Strap, tied High or Low]	[Strap, tied High or Low]	–	[Strap, tied High or Low]
GPIO_9	N/A	–	N/A	N/A
GPIO_10	N/A	SECI_IN	N/A	N/A
GPIO_11	N/A	SECI_OUT	N/A	N/A
GPIO_12	N/A	UART_TX	N/A	N/A
GPIO_13	N/A	UART_RX	WL_LED	WL_LED
GPIO_14	N/A	–	–	–
GPIO_15	N/A	–	–	–
SDIO_CLK	SDIO_CLK	SDIO_CLK	[Strap, tied High]	SDIO_CLK
SDIO_CMD	SDIO_CMD	SDIO_CMD	SPROM_CS	SDIO_CMD
SDIO_DATA_0	SDIO_DATA_0	SDIO_DATA_0	SPROM_CLK	SDIO_DATA_0
SDIO_DATA_1	SDIO_DATA_1	SDIO_DATA_1	SPROM_MISO	SDIO_DATA_1
SDIO_DATA_2	SDIO_DATA_2	SDIO_DATA_2	[Strap, tied Low]	SDIO_DATA_2
SDIO_DATA_3	SDIO_DATA_3	SDIO_DATA_3	SPROM_MOSI	SDIO_DATA_3

1. N/A = Pin not available in this package.

2. JTAG signals (TCK, TDI, TDO, TMS, and TRST_L) are selected when JTAG_SEL pin is high.

12.6 I/O States

The following notations are used in Table 27:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 27. I/O States

Name	I/O	Keeper[1]	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs Are Present	Power Rail
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	–
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high	PD	Open drain. Active high	Open drain. Active high.	BT_VDDIO
BT_HOST_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PD	BT_VDDIO
BT_DEV_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDIO
BT_GPIO 2, 3, 4, 5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDIO
BT_UART_CTS	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	BT_VDDIO
BT_UART_RTS	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	BT_VDDIO
BT_UART_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	BT_VDDIO
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	BT_VDDIO
SDIO Data	I/O	N	Input/Output; PU (SDIO Mode)	Input; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)	Input; PU (SDIO Mode)	VDDIO_SD
SDIO CMD	I/O	N	Input/Output; PU (SDIO Mode)	Input; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)	Input; PU (SDIO Mode)	VDDIO_SD

Table 27. I/O States (Cont.)

Name	I/O	Keeper[1]	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs Are Present	Power Rail
SDIO_CLK	I	N	Input; NoPull	Input; noPull	High-Z, NoPull	Input; noPull	Input; noPull	VDDIO_SD
BT_PCM_CLK	I/O	Y	Input; NoPull[3]	Input; NoPull[3]	High-Z, NoPull	Output	Input, PD	BT_VDDIO
BT_PCM_IN	I/O	Y	Input; NoPull[3]	Input; NoPull[3]	High-Z, NoPull	Input; NoPull, Hi-Z	Input, PD	BT_VDDIO
BT_PCM_OUT	I/O	Y	Input; NoPull[3]	Input; NoPull[3]	High-Z, NoPull	Output	Input, PD	BT_VDDIO
BT_PCM_SYNC	I/O	Y	Input; NoPull [3]	Input; NoPull[3]	High-Z, NoPull	Output	Input, PD	BT_VDDIO
BT_I2S_WS	I/O	Y	PD[4]	PD[4]	High-Z, NoPull	Input, PD	Input, PD	BT_VDDIO
BT_I2S_CLK	I/O	Y	PD[4]	PD[4]	High-Z, NoPull	Input, PD	Input, PD	BT_VDDIO
BT_I2S_DI	I/O	Y	PD[4]	Input; PD[4]	High-Z, NoPull	Input, PD	Input, PD	BT_VDDIO
BT_I2S_DO	I/O	Y	Output[4]	Output[4]	High-Z, NoPull	Input, PD	Input, PD	BT_VDDIO
WL GPIO_0	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	VDDIO
WL GPIO_1	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_2	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	VDDIO
WL GPIO_4	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	VDDIO

Table 27. I/O States (Cont.)

Name	I/O	Keeper[1]	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs Are Present	Power Rail
WL GPIO_6	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_7	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_8	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])[5]	Input/Output; PU, PD, NoPull (programmable [Default: PD])[5]	High-Z, NoPull	Input; PD[5]	Input; PD[5]	VDDIO
WL GPIO_9[6]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	VDDIO
WL GPIO_10[6]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_11[6]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	VDDIO
WL GPIO_12[6]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_13[7]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_14[7]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO
WL GPIO_15[7]	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	VDDIO

Table 27. I/O States (Cont.)

Name	I/O	Keeper[1]	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs Are Present	Power Rail
RF_SW_CTRL_X	O	N	Output, NoPull	Output, NoPull	High-Z, NoPull	Output, NoPull	Output, NoPull	VDDIO_RF

1. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in Power-down state. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).

2. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.

3. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either output or input.

4. Depending on whether the I^2S interface is enabled and the configuration of I^2S is in master or slave mode, it can be either output or input

5. NoPull when in SDIO mode.

6. Only available in WLCSP package.

7. Only available in WLCSP and FCBGA packages.

13. DC Characteristics

13.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 28 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 28. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply[1]	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDD1P2	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O[2]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[b]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C

1. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V (for up to 250 seconds), cumulative duration over the lifetime of the device, are allowed.

2. Duration not to exceed 25% of the duty cycle.

13.2 Environmental Ratings

The environmental ratings are shown in Table 29.

Table 29. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[1]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

1. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

13.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 30. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	±1000	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	±300	V

13.4 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 31 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 31. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[1]	–	5.25[2]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDD1P2	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	WRF_TSSI_A, WRF_TSSI_G	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V

Table 31. Recommended Operating Conditions and DC Characteristics (Cont.)

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[3]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Output capacitance	C_{OUT}	–	–	5	pF

1. The CYW4339 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 4.8V.

2. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device are allowed. Voltage transients as high as 5.5V (for up to 250 seconds), cumulative duration over the lifetime of the device are allowed.

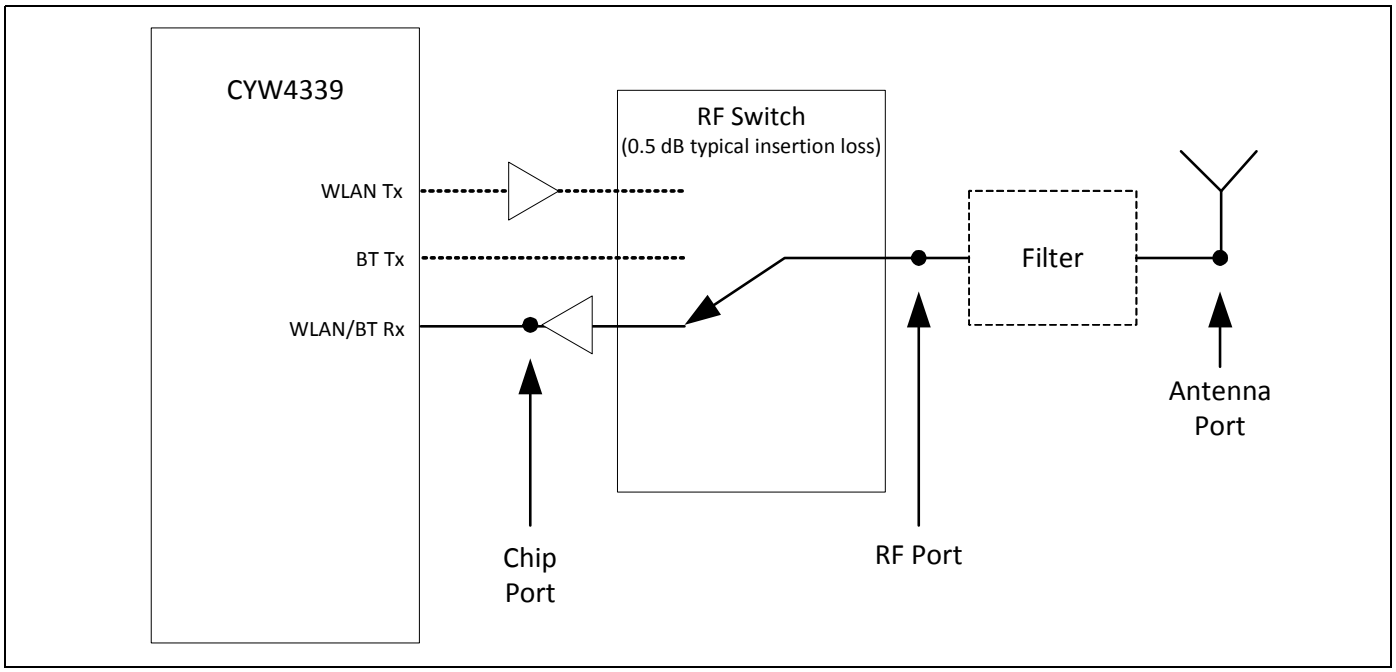
3. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

14. Bluetooth RF Specifications

Unless otherwise stated, limit values apply for the conditions specified in Table 29, “Environmental Ratings,” and Table 31, “Recommended Operating Conditions and DC Characteristics,”. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 29. Port Locations for Bluetooth Testing



Note: All Bluetooth specifications are measured at the chip port unless otherwise specified.

Table 32. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
Interference Performance[1]					
C/I co-channel	GFSK, 0.1% BER	–	8	–	dB
C/I 1-MHz adjacent channel	GFSK, 0.1% BER	–	–7	–	dB

Table 32. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
C/I 2-MHz adjacent channel	GFSK, 0.1% BER	–	–38	–	dB
C/I ≥ 3-MHz adjacent channel	GFSK, 0.1% BER	–	–56	–	dB
C/I image channel	GFSK, 0.1% BER	–	–31	–	dB
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	–	–46	–	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	9	–	dB
C/I 1-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–11	–	dB
C/I 2-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–39	–	dB
C/I ≥ 3-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–55	–	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–23	–	dB
C/I 1-MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–43	–	dB
C/I co-channel	8–DPSK, 0.1% BER	–	17	–	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–4	–	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–37	–	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–53	–	dB
C/I Image channel	8–DPSK, 0.1% BER	–	–16	–	dB
C/I 1-MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–37	–	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					
GFSK (1 Mbps)[2]					
698–716 MHz	WCDMA	–	–13.5	–	dBm
776–849 MHz	WCDMA	–	–13.8	–	dBm
824–849 MHz	GSM850	–	–13.5	–	dBm
824–849 MHz	WCDMA	–	–14.3	–	dBm
880–915 MHz	E-GSM	–	–13.1	–	dBm
880–915 MHz	WCDMA	–	–13.1	–	dBm
1710–1785 MHz	GSM1800	–	–18.1	–	dBm
1710–1785 MHz	WCDMA	–	–17.4	–	dBm
1850–1910 MHz	GSM1900	–	–19.4	–	dBm
1850–1910 MHz	WCDMA	–	–18.8	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.7	–	dBm
1920–1980 MHz	WCDMA	–	–19.6	–	dBm
2010–2025 MHz	TD–SCDMA	–	–20.4	–	dBm
2500–2570 MHz	WCDMA	–	–20.4	–	dBm
2500–2570 MHz [5]	Band 7	–	–30.5	–	dBm
2300-2400 MHz [6]	Band 40	–	–34.0	–	dBm
2570–2620 MHz [3]	Band 38	–	–30.8	–	dBm

Table 32. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2545–2575 MHz [4]	XGP Band	–	–29.5	–	dBm
π/4 DPSK (2 Mbps)[2]					
698–716 MHz	WCDMA	–	–9.8	–	dBm
776–794 MHz	WCDMA	–	–9.7	–	dBm
824–849 MHz	GSM850	–	–10.7	–	dBm
824–849 MHz	WCDMA	–	–11.4	–	dBm
880–915 MHz	E-GSM	–	–10.4	–	dBm
880–915 MHz	WCDMA	–	–10.2	–	dBm
1710–1785 MHz	GSM1800	–	–15.8	–	dBm
1710–1785 MHz	WCDMA	–	–15.4	–	dBm
1850–1910 MHz	GSM1900	–	–16.6	–	dBm
1850–1910 MHz	WCDMA	–	–16.4	–	dBm
1880–1920 MHz	TD-SCDMA	–	–17.9	–	dBm
1920–1980 MHz	WCDMA	–	–16.8	–	dBm
2010–2025 MHz	TD-SCDMA	–	–18.6	–	dBm
2500–2570 MHz	WCDMA	–	–20.4	–	dBm
2500–2570 MHz [5]	Band 7	–	–31.9	–	dBm
2300–2400 MHz [6]	Band 40	–	–35.3	–	dBm
2570-2620 MHz [3]	Band 38	–	–31.8	–	dBm
2545-2575 MHz [4]	XGP Band	–	–31.1	–	dBm
8DPSK (3 Mbps)[2]					
698–716 MHz	WCDMA	–	–12.6	–	dBm
776–794 MHz	WCDMA	–	–12.6	–	dBm
824–849 MHz	GSM850	–	–12.7	–	dBm
824–849 MHz	WCDMA	–	–13.7	–	dBm
880–915 MHz	E-GSM	–	–12.8	–	dBm
880–915 MHz	WCDMA	–	–12.6	–	dBm
1710–1785 MHz	GSM1800	–	–18.1	–	dBm
1710–1785 MHz	WCDMA	–	–17.4	–	dBm
1850–1910 MHz	GSM1900	–	–19.1	–	dBm
1850–1910 MHz	WCDMA	–	–18.6	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.3	–	dBm
1920–1980 MHz	WCDMA	–	–18.9	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.4	–	dBm
2500–2570 MHz	WCDMA	–	–21.4	–	dBm
2500–2570 MHz [5]	Band 7	–	–31.0	–	dBm
2300–2400 MHz [6]	Band 40	–	–34.5	–	dBm
2570–2620 MHz [3]	Band 38	–	–31.2	–	dBm
2545–2575 MHz [4]	XGP Band	–	–30.0	–	dBm

Table 32. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Spurious Emissions					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
851–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

1. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.1 specification.

2. Bluetooth reference level is taken at the 3 dB RX desense on each of the modulation schemes.

3. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.

4. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.

5. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.

6. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.

Table 33. Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		11.0	13.0	–	dBm
QPSK TX Power at Bluetooth		8.0	10.0	–	dBm
8PSK TX Power at Bluetooth		8.0	10.0	–	dBm
Power control step		2	4	8	dB
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20.0	dBm
|M – N| ≥ 2.5 MHz[1]		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [2, 3]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [b, 4, 5]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor[6]					
65–108 MHz	FM RX	–	–147	–	dBm/Hz
776–794 MHz	CDMA2000	–	–147	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–147	–	dBm/Hz
925–960 MHz	E-GSM	–	–147	–	dBm/Hz
1570–1580 MHz	GPS	–	–146	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–145	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–144	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–141	–	dBm/Hz
2500–2570 MHz	Band 7	–	–140	–	dBm/Hz
2300–2400 MHz	Band 40	–	–140	–	dBm/Hz
2570–2620 MHz	Band 38	–	–140	–	dBm/Hz
2545–2575 MHz	XGP Band	–	–140	–	dBm/Hz

1. The typical number is measured at ±3 MHz offset.

2. The maximum value represents the value required for Bluetooth qualification as defined in the v4.1 specification.

3. The spurious emissions during Idle mode are the same as specified in Table 33.

4. Specified at the Bluetooth Antenna port.

5. Meets this specification using a front-end band-pass filter.

6. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See Figure 29 for location of the port.

Table 34. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[1]	140	155	175	kHz
10101010 sequence in payload[2]	115	140	–	kHz
Channel spacing	–	1	–	MHz

1. This pattern represents an average deviation in payload.

2. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 35. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402		2480	MHz
RX sense[1]	GFSK, 0.1% BER, 1 Mbps	–	–95.5	–	dBm
TX power[2]	–	–	8.5	–	dBm
Mod Char: delta F1 average	–	225	255	275	kHz
Mod Char: delta F2 max[3]	–	99.9	–	–	%
Mod Char: ratio	–	0.8	0.95	–	%

1. Dirty TX is On.

2. BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm out. The BLE TX power at the antenna port cannot exceed the 10 dBm specification limit.

3. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz

15. WLAN RF Specifications

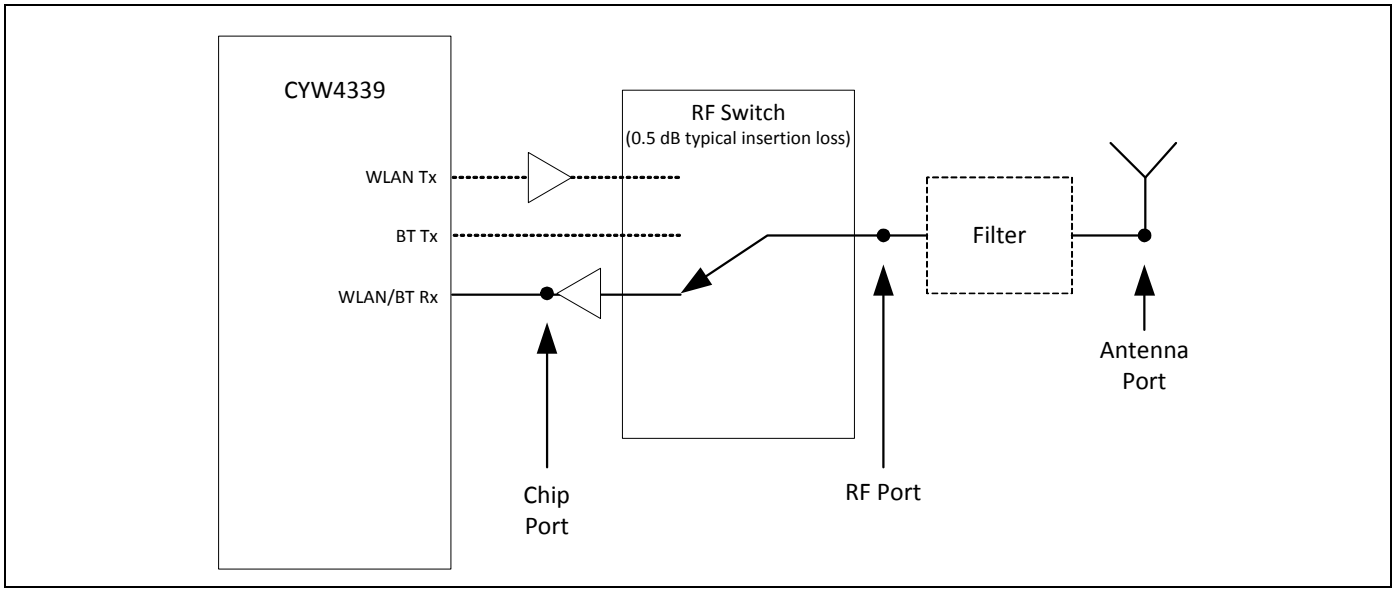
15.1 Introduction

The CYW4339 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radio.

Unless otherwise stated, limit values apply for the conditions specified inTable 29, “Environmental Ratings,” and Table 31, “Recommended Operating Conditions and DC Characteristics,”. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 30. Port Locations Showing Optional ePA and eLNA (Applies to 2.4 GHz and 5 GHz)



15.2 All WLAN specifications are specified at the RF port, unless otherwise specified.**2.4 GHz Band General RF Specifications**

Table 36. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

15.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 37 are specified at the RF port and include the use of an external FEM with LNA from Cypress's approved-vendor list (AVL), unless otherwise specified. Results with FEMs that are not on Cypress's AVL are not guaranteed.

Table 37. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)[1]	1 Mbps DSSS	–	–98.4	–	dBm
	2 Mbps DSSS	–	–96.5	–	dBm
	5.5 Mbps DSSS	–	–93.7	–	dBm
	11 Mbps DSSS	–	–91.4	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–95.5	–	dBm
	9 Mbps OFDM	–	–94.1	–	dBm
	12 Mbps OFDM	–	–93.2	–	dBm
	18 Mbps OFDM	–	–90.6	–	dBm
	24 Mbps OFDM	–	–87.3	–	dBm
	36 Mbps OFDM	–	–84.0	–	dBm
	48 Mbps OFDM	–	–79.3	–	dBm
	54 Mbps OFDM	–	–77.8	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a,2.] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–95.0	–	dBm
	MCS1	–	–92.7	–	dBm
	MCS2	–	–90.2	–	dBm
	MCS3	–	–87.1	–	dBm
	MCS4	–	–83.5	–	dBm
	MCS5	–	–78.9	–	dBm
	MCS6	–	–77.3	–	dBm
	MCS7	–	–75.7	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a,3.] Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–92.8	–	dBm
	MCS1	–	–89.9	–	dBm
	MCS2	–	–87.5	–	dBm
	MCS3	–	–84.0	–	dBm
	MCS4	–	–80.9	–	dBm
	MCS5	–	–76.2	–	dBm
	MCS6	–	–74.7	–	dBm
	MCS7	–	–73.3	–	dBm

Table 37. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a,4]. Defined for default parameters: 800 ns GI and non-STBC	20 MHz channel spacing for all MCS rates					
	MCS0		–	–94.3	–	dBm
	MCS1		–	–91.9	–	dBm
	MCS2		–	–90.1	–	dBm
	MCS3		–	–86.9	–	dBm
	MCS4		–	–83.4	–	dBm
	MCS5		–	–78.9	–	dBm
	MCS6		–	–77.3	–	dBm
	MCS7		–	–75.6	–	dBm
	MCS8		–	–71.2	–	dBm
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a,5]. Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates					
	MCS0		–	–91.5	–	dBm
	MCS1		–	–89.0	–	dBm
	MCS2		–	–87.2	–	dBm
	MCS3		–	–84.0	–	dBm
	MCS4		–	–80.8	–	dBm
	MCS5		–	–76.3	–	dBm
	MCS6		–	–74.7	–	dBm
	MCS7		–	–73.3	–	dBm
	MCS8		–	–68.9	–	dBm
	MCS9		–	–67.6	–	dBm
RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	MCS7	20 MHz	–	–77.4	–	dBm
	MCS8	20 MHz	–	–74.7	–	dBm
	MCS7	40 MHz	–	–74.6	–	dBm
	MCS8	40 MHz	–	–71.6	–	dBm
	MCS9	40 MHz	–	–70.1	–	dBm
	MCS7	80 MHz	–	–71.5	–	dBm
	MCS8	80 MHz	–	–68.1	–	dBm
	MCS9	80 MHz	–	–66.0	–	dBm

Table 37. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 3 dB RX sensitivity degradation (without external filtering)[6]	776–794 MHz	CDMA2000	–	–24	–	dBm
	824–849 MHz[7]	cdmaOne	–	–25	–	dBm
	824–849 MHz	GSM850	–	–15	–	dBm
	880–915 MHz	E-GSM	–	–16	–	dBm
	1710–1785 MHz	GSM1800	–	–18	–	dBm
	1850–1910 MHz	GSM1800	–	–19	–	dBm
	1850–1910 MHz	cdmaOne	–	–26	–	dBm
	1850–1910 MHz	WCDMA	–	–26	–	dBm
	1920–1980 MHz	WCDMA	–	–28.5	–	dBm
	2500–2570 MHz	Band 7	–	–45	–	dBm
	2300–2400 MHz	Band 40	–	–50	–	dBm
	2570–2620 MHz	Band 38	–	–45	–	dBm
	2545–2575 MHz	XGP Band	–	–45	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input in-band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
	@ MCS8–9 rates (10% PER, 4095 octets)		–11.5	–	–	dBm
LPF 3 dB bandwidth	–		9	–	36	MHz
Adjacent channel rejection—DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	**Desired and interfering signal 30 MHz apart**					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection—OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB

Table 37. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection MCS0–9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
	MCS8	–59 dBm	–4	–	–	dB
	MCS9	–57 dBm	–6	–	–	dB
Maximum receiver gain	–	–	–	95	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[8]	Range –95 dBm[9] to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

1. Derate by 1.5 dB for –30°C to –10°C and 55°C to 85°C.

2. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.

3. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.

4. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.

5. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.

6. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.

7. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)

8. The minimum and maximum values shown have a 95% confidence level.

9. –95 dBm with calibration at the time of manufacture, –92 dBm without calibration.

15.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 38 include the use of the CYW4339's internal PAs and are specified at the chip port.

Table 38. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (at 18.5 dBm, 100% duty cycle, 1 Mbps CCK)[1]	76–108 MHz	FM RX	–	–148.5	–	dBm/Hz
	776–794 MHz	–	–	–126.5	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–162.5	–	dBm/Hz
	925–960 MHz	E-GSM	–	–162.5	–	dBm/Hz
	1570–1580 MHz	GPS	–	–149.5	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–140.5	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–137.5	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–128.5	–	dBm/Hz
	2500–2570 MHz	Band 7	–	–104.5	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–94.5	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–119.5	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–109.5	–	dBm/Hz
Harmonic level (at 18 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–7.5	–	dBm/ 1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–17.5	–	dBm/ 1 MHz
EVM Does Not Exceed						
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance[2, 3]	802.11b (DSSS/CCK)	–9 dB	–	21.5	–	dBm
	OFDM, BPSK	–8 dB	–	20	–	dBm
	OFDM, QPSK	–13 dB	–	20	–	dBm
	OFDM, 16-QAM	–19 dB	–	19	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	19	–	dBm
	OFDM, 64-QAM (MCS7, HT20)	–27 dB	–	19	–	dBm
	OFDM, 256-QAM (MCS8, VHT20)	–30 dB	–	17	–	dBm
	OFDM, 256-QAM (MCS8, VHT40)	–32 dB	–	17	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees RMS
TX power control dynamic range	–		10	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies across 10 dBm to 20 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port TX	Z_o = 50Ω		–	6	–	dB

1. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

2. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.

3. TX power for Channel 1 and Channel 11 is specified by nonvolatile memory parameters.

15.5 WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 39 are specified at the RF port and include the use of an external FEM with LNA from Cypress's approved-vendor list (AVL), unless otherwise specified. Results with FEMs that are not on Cypress's AVL are not guaranteed.

Table 39. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)[1]	6 Mbps OFDM	–	–94.5	–	dBm
	9 Mbps OFDM	–	–93.1	–	dBm
	12 Mbps OFDM	–	–92.2	–	dBm
	18 Mbps OFDM	–	–89.6	–	dBm
	24 Mbps OFDM	–	–86.3	–	dBm
	36 Mbps OFDM	–	–83	–	dBm
	48 Mbps OFDM	–	–78.3	–	dBm
	54 Mbps OFDM	–	–76.8	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94	–	dBm
	MCS1	–	–91.7	–	dBm
	MCS2	–	–89.2	–	dBm
	MCS3	–	–86.1	–	dBm
	MCS4	–	–82.5	–	dBm
	MCS5	–	–77.9	–	dBm
	MCS6	–	–76.3	–	dBm
	MCS7	–	–74.7	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–91.8	–	dBm
	MCS1	–	–88.9	–	dBm
	MCS2	–	–86.5	–	dBm
	MCS3	–	–83.0	–	dBm
	MCS4	–	–79.9	–	dBm
	MCS5	–	–75.2	–	dBm
	MCS6	–	–73.7	–	dBm
	MCS7	–	–72.3	–	dBm

Table 39. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS0		–	–93.3	–	dBm
	MCS1		–	–90.3	–	dBm
	MCS2		–	–87.9	–	dBm
	MCS3		–	–84.9	–	dBm
	MCS4		–	–81.4	–	dBm
	MCS5		–	–76.7	–	dBm
	MCS6		–	–75.1	–	dBm
	MCS7		–	–74.6	–	dBm
	MCS8		–	–70.2	–	dBm
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates					
	MCS0		–	–90.5	–	dBm
	MCS1		–	–87.4	–	dBm
	MCS2		–	–85.3	–	dBm
	MCS3		–	–82.1	–	dBm
	MCS4		–	–79	–	dBm
	MCS5		–	–73.9	–	dBm
	MCS6		–	–72.4	–	dBm
	MCS7		–	–72.3	–	dBm
	MCS8		–	–67.9	–	dBm
	MCS9		–	–66.6	–	dBm
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI and non-STBC.	80 MHz channel spacing for all MCS rates					
	MCS0		–	–87	–	dBm
	MCS1		–	–83.9	–	dBm
	MCS2		–	–81.9	–	dBm
	MCS3		–	–78.1	–	dBm
	MCS4		–	–75	–	dBm
	MCS5		–	–73	–	dBm
	MCS6		–	–68.5	–	dBm
	MCS7		–	–68.5	–	dBm
	MCS8		–	–64.3	–	dBm
	MCS9		–	–62.7	–	dBm
RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: 800 ns GI, LDPC coding and non-STBC.	MCS7	20 MHz	–	–76.4	–	dBm
	MCS8	20 MHz	–	–73.7	–	dBm
	MCS7	40 MHz	–	–73.6	–	dBm
	MCS8	40 MHz	–	–70.6	–	dBm
	MCS9	40 MHz	–	–69.1	–	dBm
	MCS7	80 MHz	–	–70.5	–	dBm
	MCS8	80 MHz	–	–67.1	–	dBm
	MCS9	80 MHz	–	–65.0	–	dBm

Table 39. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 1 dB RX sensitivity degradation (without external filtering)[2]	776–794 MHz	CDMA2000	–21	–	–	dBm
	824–849 MHz	cdmaOne	–20	–	–	dBm
	824–849 MHz	GSM850	–12	–	–	dBm
	880–915 MHz	E-GSM	–12	–	–	dBm
	1710–1785 MHz	GSM1800	–15	–	–	dBm
	1850–1910 MHz	GSM1800	–15	–	–	dBm
	1850–1910 MHz	cdmaOne	–20	–	–	dBm
	1850–1910 MHz	WCDMA	–21	–	–	dBm
	1920–1980 MHz	WCDMA	–21	–	–	dBm
	2500–2570 MHz	Band 7	–21	–	–	dBm
	2300–2400 MHz	Band 40	–21	–	–	dBm
	2570–2620 MHz	Band 38	–21	–	–	dBm
	2545–2575 MHz	XGP Band	–21	–	–	dBm
Input in-band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps		–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps		–14.5	–	–	dBm
LPF 3 dB bandwidth	–		9	–	36	MHz
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[3] octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	95	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[4]	Range –95 dBm[5] to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB

Table 39. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Return loss	Z_o = 50Ω, across the dynamic range	10	–	13	dB
Receiver cascaded noise figure	At maximum gain	–	4	6	dB

1. Derate by 1.5 dB for –30°C to –10°C and 55°C to 85°C.

2. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.

3. For 65 Mbps, the size is 4096.

4. The minimum and maximum values shown have a 95% confidence level.

5. –95 dBm with calibration at the time of manufacture, –92 dBm without calibration.

15.6 WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 39 include the use of the CYW4339's internal PAs and are specified at the chip port.

Table 40. WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (at 18.5 dBm)[1]	76–108 MHz	FM RX	–	–161.5	–	dBm/Hz
	776–794 MHz	–	–	–161.5	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–161.5	–	dBm/Hz
	925–960 MHz	E-GSM	–	–161.5	–	dBm/Hz
	1570–1580 MHz	GPS	–	–161.5	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–159.5	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–161.5	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–158.5	–	dBm/Hz
	2400–2483 MHz	BT/WLAN	–	–156.5	–	dBm/Hz
	2500–2570 MHz	Band 7	–	–156.5	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–156.5	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–156.5	–	dBm/Hz
	2545–2575 MHz	XGP band	–	–156.5	–	dBm/Hz
Harmonic level (at 17 dBm)	9.8–11.570 GHz	2nd harmonic	–	–30.5	–	dBm/MHz
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance[2, 3]	OFDM, QPSK	–13 dB	–	21.5	–	dBm
	OFDM, 16-QAM	–19 dB	–	19	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	19	–	dBm
	OFDM, 64-QAM (MCS7, HT20)	–27 dB	–	19	–	dBm
	OFDM, 256-QAM (MCS8, VHT80)	–30 dB	–	17	–	dBm
	OFDM, 256-QAM (MCS9, VHT40 and VHT80)	–32 dB	–	17	–	dBm
Phase noise	37.4 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees RMS
TX power control dynamic range	–		10	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.		–	–	±2.0	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

1. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

2. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.

3. TX power for Channel 1 and Channel 11 is specified by non-volatile memory parameters.

15.7 General Spurious Emissions Specifications

Table 41. General Spurious Emissions Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–93	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–45.5	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–72	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–87	–	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–107	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–65[1]	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–87	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–100	–	dBm

1. The value presented in this table is the result of LO leakage at 3/2 * f_c for 2.4 GHz or 2/3 * f_c for 5 GHz (where f_c is the carrier frequency). For all other emissions in this range, the value is –96 dBm.

16. Internal Regulator Electrical Specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

16.1 Core Buck Switching Regulator

Table 42. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	5.25[1]	V
PWM mode switching frequency	CCM, Load > 100 mA VBAT = 3.6V	2.8	4	5.2	MHz
PWM output current	–	–	–	600	mA
Output current limit	–	–	1400		mA
Output voltage range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max. Ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load	78	86	–	%
PFM mode efficiency	10 mA load current	70	81	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	–	850	µs
External inductor	0806 size, ± 30%, 0.11 ± 25% Ohms	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, ± 20%, 6.3V	2.0[2]	4.7	10[3]	µF

Table 42. Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

1. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V (for up to 250 seconds), cumulative duration over the lifetime of the device, are allowed.

2. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

3. Total capacitance includes those connected at the far end of the active load.

16.2 3.3V LDO (LDO3P3)

Table 43. LDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	5.25[1]	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V	–	3.3	–	V
Dropout voltage	At max load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	–	100	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[2]	4.7	10	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

1. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V (for up to 250 seconds), cumulative duration over the lifetime of the device, are allowed.

2. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.3 2.5V LDO (BTLDO2P5)

Table 44. BTLDO2P5 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage	Min. = 2.5V + 0.2V = 2.7V. Dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	5.25[1]	V
Nominal output voltage	Default = 2.5V.	–	2.5	–	V
Output voltage programmability	Range	2.2	2.5	2.8	V
	Accuracy at any step (including line/load regulation), load > 0.1 mA.	–5	–	5	%
Dropout voltage	At maximum load.	–	–	200	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load.	–	8	16	µA
	Maximum load at 70 mA.	–	660	700	µA
Leakage current	Power-down mode.	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, maximum load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, V_{in} = 3.6V.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 2.5V, C_o = 2.2 µF, maximum load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	150	µs
In-rush current	$V_{in} = V_o$ + 0.15V to 4.8V, C_o = 2.2 µF, No load.	–	–	250	mA
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5–240 mΩ), ±10%, 10V	0.7[2]	2.2	2.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	–	4.7	–	µF

1. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V (for up to 250 seconds), cumulative duration over the lifetime of the device, are allowed.

2. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

16.4 CLDO

Table 45. CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	300	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	24	–	µA
	300 mA load	–	2.1	–	mA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage current	Power down	–	–	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF	20	–		dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.32[1]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.5 LNLDO

Table 46. LNLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. = $1.2V_o$ + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps.Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
	Max. load	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, max load	–	–	5	mV/V
Load regulation	Load from 1 mA to 150 mA	–	0.02	0.05	mV/mA
Leakage current	Power-down	–	–	10	µA
Output noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	140	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[1]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

17. System Power Consumption

Note: Unless otherwise stated, these values apply for the conditions specified in Table 31, "Recommended Operating Conditions and DC Characteristics,".

17.1 WLAN Current Consumption

Table 47 shows the typical, total current consumed by the CYW4339. To calculate total-solution current consumption for designs using external PAs, LNAs, and/or FEMs, add the current consumption of the external devices to the numbers in Table 47.

All values in Table 47 are with the Bluetooth core in reset (that is, with Bluetooth off).

Table 47. Typical WLAN Current Consumption (CYW4339 Current Only)

Mode	Bandwidth (MHz)	Band (GHz)	VBAT = 3.6V, VDDIO = 1.8V, T_A 25°C	
			Vbat, mA	Vio[1], µA
Sleep Modes				
OFF[2]	–	–	0.005	5
SLEEP[3]	–	–	0.005	150
IEEE Power Save, DTIM 1[4]	–	2.4	0.850	150
IEEE Power Save, DTIM 3[4]	–	2.4	0.350	150
IEEE Power Save, DTIM 1[4]	–	5	0.550	150
IEEE Power Save, DTIM 3[4]	–	5	0.300	150
Active Modes				
Receive[5,6] MCS8 (SGI)	20	2.4	50	5
CRS[7]	20	2.4	46	5
Receive[5,6] MCS7 (SGI)	20	5	66	5
CRS[7]	20	5	56	5
Receive[5,6] MCS7 (SGI)	40	5	79.5	5
CRS[7]	40	5	67	5
Receive[5,6] MCS9 (SGI)	80	5	110	5
CRS[7]	80	5	103	5
Active Modes with Internal PAs (TX Output Power Measured at the Chip Port)				
TX CCK 11 Mbps at 21.7 dBm	20	2.4	325	5
TX OFDM MCS8 (SGI) at 17.2 dBm	20	2.4	240	5
TX OFDM MCS7 (SGI) at 18.5 dBm	20	5	280	5
TX OFDM MCS7 at 18.7 dBm	40	5	340	5
TX OFDM MCS9 (SGI) at 16.2 dBm	40	5	270	5
TX OFDM MCS9 (SGI) at 15.7 dBm	80	5	270	5

Table 47. Typical WLAN Current Consumption (CYW4339 Current Only) (Cont.)

Mode	Bandwidth (MHz)	Band (GHz)	VBAT = 3.6V, VDDIO = 1.8V, T_A 25°C	
			Vbat, mA	Vio[1], µA
Active Modes with External PAs (TX Output Power is –5 dBm at the Chip Port)				
Transmit, CCK	20	2.4	88	5
Transmit, MCS8, HT20, SGI[5, 8]	20	2.4	76	5
Transmit, MCS7, SGI[5, 8]	20	5	111	5
Transmit, MCS7[5, 8]	40	5	125	5
Transmit, MCS9, SGI[5, 8]	40	5	125	5
Transmit, MCS9, SGI[5, 8]	80	5	147	5

1. VIO is specified with all pins idle (not switching) and not driving any loads.

2. WL_REG_ON, BT_REG_ON low.

3. Idle, not associated, or inter-beacon.

4. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over the specified DTIM intervals.

5. Measured using packet engine test mode.

6. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.

7. Carrier sense (CCA) when no carrier present.

8. Duty cycle is 100%. Excludes external PA contribution.

17.2 Bluetooth Current Consumption

The Bluetooth, and Bluetooth BLE current consumption measurements are shown in Table 48.

Note:

- The WLAN core is in reset (WLAN_REG_ON = low) for all measurements provided in Table 48.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 48. Bluetooth BLE Current Consumption

Operating Mode	VBAT (VBAT = 3.6V) Typical	VDDIO (VDDIO = 1.8V) Typical	Units
Sleep	10	225	µA
Standard 1.28s Inquiry Scan	180	235	µA
P and I Scan[2]	320	235	µA
500 ms Sniff Master	170	250	µA
500 ms Sniff Slave	120	250	µA
DM1/DH1 Master	22.81	0.034	mA
DM3/DH3 Master	28.06	0.044	mA
DM5/DH5 Master	29.01	0.047	mA
3DH5 Master	27.09	0.100	mA
SCO HV3 Master	7.9	0.123	mA
HV3 + Sniff + Scan[1]	11.38	0.180	mA
BLE Scan[2]	175	235	µA
BLE Scan 10 ms	14.09	0.022	mA
BLE Adv – Unconnectable 1.00 sec	69	245	µA
BLE Adv – Unconnectable 1.28 sec	67	235	µA
BLE Adv – Unconnectable 2.00 sec	42	240	µA
BLE Connected 7.5 ms	4.30	0.020	mA
BLE Connected 1 sec	53	240	µA
BLE Connected 1.28 sec	48	240	µA

1. At maximum class 1 TX power, 500 ms sniff, four attempts (slave), P = 1.28s, and I = 2.56s.

2. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

18. Interface Timing and AC Characteristics

18.1 SDIO Timing

18.1.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 31 and Table 49.

Figure 31. SDIO Bus Timing (Default Mode)

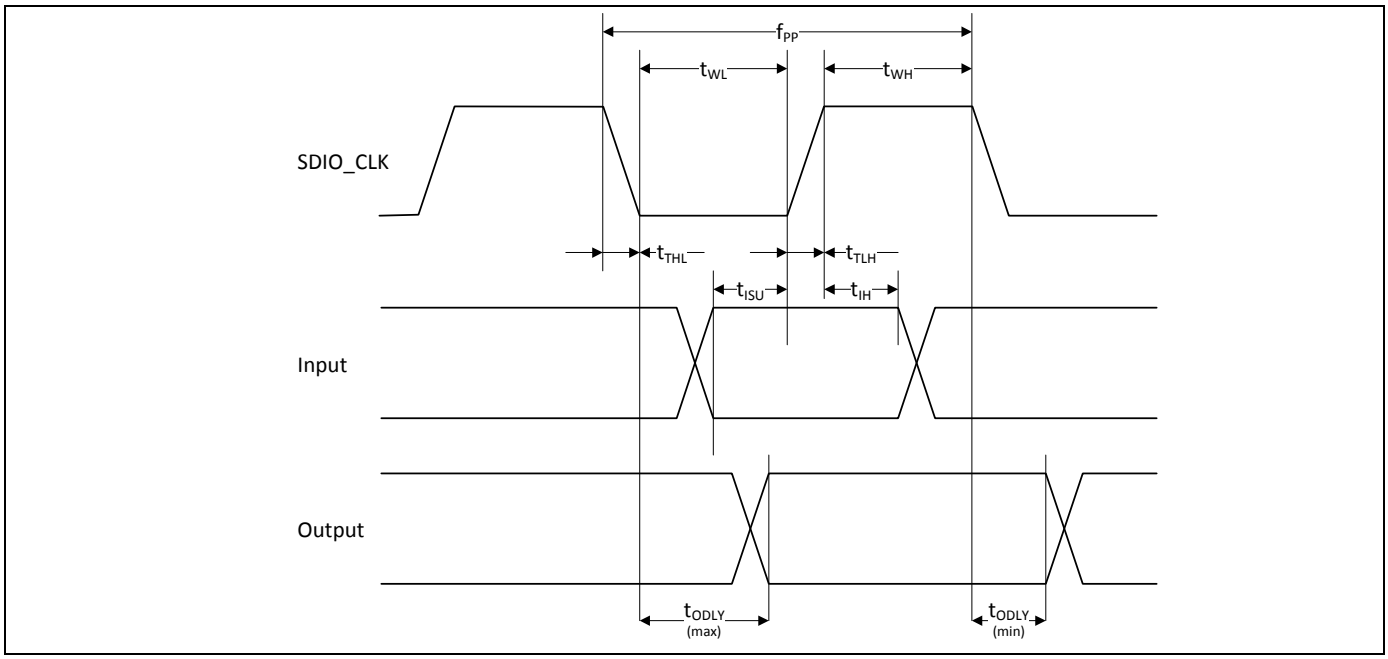


Table 49. SDIO Bus Timing[1] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock fall time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

1. Timing is based on CL ≤ 40pF load on CMD and Data.

2. Min. (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

18.1.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 32 and Table 50.

Figure 32. SDIO Bus Timing (High-Speed Mode)

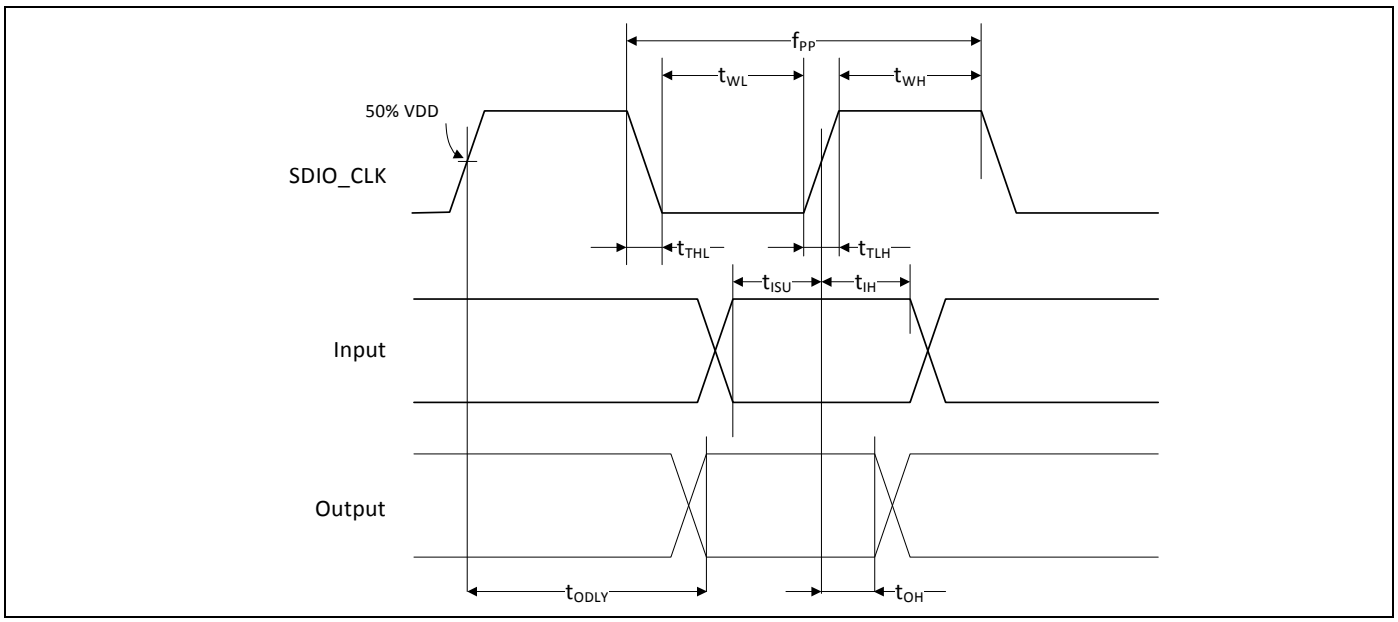


Table 50. SDIO Bus Timing[1] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	–	–	ns
Input hold time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

1. Timing is based on CL ≤ 40pF load on CMD and Data.

2. Min. (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

18.1.3 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 33. SDIO Clock Timing (SDR Modes)

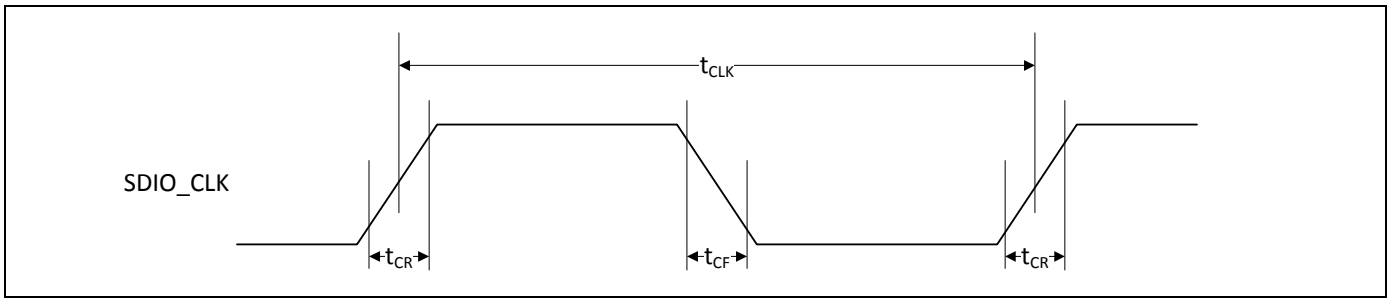


Table 51. SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max.) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max.) @208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

Device Input Timing

Figure 34. SDIO Bus Input Timing (SDR Modes)

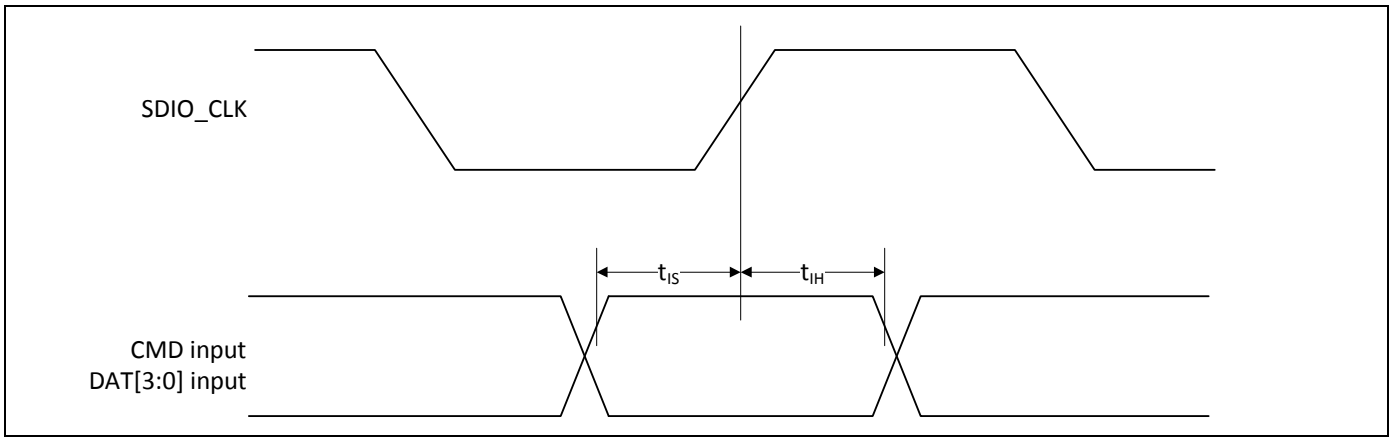


Table 52. SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.0	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR25 Mode				
t_{IS}	3.0	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR12 Mode				
t_{IS}	3.0	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Device Output Timing

Figure 35. SDIO Bus Output Timing (SDR Modes up to 100 MHz)

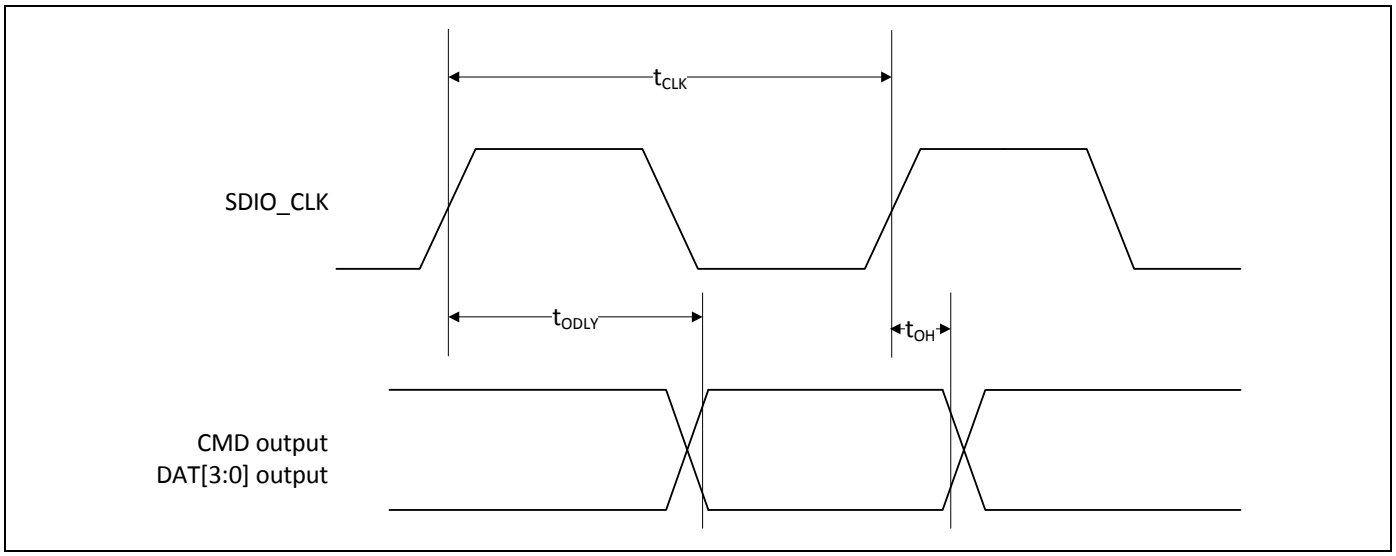


Table 53. SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

Figure 36. SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

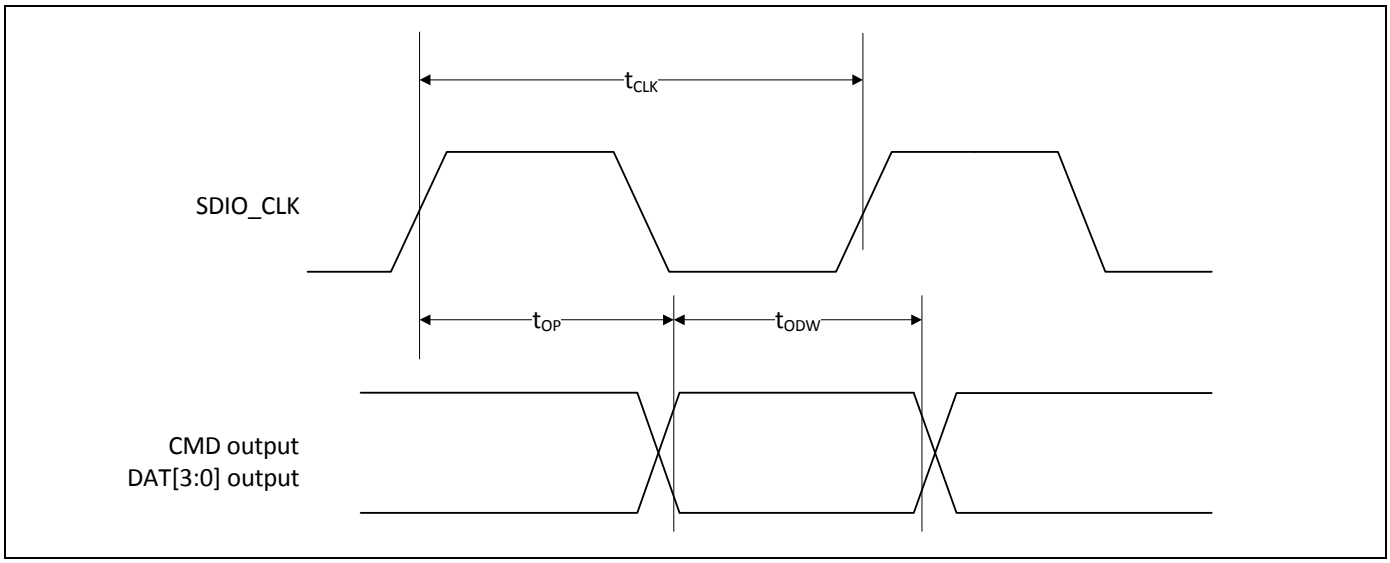
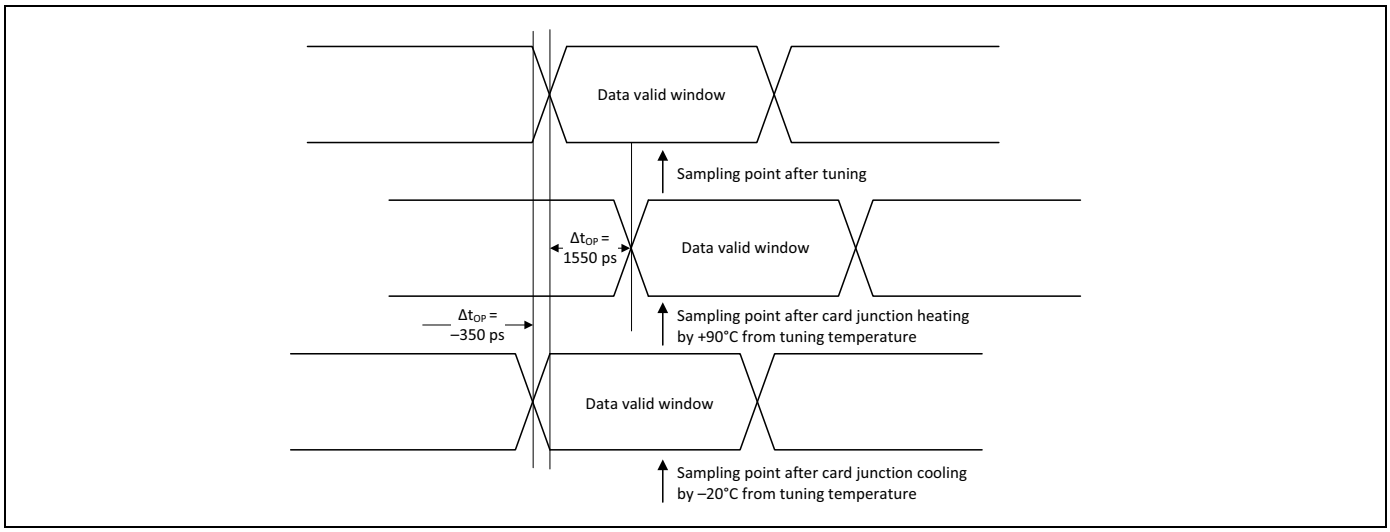


Table 54. SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

Figure 37. Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



18.1.4 SDIO Bus Timing Specifications in DDR50 Mode

Figure 38. SDIO Clock Timing (DDR50 Mode)

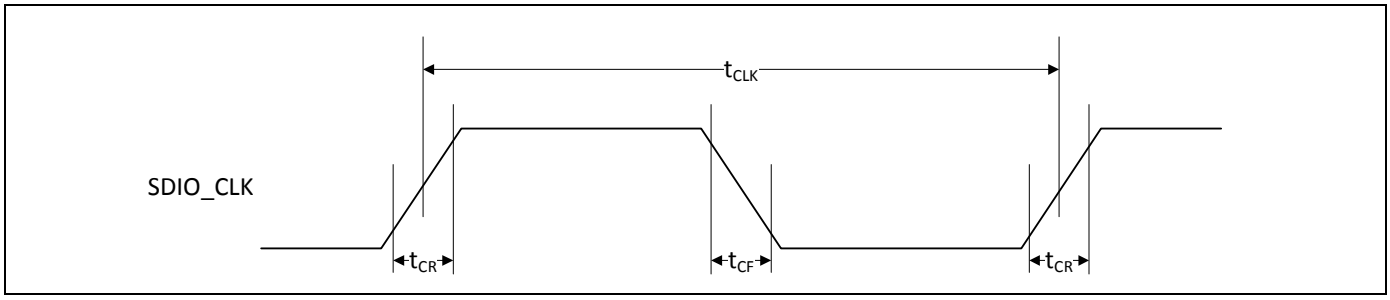


Table 55. SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	45	55	%	–

Data Timing, DDR50 Mode

Figure 39. SDIO Data Timing (DDR50 Mode)

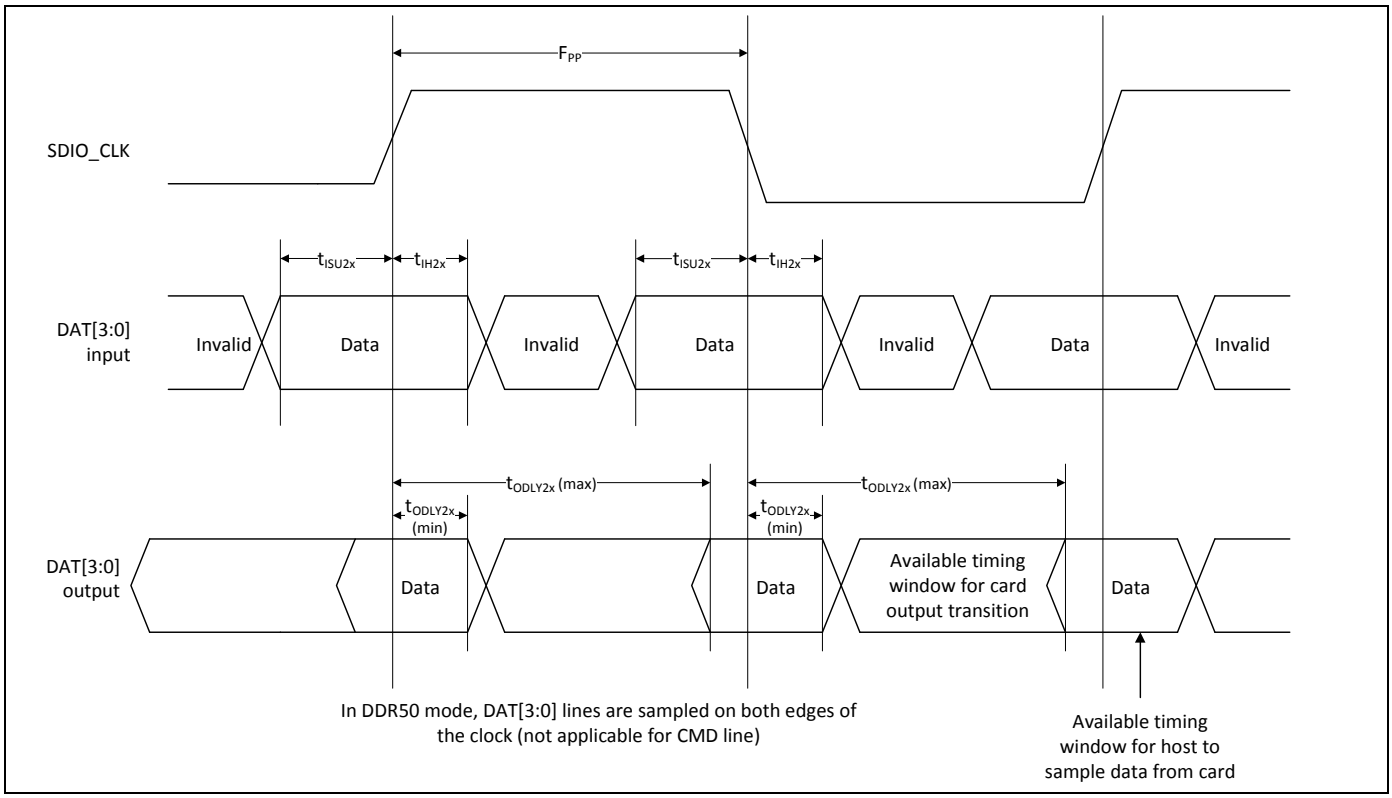


Table 56. SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.0	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15pF (1 Card)

18.2 PCI Express Interface Parameters

Table 57. PCI Express Interface Parameters

Parameter	Symbol	Comments	Minimum	Typical	Maximum	Unit
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock amplitude	Vref	LVPECL, AC coupled	1	–	–	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20	mV

Table 57. PCI Express Interface Parameters (Cont.)

Parameter	Symbol	Comments	Minimum	Typical	Maximum	Unit
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D–	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D–	0	–	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz 8 (min) for 1.25: 2.5 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

18.3 JTAG Timing

Table 58. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

19. Power-Up Sequence and Timing

19.1 Sequencing of Reset and Regulator Control Signals

The CYW4339 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 40, Figure 41, and Figure 42 and Figure 43). The timing values indicated are minimum required values; longer delays are also acceptable.

19.1.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4339 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW4339 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note:

- 2w2For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.
- The CYW4339 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

19.1.2 Control Signal Timing Diagrams

Figure 40. WLAN = ON, Bluetooth = ON

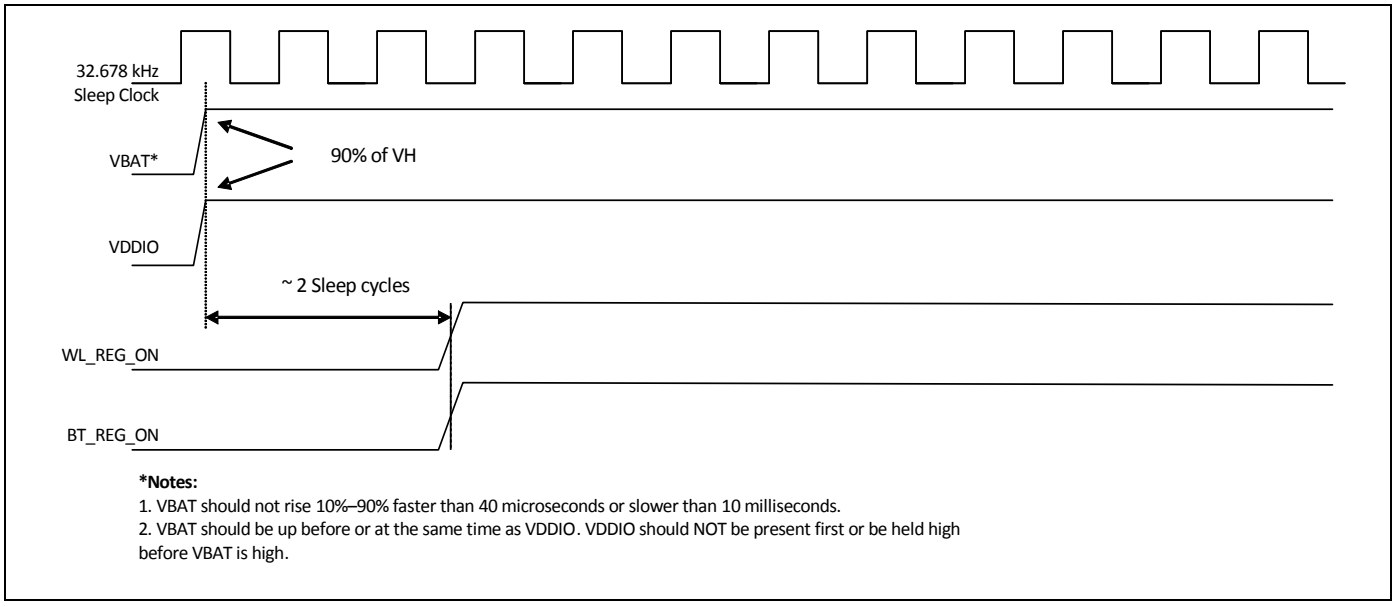
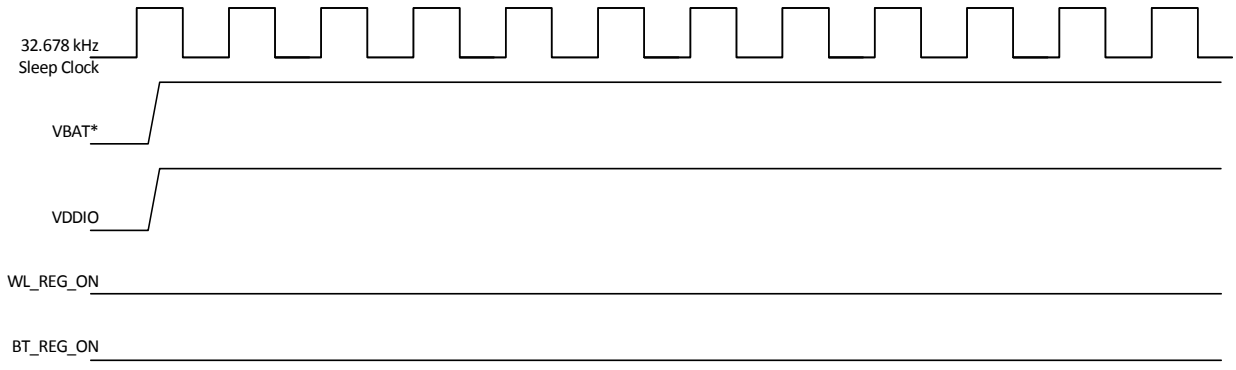
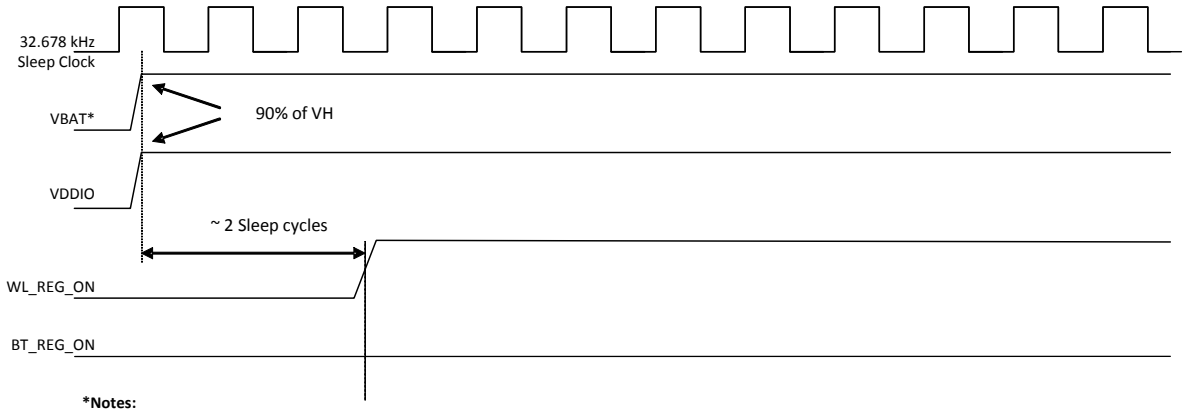


Figure 41. WLAN = OFF, Bluetooth = OFF



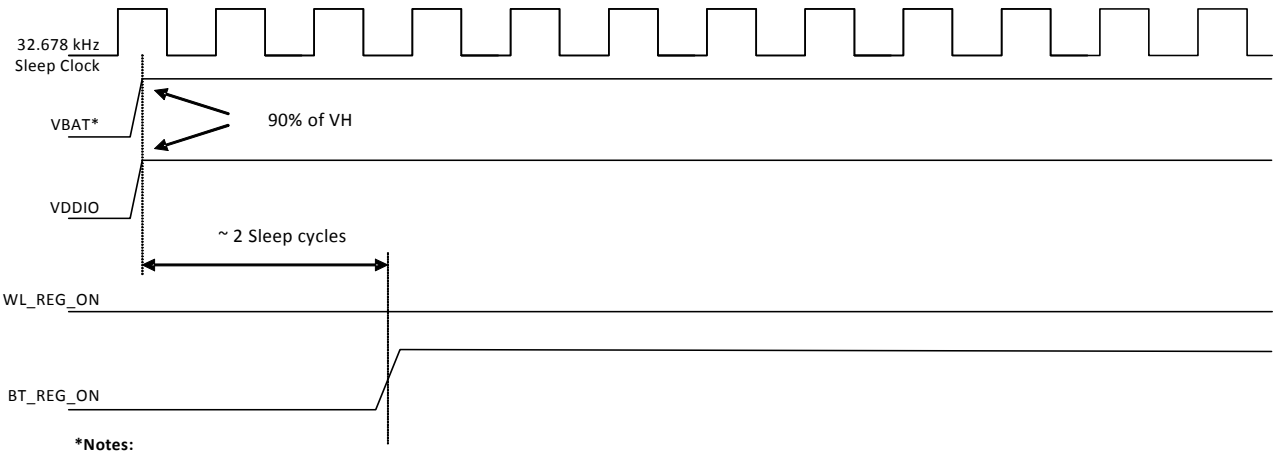
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 42. WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 43. WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

20. Package Information

20.1 Package Thermal Characteristics

Table 59. Package Thermal Characteristics[1]

Characteristic	FCFBGA	WLBGA	WLCSP
θ_{JA} (°C/W) (value in still air)	48.03	32.9	33.45
θ_{JB} (°C/W)	17.01	2.56	3.45
θ_{JC} (°C/W)	24.52	0.98	1.00
Ψ_{JT} (°C/W)	10.78	3.30	3.45
Ψ_{JB} (°C/W)	18.02	9.85	10.64
Maximum Junction Temperature T_j (°C)	125	125	125
Maximum Power Dissipation (W)	1.41	1.119	1.119

1. No heat sink, TA = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = specified power maximum continuous power dissipation.

20.2 Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$TJ = TT + P \times \Psi JT$$

Where:

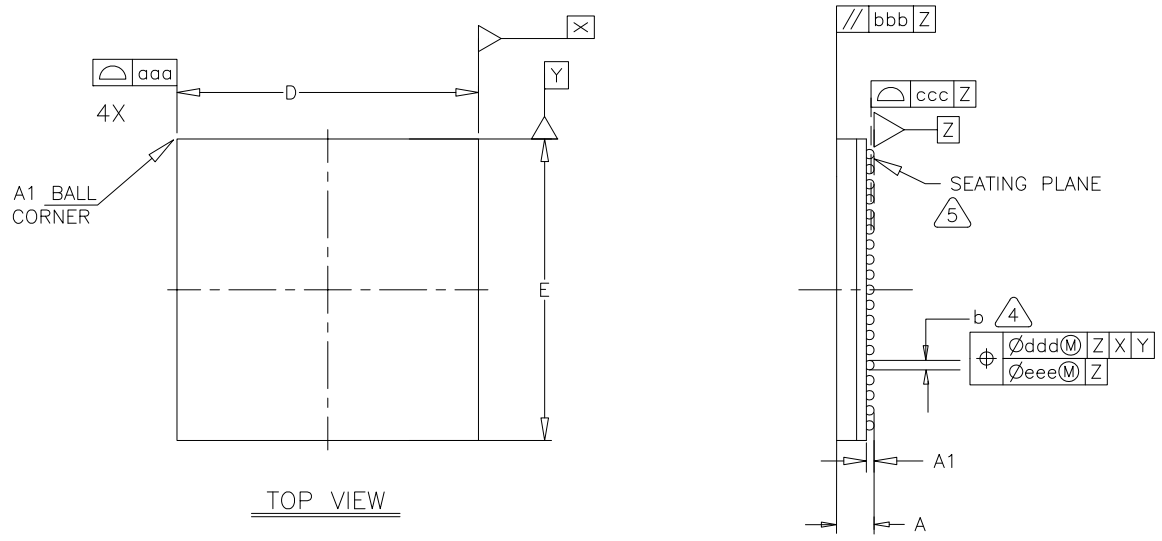
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

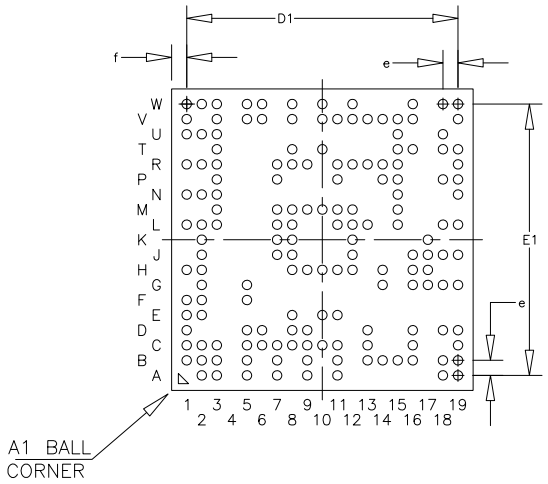
20.3 Environmental Characteristics

For environmental characteristics data, see Table 29, “Environmental Ratings,”.

21. Mechanical Information

Figure 44. 160-Ball FCFBGA Package Mechanical Information





DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.00
A1	0.15	0.18	0.21
D	7.85	8.00	8.15
D1		7.20 BSC	
E	7.85	8.00	8.15
E1		7.20 BSC	
b	0.21	0.26	0.31
e		0.40 BSC	
f	0.30	0.40	0.50
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD01751 Rev: 000

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

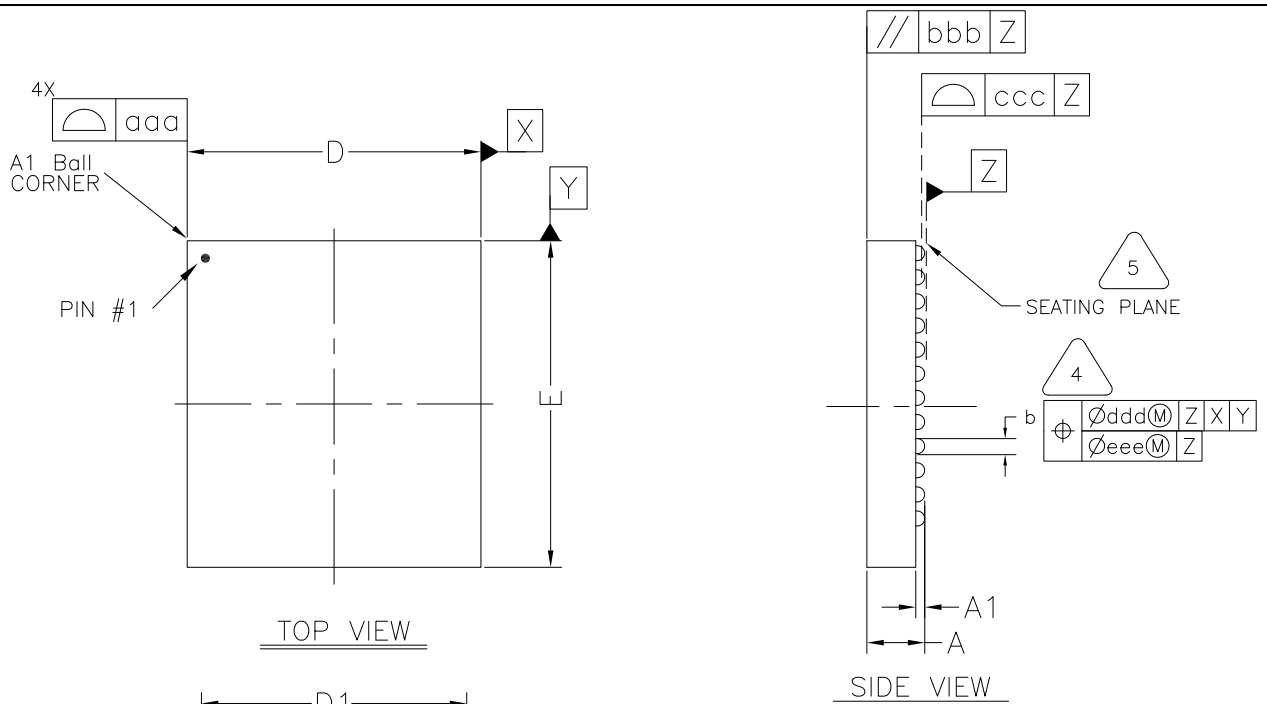
3. THE BASIC SOLDER BALL GRID PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-034.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 45. 145-Ball WLBGA Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	4.83	4.87	4.91
D1		4.40 REF.	
E	5.373	5.413	5.453
E1		4.80 REF.	
b	0.20	0.25	0.30
e		0.40 BSC	
f1		0.235 BSC	
f2		0.378 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD01829 Rev: 000

6. REFER TO BROADCOM APPLICATION NOTE "WAFER–LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 46. WLBGA Keep-out Areas for PCB Layout—Bottom View with Balls Facing Up

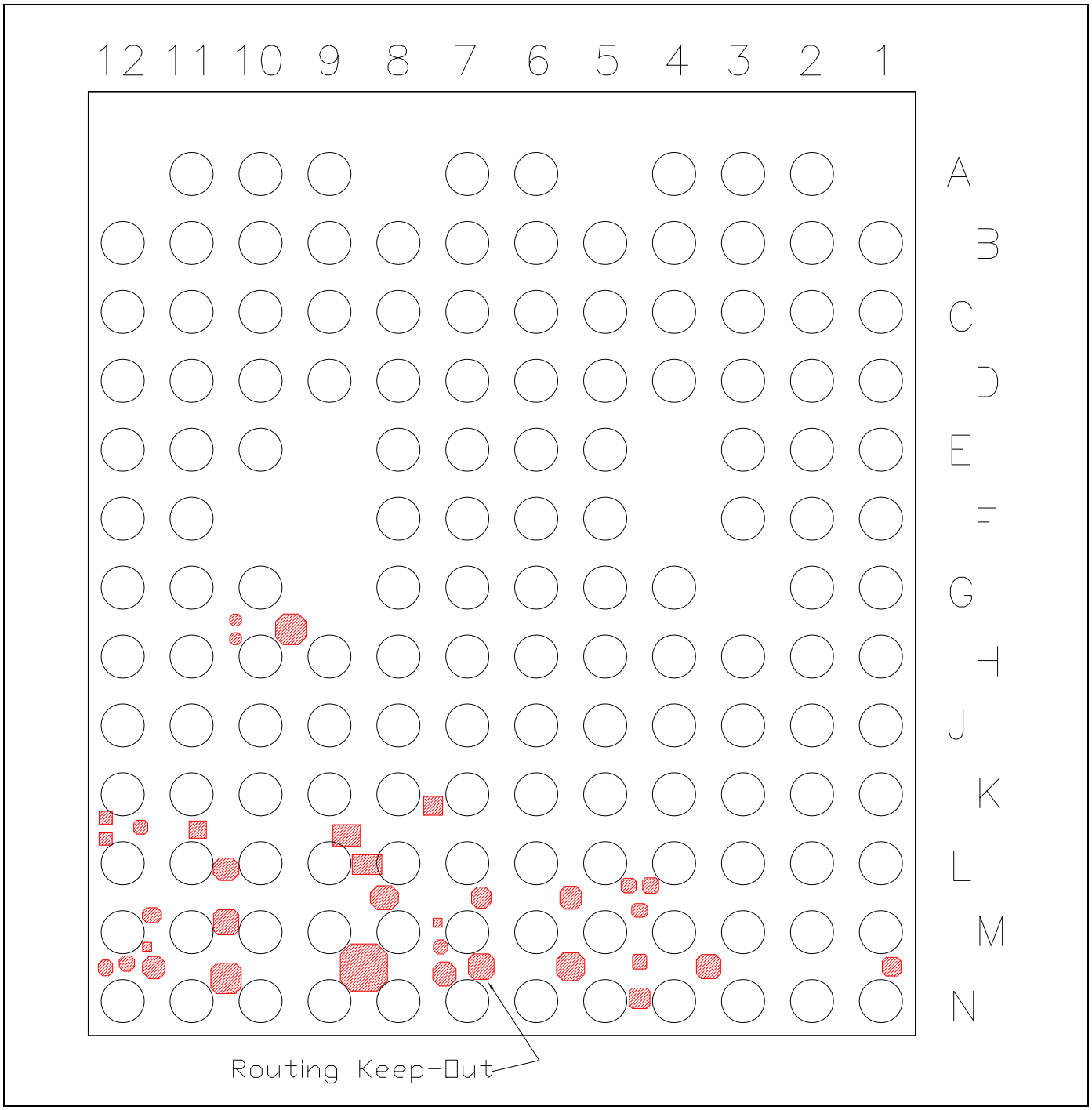
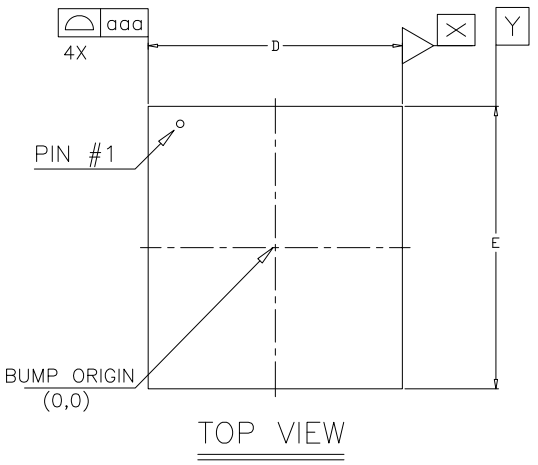
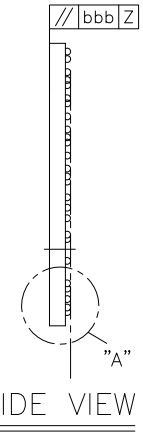
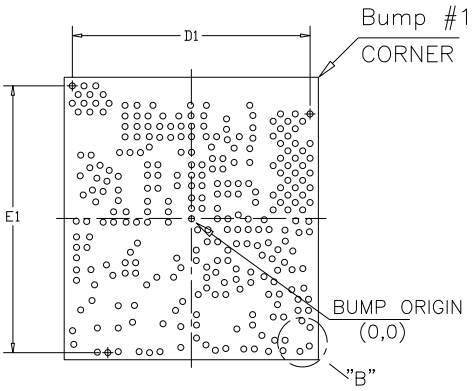
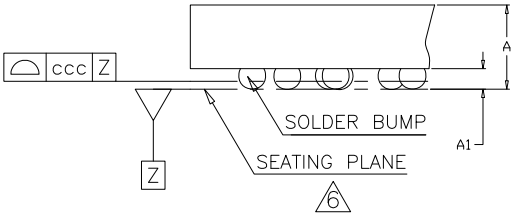


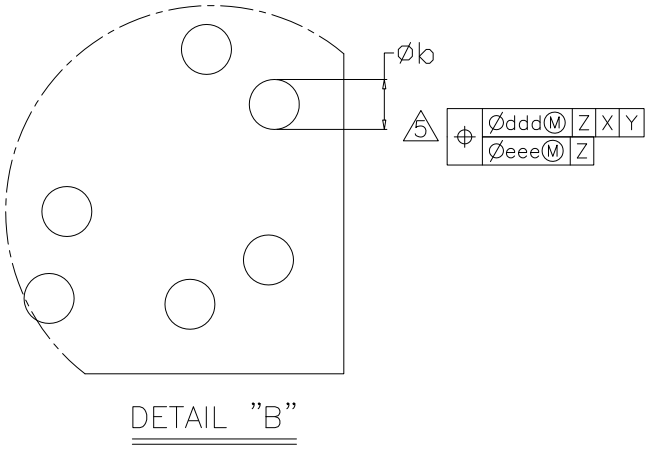
Figure 47. 286-Bump WLCSP Package Mechanical Information











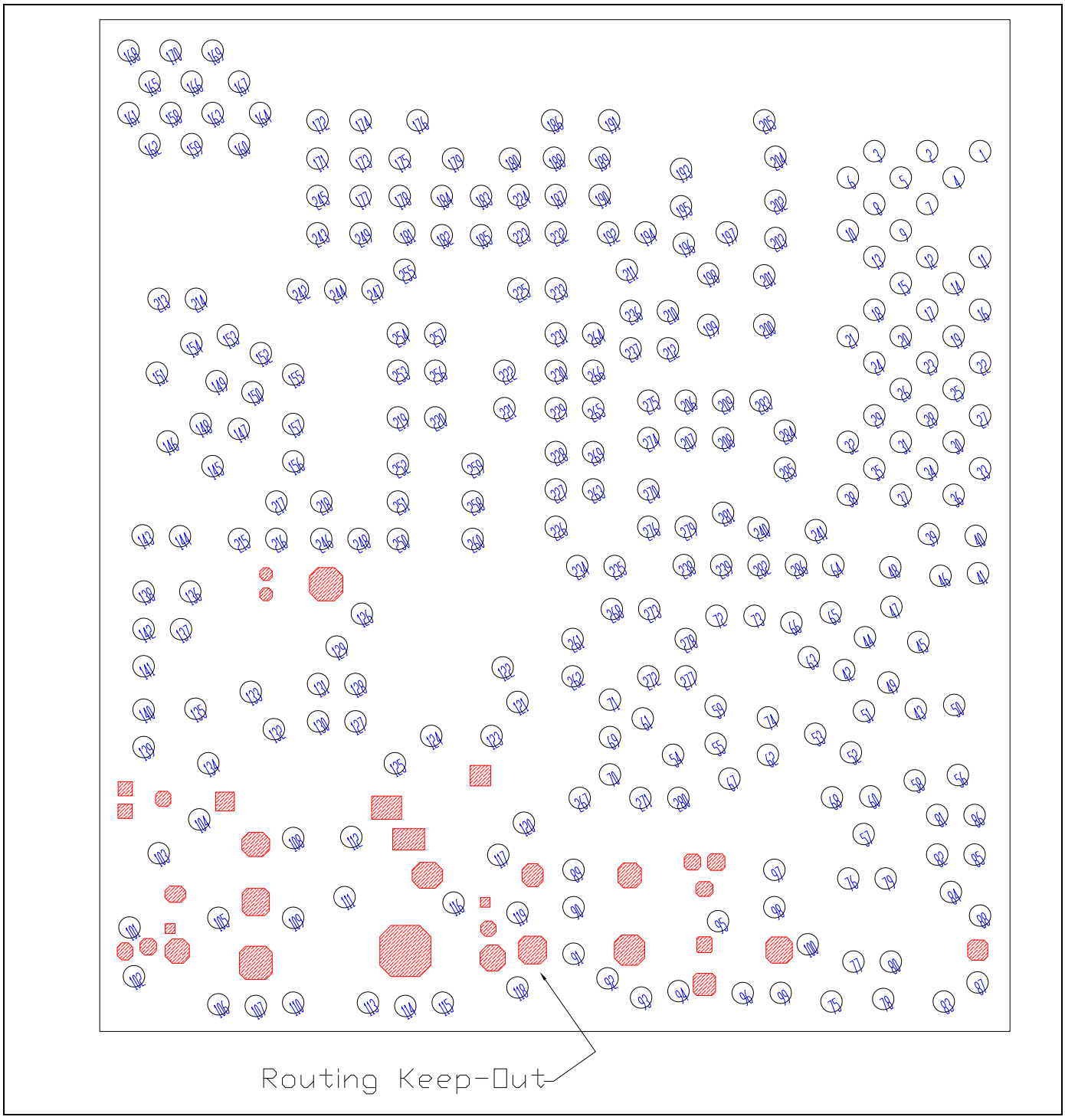
DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.41
A1	0.075	0.090	0.105
D	4.830	4.870	4.910
D1		4.556 BSC	
E	5.373	5.413	5.453
E1		5.112 BSC	
b	0.100	0.115	0.130
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD01828 Rev: 000

6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
4. MINIMUM BUMP PITCH IS 0.200MM
3. REFER TO BROADCOM APPLICATION NOTE "WAFER–SCALE CHIP–SIZED PACKAGE (WSCSP) OVERVIEW AND ASSEMBLY GUIDELINES FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.
2. BUMP POSITION DESIGNATION PER JESD 95–1, SPP–010
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 48. WLCSP Keep-out Areas for PCB Layout—Bottom View with Bumps Facing Up



Note: No top-layer metal is allowed in keep-out areas.

22. Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW4339NKFFBG	160-ball FCFBGA (8 mm × 8 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.1	–30°C to +85°C
CYW4339XKWBG	286-bump WLCSP (4.87 mm × 5.413 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.1	–30°C to +85°C
CYW4339XKUBG	145-ball WLBGA (4.87 mm × 5.413 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.1	–30°C to +85°C

23. IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/)

23.1 References

The references in this section may be used in conjunction with this document.

Note: Cypress provides customer access to technical documentation and software through its https://community.cypress.com and Downloads & Support site (see IoT Resources).

Document (or Item) Name	Number	Source
[1] Bluetooth MWS Coexistence 2-wire Transport Interface Specification	–	wiced-smart

Document History Page

Document Title: CYW4339 Single-Chip 5G WiFi IEEE 802.11ac MAC/Baseband/Radio with Integrated Bluetooth 4.1 Document Number: 002-14784				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	02/15/2013	4339-DS100-R Initial release.
*A	-	-	03/12/2013	4339-DS101-R **Updated:** • Package option dimensions. • Table 19: “286-Bump WLCSP Coordinates,” on page 109 by replacing the PACKAGEOPTION_0 through PACKAGEOPTION_3 signal names with VSSC. • The Power Rail column in Table 31: “I/O States” • Table 32: “Absolute Maximum Ratings”. • Table 35: “Recommended Operating Conditions and DC Characteristics” • Table 43: “WLAN 2.4 GHz Transmitter Performance Specifications” • Table 45: “WLAN 5 GHz Transmitter Performance Specifications”. • “WLAN Current Consumption” • Table 53: “Bluetooth BLE and FM Current Consumption” Figure 77: “145-Ball WLBGA Package Mechanical Information” • Section 24: “Ordering Information”
*B	-	-	07/02/2013	4339-DS102-R **Updated:** • Figure 1: “Functional Block Diagram” • Figure 2: “BCM4339 Block Diagram” • Figure 5: “Typical Power Topology for BCM4339” • Table 20: “FCFBGA, WLBGA, and WLCSP Signal Descriptions” • Table 35: “Recommended Operating Conditions and DC Characteristics,” by changing DC supply voltage for VBAT from 4.8V to 5.25V. • Table 47: “Core Buck Switching Regulator (CBUCK) Specifications,” by changing input supply voltage (DC) Max from 4.8V to 5.25V. • Table 48: “LDO3P3 Specifications,” by changing input supply voltage, VIN Max from 4.8V to 5.25V. • Table 49: “BTLDO2P5 Specifications,” by changing input supply voltage Max from 4.8V to 5.25V. • Table 52: “Typical WLAN Power Consumption (External PA configuration)” • Table 53: “Bluetooth BLE and FM Current Consumption” Section 24: “Ordering Information”
*C	-	-	11/08/2013	4339-DS103-R **Updated:** • BT_VDDO to BT_VDDIO throughout the document. • Table 34: “ESD Specifications”.

Document Title: CYW4339 Single-Chip 5G WiFi IEEE 802.11ac MAC/Baseband/Radio with Integrated Bluetooth 4.1 Document Number: 002-14784				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	-	-	04/02/2014	4339-DS104-R **Updated:** • The cover page and the general features . • By deleting the HSIC interface throughout, leaving pin and signal names unchanged. • By changing to *PCI Express Base Specification (*revision 3.0 compliant Gen1 interface) throughout. • “External Frequency Reference” . • Table 2: “Crystal Oscillator and External Clock — Requirements and Performance” • “Frequency Selection” • Figure 10: “Startup Signaling Sequence” • Figure 22: “UART Timing” • “One-Time Programmable Memory”. • Figure 50: “160-Ball FCFBGA (Top View),” by changing BT_VDDO to BT_VDDIO. • Figure 54: “286-Bump WLCSP (Bottom View)”. • Table 19: “286-Bump WLCSP Coordinates” by changing BT_VDDO to BT_VDDIO. • Table 20: “FCFBGA, WLBGA, and WLCSP Signal Descriptions” by changing BT_VDDO to BT_VDDIO and adding a note to the GPIO pin description. • Table 31: “I/O States” • Table 34: “ESD Specifications” • Table 35: “Recommended Operating Conditions and DC Characteristics,” by changing C_{IN} to C_{OUT}. • Table 36: “Bluetooth Receiver RF Specifications,” by deleting what was footnote e, altering footnote b, and adding footnote b to one additional place. • “Introduction”. • RSSI accuracy in Table 42: “WLAN 2.4 GHz Receiver Performance Specifications” and Table 44: “WLAN 5 GHz Receiver Performance Specifications” • Table 43: “WLAN 2.4 GHz Transmitter Performance Specifications,” and the note preceding it. • Table 45: “WLAN 5 GHz Transmitter Performance Specifications” and the note preceding it. • Section 18: “Internal Regulator Electrical Specifications” “WLAN Current Consumption”. • Figure 65: “SDIO Bus Output Timing (SDR Modes up to 100 MHz)”. • Figure 66: “SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)”.

Document Title: CYW4339 Single-Chip 5G WiFi IEEE 802.11ac MAC/Baseband/Radio with Integrated Bluetooth 4.1 Document Number: 002-14784				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	-	-	05/28/2014	4339-DS105-R **Updated:** • The Features listed in the front matter of the document. • By changing all instances of Bluetooth 4.0 to Bluetooth 4.1 throughout the document. • By removing the word draft after all instances of IEEE 802.11ac throughout the document. • “Features”. • “External 32.768 kHz Low-Power Oscillator”. • “Advanced Bluetooth/WLAN Coexistence”. • “SDIO v3.0”. • Table 20: “FCFBGA, WLBGA, and WLCSP Signal Descriptions” by fixing an incorrect WLBGA ball. The second instance of M12 was changed to M10. • Table 21: “WLAN GPIO Functions and Strapping Options” . • Table 24: “Host Interface Selection (WLBGA and WLCSP Packages)”
*F	-	-	11/17/2014	4339-DS106-R **Updated:** • Table 55: “SDIO Bus Input Timing Parameters (SDR Modes)” .
*G	5450674	UTSV	10/04/2016	Added Cypress Part Numbering Scheme and Mapping Table on Page 1. Updated to Cypress template.
*H	5674872	UTSV	03/29/2017	Removed Sections belong to FM and gSPI throughout the document.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А