

# 74ALVCH16821

20-bit bus-interface D-type flip-flop; positive-edge trigger;  
3-state

Rev. 3 — 2 February 2018

Product data sheet

## 1 General description

The 74ALVCH16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-state output buffer. The two sections of each register are controlled independently by the clock ( $nCP$ ) and output enable ( $n\overline{OE}$ ) control gates.

Each register is fully edge triggered. The state of each  $nDn$  input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's  $nQn$  output.

When  $n\overline{OE}$  is LOW, the data in the register appears at the outputs. When  $n\overline{OE}$  is HIGH, the outputs are in high impedance OFF state. Operation of the  $n\overline{OE}$  input does not affect the state of the flip-flops.

The 74ALVCH16821 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## 2 Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Current drive  $\pm 24$  mA at 3.0 V
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Output drive capability 50  $\Omega$  transmission lines at 85°C
- All data inputs have bushold
- Complies with JEDEC standard no. 8-1A
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

## 3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVCH16821DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4 Functional diagram

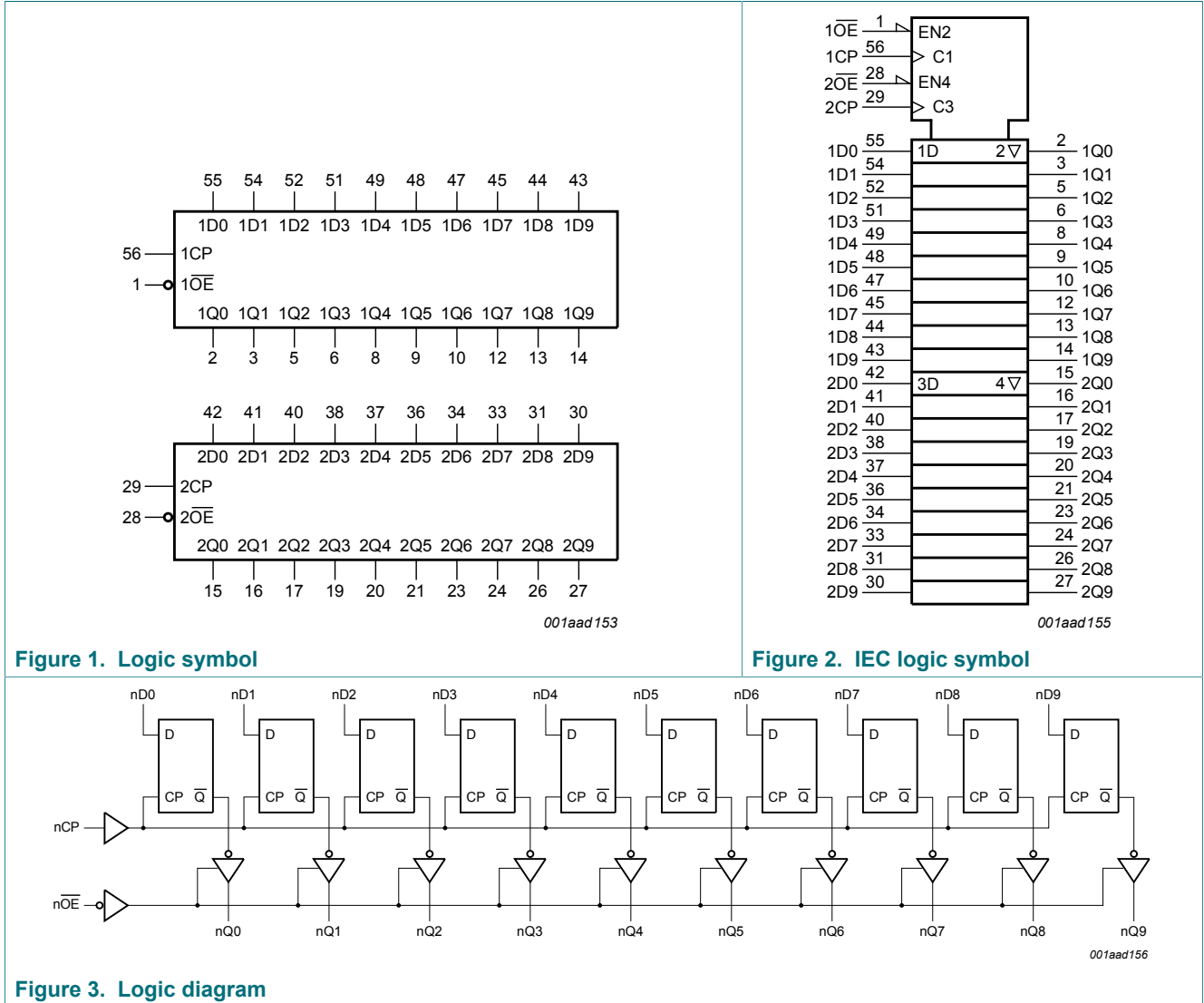


Figure 1. Logic symbol

Figure 2. IEC logic symbol

Figure 3. Logic diagram

## 5 Pinning information

### 5.1 Pinning

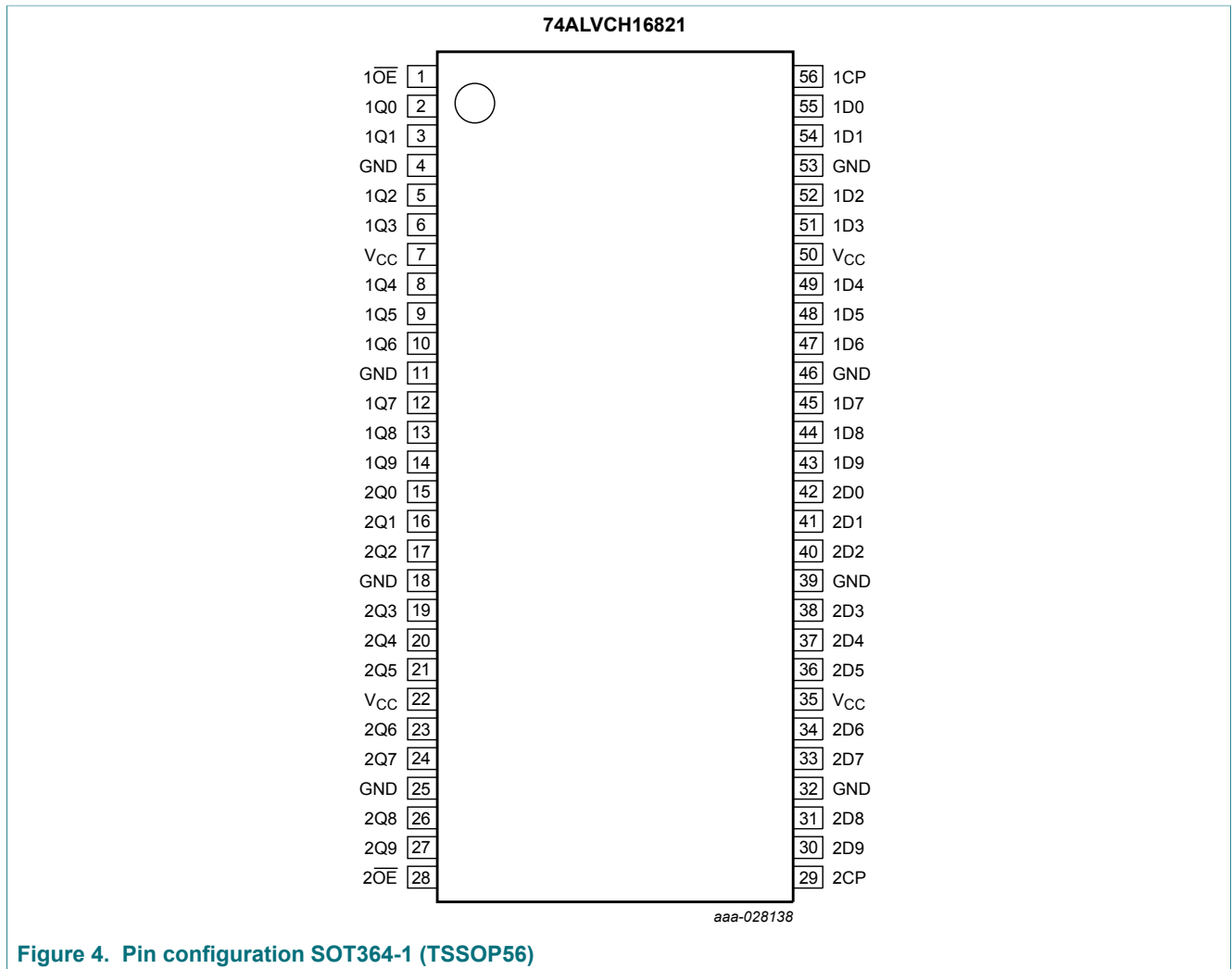


Figure 4. Pin configuration SOT364-1 (TSSOP56)

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8, 1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8, 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8, 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8, 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data outputs
1 $\overline{OE}$ , 2 $\overline{OE}$	1, 28	output enable inputs (active LOW)
1CP, 2CP	56, 29	clock pulse inputs (active rising edge)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V <sub>CC</sub>	7, 22, 35, 50	supply voltage

## 6 Functional description

Table 3. Function table <sup>[1]</sup>

Operating mode	Input			Internal register	Output
	n $\overline{OE}$	nCP	nDn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 NC = no change;  
 X = don't care;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition.

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage	For control pins <sup>[1]</sup>	-0.5	+4.6	V
		For data inputs <sup>[1]</sup>	-0.5	$V_{CC} + 0.5$	V
$V_O$	output voltage	<sup>[1]</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$I_{O(\text{sink/source})}$	output sink or source current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C <sup>[2]</sup>	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

## 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage	2.5 V range for maximum speed performance at 30 pF output load	2.3	2.7	V
		3.3 V range for maximum speed performance at 50 pF output load	3.0	3.6	V
$V_I$	input voltage		0	$V_{CC}$	V
$V_O$	output voltage		0	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	-	10	ns/V

## 9 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions;  $T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$ ; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	GND	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.70	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	10	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	40	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	150	750	μA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V	45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	150	-	μA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V	-45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	-75	-175	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	per data input; V <sub>CC</sub> = 3.6 V	500	-	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	per data input; V <sub>CC</sub> = 3.6 V	-500	-	-	μA
C <sub>I</sub>	input capacitance		-	5.0	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

10 Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
t <sub>pd</sub>	propagation delay	nCP to nQn; see Figure 5 <sup>[2]</sup>				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	5.8	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	5.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	4.5	ns
t <sub>en</sub>	enable time	nOE to nQn; see Figure 7 <sup>[2]</sup>				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.8	6.6	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.2	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.3	5.1	ns
t <sub>dis</sub>	disable time	nOE to nQn; see Figure 7 <sup>[2]</sup>				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	5.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.1	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.8	4.6	ns
t <sub>su</sub>	set-up time	nDn to nCP; see Figure 6				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	0.3	-	ns
		V <sub>CC</sub> = 2.7 V	1.2	0.3	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	0.2	-	ns
t <sub>h</sub>	hold time	nDn to nCP; see Figure 6				
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.4	0.0	-	ns
		V <sub>CC</sub> = 2.7 V	0.6	-0.3	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.8	0.4	-	ns
t <sub>w</sub>	pulse width	nCP HIGH or LOW; see Figure 5				
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.0	1.8	-	ns
		V <sub>CC</sub> = 2.7 V	3.3	1.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.3	0.2	-	ns
f <sub>max</sub>	maximum frequency	nCP; see Figure 5				
		V <sub>CC</sub> = 2.3 V to 2.7 V	150	250	-	MHz
		V <sub>CC</sub> = 2.7 V	150	300	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	150	350	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per latch; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>				
		outputs enabled	-	33	-	pF
		outputs disabled	-	17	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C

Typical values for V<sub>CC</sub> = 2.3 V to 2.7 V are measured at V<sub>CC</sub> = 2.5 V. Typical values for V<sub>CC</sub> = 3.0 V to 3.6 V are measured at V<sub>CC</sub> = 3.3 V.

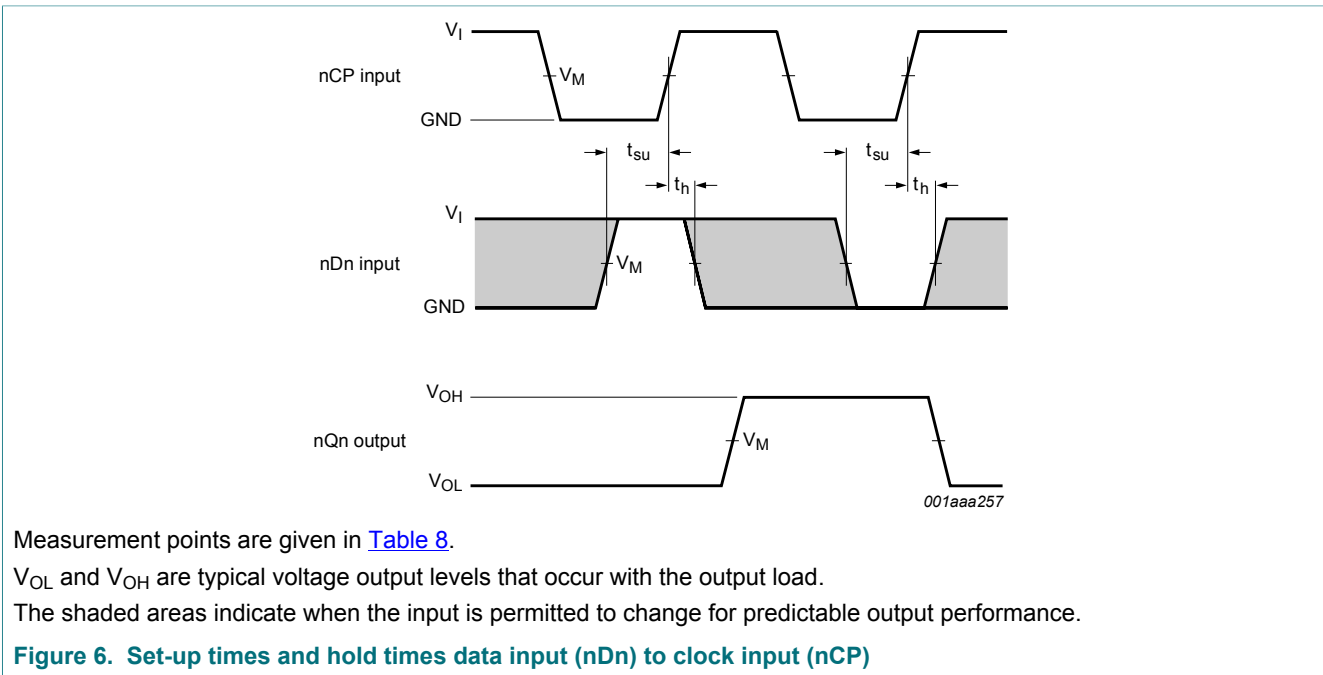
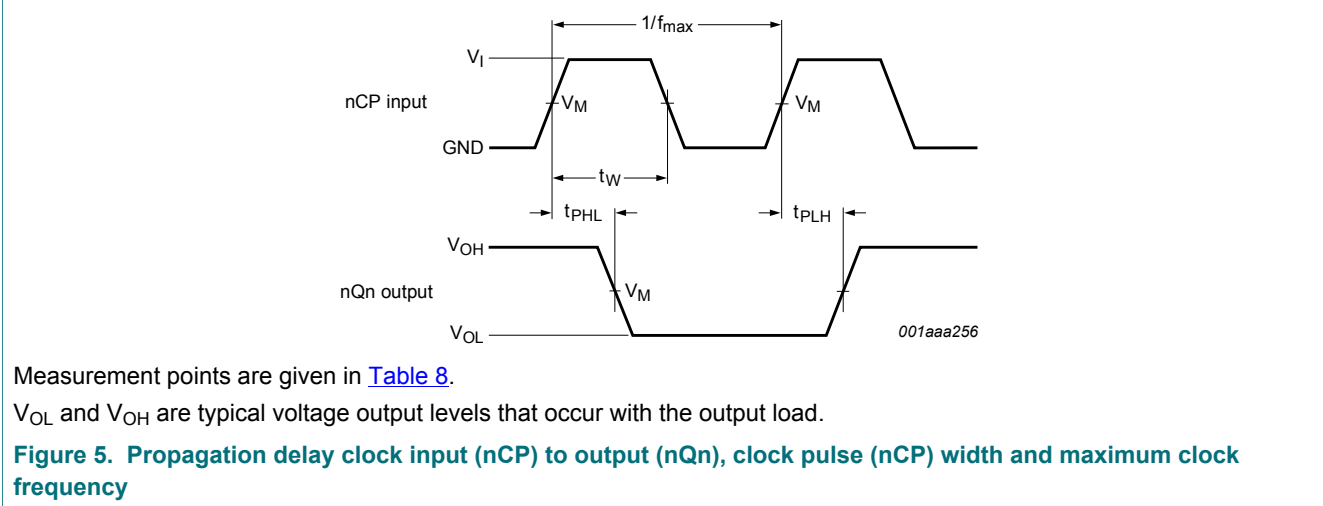
[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>B LZ</sub> and t<sub>B HZ</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW). P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:

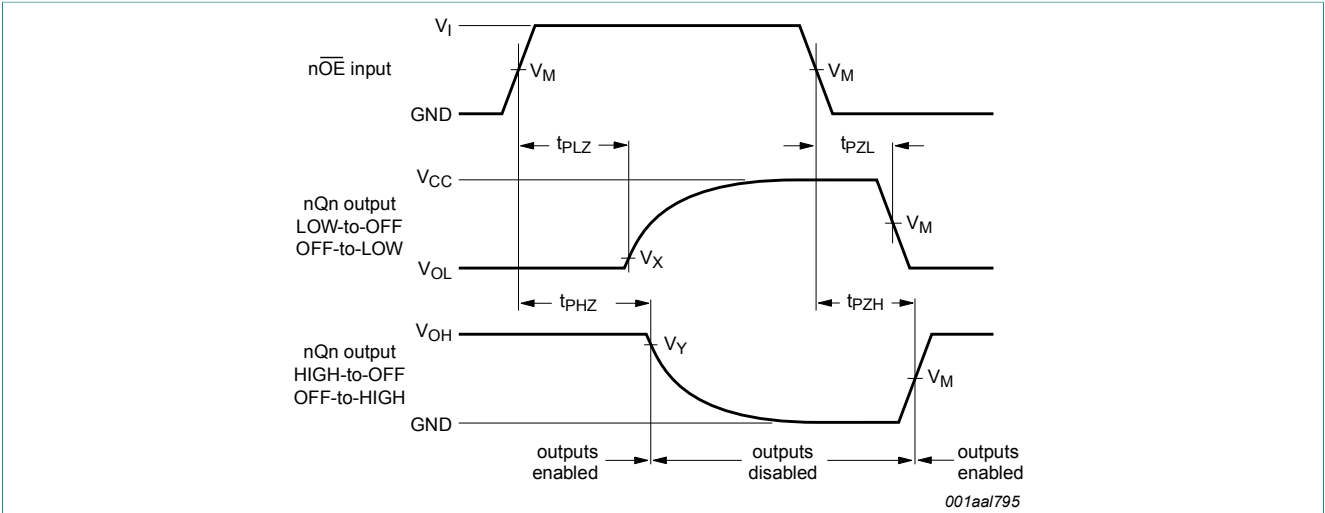
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz; C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts; N = total load switching outputs; ∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

10.1 Waveforms and test circuit







Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Figure 7. OFF-state to HIGH and LOW propagation delays and LOW and HIGH to OFF-state propagation delays**

**Table 8. Measurement points**

$V_{CC}$	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$< 2.7\text{ V}$	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$\geq 2.7\text{ V}$	$2.7\text{ V}$	$1.5\text{ V}$	$1.5\text{ V}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

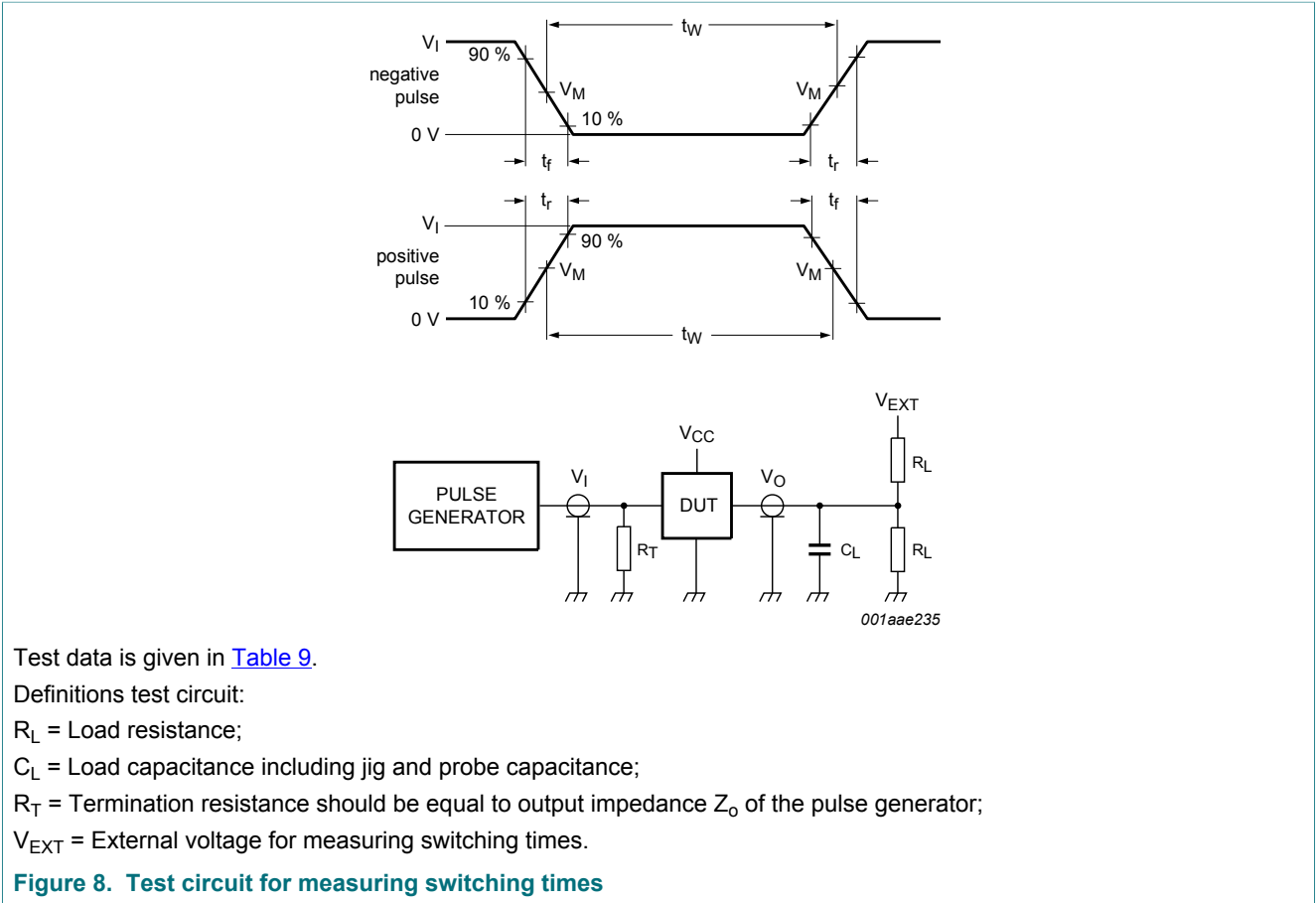


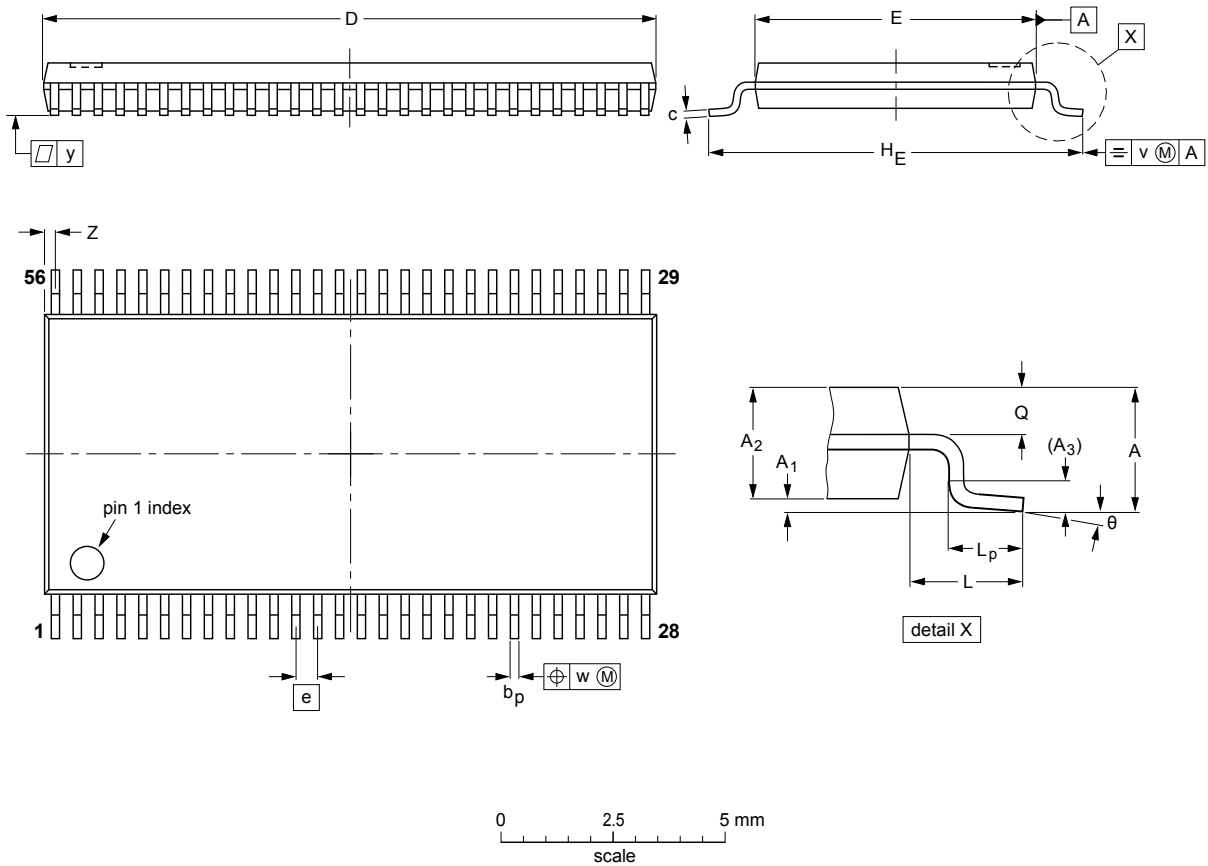
Table 9. Test data

Input			Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$R_L$	$C_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
< 2.7 V	$V_{CC}$	$\leq 2.0$ ns	500 $\Omega$	30 pF	GND	$2 \times V_{CC}$	open
$\geq 2.7$ V	2.7 V	$\leq 2.5$ ns	500 $\Omega$	50 pF	GND	$2 \times V_{CC}$	open

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT364-1		MO-153			99-12-27 03-02-19

Figure 9. Package outline SOT364-1 (TSSOP56)

## 12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16821 v.3	20180202	Product data sheet	-	74ALVCH16821 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ALVCH16821DL (SOT371-1 / SSOP56) removed</li> </ul>			
74ALVCH16821 v.2	19980529	Product specification	-	74ALVCH16821 v.1
74ALVCH16821 v.1	19980529	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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